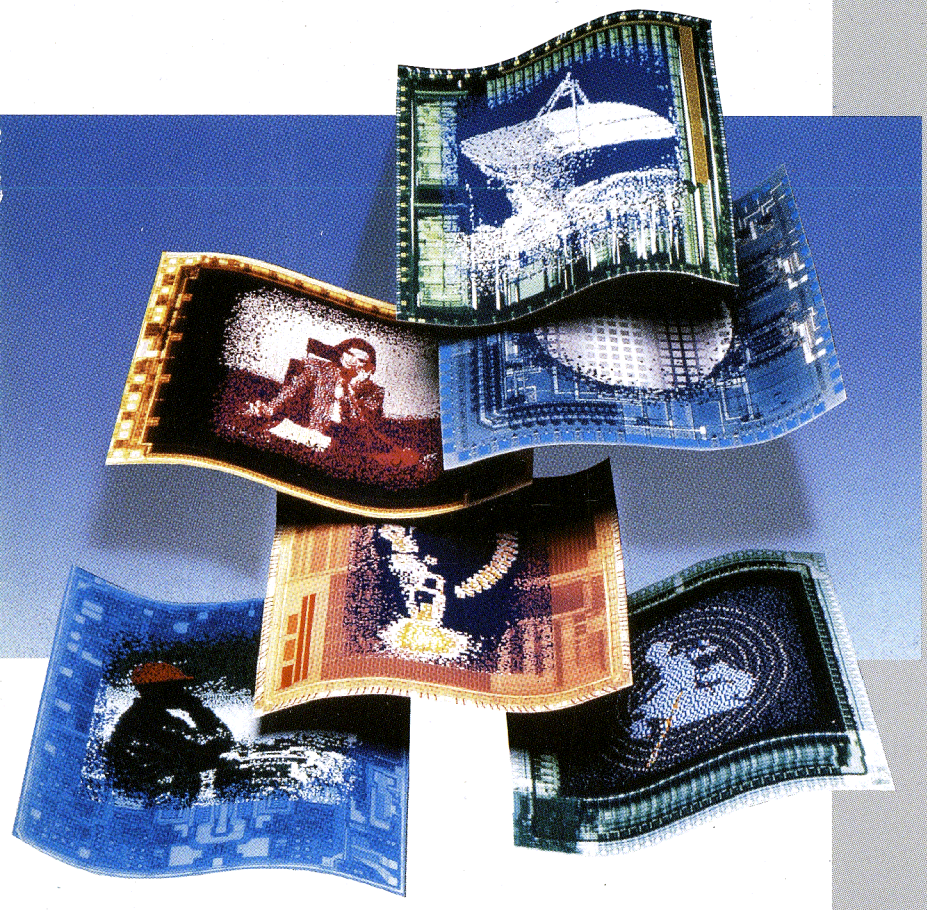
Professional Products

IC Handbook

June 1994



GEC PLESSEY
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DATASHEET ANNOTATION

GPS annotate datasheets in the top right hand corner of the first page, to indicate product status. These annotations are as follows:-

TARGET SPECIFICATION

This is the most tentative form of information and represents a very preliminary product specification. No actual design work on the product has started.

PRELIMINARY INFORMATION

The product is in design and development. The datasheet represents the product as it is understood but details may change.

ADVANCE INFORMATION

The product design is complete and final characterisation for volume production is well in hand.

No annotation

The product parameters are fixed and the product is available to datasheet specification in volume.

If you have any queries about the status of any GPS product, please contact your nearest GPS Customer Service Centre.

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Foreword

This Professional Products IC Handbook replaces the previous version (Publication Number PS2480, May 1991) and the High Speed Silicon Frequency Dividers Summary (Publication Number LF3704, November 1992). It excludes certain specialist personal communications products which are now published in the Personal Communications IC Handbook (Publication Number HB2123).

Existing circuits are covered as well as a range of new designs. The bipolar synthesiser family has been enhanced by the addition of the SP8858 and SP885xD phase lock loop devices. These offer up to 1.7GHz frequency operation, a wide range of RF and Reference Division ratios plus a phase noise performance that leaves similar PLLs far behind. It is our intention to further enhance this product area, with the introduction of even higher frequency devices, over the next 12 months.

Many devices included in this handbook have extended operating temperature ranges and more package options, especially surface mount. The number of devices available to internationally approved screening standards also has increased, as has the number of fully approved DESC product datasheets.

Contents

Product index

Logarithmic/Limiting Amplifier

Type No.	Description	Bandwidth	Dynamic Range	Page
SL3522	Monolithic 6 stage amplifier (successive detection)	600MHz	70dB	83

Logarithmic Amplifiers

Type No.	Description	Supply Voltage	Supply Current	Bandwidth	Noise Figure	Gain	Page
SL1613	Successive detection	6V	15mA	80MHz	4.5dB	12dB (±2.0)	49
SL1615	Successive detection	6V	15mA	80MHz	4dB	12dB (±1.0)	52
SL2524A#	Dual successive detection	6V	90mA	300MHz	9dB	12dB	61
SL2524B/C#	Dual successive detection	6V	90mA	1000MHz	9dB	12dB	61
SL521A/B/C#	Successive detection	6V	15mA	165MHz	4dB	12dB	17
SL523B/C/CB*#	Dual successive detection	6V	30mA	100MHz	4dB	24dB (±1.4)	21
SL531#	True Log amp	9V	17mA	500MHz		10dB (±2)	25
SL532#	Low Phase Shift Limiter	9V	10mA	400MHz	7dB	10dB (±2)	28

* Supplied in matched sets if required. # DESC approved Standard Militarised Drawings.

Wideband Amplifier

Type No.	Description	Supply Voltage	Supply Current	Bandwidth	Noise Figure	Gain	Page
SL560C/AC	Low Noise amplifier	2-15V	20mA	300MHz	2dB	40dB	38

Operational Amplifier

Type No.	Description	Supply Voltage	Supply Current	Bandwidth	Noise Figure	Gain	Page
SL541	High Slew Rate Op amp	+12V.-6V	16mA	100MHz	5mV	70dB	31

Very Low Noise Amplifiers

Type No.	Function	Bandwidth	Gain	Input Noise Voltage	Page
SL561	Preamplifier	6.0MHz	60dB	0.8nV/√Hz (Typical)	43
ZN459	Preamplifier	15MHz	60dB	0.8nV/√Hz (Typical)	118
ZN460	Programmable gain/bandwidth preamplifier	6.0MHz	50-60dB	0.8nV/√Hz (Typical)	126

Matched Transistor Arrays

Type No.	Description	LV CEO Min	LV CEO Typ	Icm	Typ. Cut-off Frequency	No. of Transistors	hFE (Min)	Page
SL2364	Very high performance transistor arrays	6V	9V	12mA	5.0GHz	6	20 at 8mA	58
SL2365	Very high performance transistor array	6V	9V	8mA	5.0GHz	8	50 at 8mA	60
SL3145	NPN transistor arrays	15V	25V	20mA	1.6GHz	5	40 at 1mA	75
SL3227	NPN transistor arrays	6V	9V	12mA	3.0GHz	5	40 at 1mA	79
SL3245	NPN transistor array	6V	9V	12mA	3.0GHz	5	40 at 1mA	81

Radiocoms

Type No.	Function	Page
SL1640	Double balanced modulator	56
SL610C	RF Amplifier 85MHz, 20dB - AGC capability	46
SL611C	RF Amplifier 50MHz, 26dB - AGC capability	46
SL612C	RF Amplifier 15MHz, 34dB - AGC capability	46
SL6140	0-400MHz, 70dB - AGC range, 45dB gain	100
ZN414	AM radio receiver	108
ZN416	AM radio receiver	108

Radio Synthesisers

Type No.	Function	Process	Page
SP2002A	Direct digital synthesiser with 350MHz output	Bipolar	137
SP2002B	Direct digital synthesiser with 400MHz output	Bipolar	137
SP8852D	Low noise 1.7GHz professional synthesiser	Bipolar	144
SP8853A	Low power 1.3GHz professional synthesiser	Bipolar	158
SP8853B	Low power 1.5GHz professional synthesiser	Bipolar	158
SP8854D	Low noise 1.7GHz professional synthesiser	Bipolar	170
SP8855D	Low noise 1.7GHz professional synthesiser	Bipolar	184
SP8858	Ultra low noise 1.5GHz professional synthesiser	Bipolar	198
SP8861	Low power 1.3GHz professional synthesiser	Bipolar	206

Ultra Low Phase Noise Dividers

Type No.	Function	Division Ratio	Minimum Frequency	Maximum Frequency	Typical Phase Noise at 1kHz Offset	Page
SP8400	Dual modulus divider	8/9	200MHz	1.5GHz	156dBc/Hz	221
SP8401	Dual modulus divider	10/11	50MHz	300MHz	160dBc/Hz	225
SP8402	Divide by 2^N	2/4/8/16/32/64/128/256	200MHz	1.4GHz	155dBc/Hz	228

Two-Modulus Programmable Dividers

Type No.	Division Ratio	Frequency	Maximum Supply Current	Supply Voltage	Page
SP8720A/B	3/4	300MHz	65mA	-5.2V	283
SP8741#	6/7	300MHz	60mA	-5.2V	292
SP8691A	8/9	200MHz	21mA	+5 or -5.2V	275
SP8690A/B#	10/11	200MHz	21mA	+5 or -5.2V	275
SP8695A	10/11	200MHz	21mA	+5 or -5.2V	279
SP8647AC/B#	10/11	250MHz	65mA	+5V or -5.2V	249
SP8685A/B	10/11	500MHz	70mA	-5.2V	271
SP8680A	10/11	575MHz	105mA	+4V	262
SP8680B	10/11	575MHz	105mA	+4V	267
SP8789	20/21	200MHz	7mA	+5.2V	299

DESC approved Standard Militarised Drawings.

Fixed Modulus Dividers

Divide by	Type No.	Maximum Frequency	Supply Voltage	Maximum Current	Page
2	**SP8604A/B**	300MHz	5.2V	18mA	232
2	**SP8602A/B#**	500MHz	5.2V	18mA	232
2	**SP8607A/B**	600MHz	5.2V	18mA	239
2	**SP8605B**	1000MHz	5.2V	100mA	235
2	**SP8606B**	1300MHz	5.2V	100mA	235
2	**SP8802A**	3300MHz	5.0V	100mA	312
4	**SP8790A/B**	60MHz	5.0V	11mA	302
4	**SP8610A/B**	1000MHz	5.2V	100mA	242
4	**SP8611A/B**	1300/1500MHz	5.2V	100mA	242
4	**SP8804A**	3300MHz	5.0V	90mA	319
8	**SP8794A/B**	120MHz	5.0V	11mA	305
8	**SP8735B**	600MHz	5.2V	90mA	287
8	**SP8808A**	3300MHz	5.0V	85mA	322
10	**SP8630B#**	600MHz	5.2V	70mA	246
10	**SP8830A/B**	1500MHz	5.0V	50mA	325
10	**SP8660**	150MHz	5.0V	13mA	256
16	**SP8659B**	200MHz	5.0V	13mA	253
16	**SP8801A**	3300MHz	5.0V	90mA	308
16	**SP8831B**	3500MHz	5.0V	90mA	328
20	**SP8657A**	200MHz	5.0V	13mA	253
32	**SP8655A**	200MHz	5.0V	13mA	253
32	**SP8803A**	3300MHz	5.0V	90mA	315
32	**SP8833B**	3500MHz	5.0V	90mA	332
64	**SP8755A/B#**	1200MHz	5.0V	75mA	296

DESC approved Standard Militarised Drawings.

Product List - Alpha numeric

The Quality Concept

Quality cannot be inspected into a product; it is only by careful design and evaluation of materials, parts and processes (followed by strict control and on-going assessment) that quality products will be produced.

All designs conform to standard layout rules, all processes are thoroughly evaluated and all new piece part designs and suppliers are investigated before authorisation for production use.

The same basic procedures are used on all products up to and including device packing. It is only then that extra operations are performed for certain customers in terms of lot qualification or release procedure.

By working to common procedures, all users benefit; the high reliability user gains the advantage of scale (hence improving the confidence factor in the quality achieved), while the volume user gains from the benefits of basic high reliability design concepts.

GEC Plessey Semiconductors (GPS) have the following factory approvals:
AQAP1
BS9450 (Capability Approval)
MIL-STD-883 Class B (In conformance with the requirements of MIL-STD-883, paragraph 1.2.1)
DESC (Department of Electronics Supply Center - Device approvals)

Screening

Different screening procedures are carried out by GPS; a brief description of the differences involved are set out in Tables 1 and 2.

Stage/ operation	Standard product	GPS Hi-rel A	GPS Hi-rel B	MIL-STD-883 Class B	MIL-STD-883 Class S[1]
Wafer-fab					Wafer-lot accept Method 5007
Probe test	100%	100%	100%	100%	100%
Visual inspect chips	Usually 2010 Cond.B	2010 Cond.B	2010 Cond.B	2010 Cond.B	2010 Cond.A
Assemble					Includes 100% bond pull
Screen	None	Method 5004 Class B	As Table 2	Method 5004 Class B	Method 5004 Class S
Test	100%	100%	100%	100%	100%
Conformance testing	None	Method 5005 Class B Group A Group B Group C Group D	None	Method 5005 Class B Group A Group B Group C Group D	Method 5005 Class S Group A Group B Group C Group D

Table 1

1. MIL-STD-883 Class S/ESA SCC9000: GPS has supplied numerous devices to customer specifications for Space and Satellite applications. Please contact your local GPS sales office for information.

Stage/ operation	GPS Hi-rel B (References are to MIL-STD-883)	MIL-STD-883 Class B Method 5004[2]
Internal Visual	Method 2010 Test Condition B 100%	Method 2010 Test Condition B 100%
Stabilisation Bake	Method 1008 24Hrs at Condition C 100%	Method 1008 24Hrs at Condition C 100%
Temperature Cycling	Method 1010 Test Condition C 100%	Method 1010 Test Condition C 100%
Constant Acceleration	Method 2010 Condition E Y1 only 100%	Method 2010 Condition E Y1 only 100%
Visual Inspection		100%
Initial Electrical	Those parameters requiring Delta calculations. 100%	Those parameters requiring Delta calculations. 100%
Burn-In	Method 1015 160Hrs at 125°C min. 100%	Method 1015 160Hrs at 125°C min. 100%
Post Burn-In Electrical Test	Full Electrical Test to Guarantee datasheet. 100%	Those parameters requiring Delta calculations. 100%
PDA Calculation	5% max. All lots	5% max. All lots
Final Electrical Test	Done as Post Burn-In Test. 100%	Full Group A tests as Method 5005. 100%
Seal (a) Fine Seal (b) Gross	Method 1014 100%	Method 1014 100%
Qualification/Quality Conformance Test		Method 5005 Class B Samples as necessary
External Visual	GPS Spec. sample	Method 2009 100%

Table 2

2. See Section 5 for further information.

Standard Militarized Drawings (SMDs)

GEC Plessey Semiconductors has actively pursued a program of obtaining SMDs for our Professional products.

These products are qualified and approved as SMDs by DESC (Defense Electronics Supply Center), Ohio, USA.

As products are approved, they are listed in MIL-BUL-103 (list of standardized military drawings) and are 'preferred' for use in projects requesting the use of SMD qualified parts.

GPS products with approved SMDs conform to class 'M' (non-Jan Class 'B' microcircuits in accordance with para.1.2.1. of MIL-STD-883 latest revision. These are generally equivalent to the earlier GPS 'AC' series of devices.

SMD Number	Device	Ordering Information
5962-92315	SL2524	DES9231501/AC/LCAZ
5962-90792	SL521	DES9079201/AC/CMAR
5962-90792	SL521	DES9079201/AC/CMCR (Solder-DIP Leads)
5962-89803	SL523	DES8980301/AC/CMAR
5962-89803	SL523	DES8980301/AC/CMCR (Solder-DIP Leads)
5962-92084	SL531	DES9208401/AC/CMAR
5962-92084	SL531	DES9208401/AC/CMAR (Solder-DIP Leads)
5962-90521	SL532	DES9052101/AC/CMAR
5962-90521	SL532	DES9052101/AC/CMCR (Solder-DIP Leads)
5692-90520	SL560	DES9052001/AC/CMAR
5692-90520	SL560	DES9052001/AC/CMCR (Solder-DIP Leads)
5962-92059	SP8602	DES9205901/AC/CMAR
5962-92059	SP8602	DES9205901/AC/CMCR (Solder-DIP Leads)
5962-90970	SP8620	DES9097001/AC/DGAZ
5962-92003	SP8630	DES9200301/AC/DGAZ
5962-90618	SP8647	DES9061801/AC/DGAZ
5962-92088	SP8670	DES9208801/AC/DGAZ
5962-87678	SP8690	DES8767801/AC/DGAZ
5962-88617	SP8718	DES8861701/AC/DGAZ
5962-90577	SP8720	DES9057701/AC/DGAZ
5962-91590	SP8741	DES9159001/AC/DGAZ
5962-88684	SP8755	DES8868401/AC/DGAZ
5962-90661	SP8802	DES9066101/AC/DGAZ
5962-91572	SP8830	DES9157201/AC/DGAZ

Section 1
Linear Circuits

MIL-STD-883 Class B

Many of the integrated circuits detailed in this section are available screened in conformance with MIL-STD-883 Class B and are identified in their ordering codes by the letters **AC** immediately following the device type number. Separate data sheets for these circuits are available from your local GEC Plessey Semiconductors Sales Office.

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SL521

150MHz WIDEBAND LOG AMPLIFIER

The SL521A, B and C are bipolar monolithic Integrated circuit wideband amplifiers, intended primarily for use in successive detection logarithmic IF strips, operating at centre frequencies between 10MHz and 100MHz The devices provide amplification, limiting and rectification, are suitable for direct coupling and incorporate supply line decoupling The mid-band voltage gain of the SL521 is typically12dB(4times) The SL521A, B and C differ mainly in the tolerance of voltage gain and upper cut-off frequency

The device is also available as the 5962-90792 which has guaranteed operation over the full Military Temperature Range and is screened to MIL-STD-883 Class B. Data is available separately

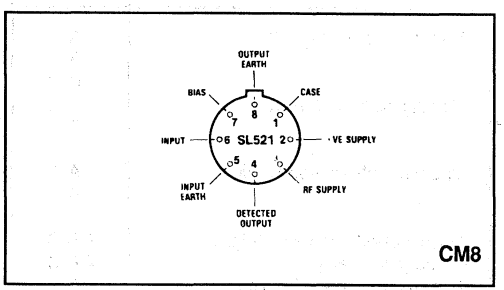


Fig.1 Pin connections - bottom view

FEATURES

- Wide Defined Gain
- 4dB Noise Figure
- Hlgh I/P impedance
- Low O/Pi mpedance
- 165MHz Bandwidth
- On Chip Supply Decoupling
- Low External Component Count

ORDERING INFORMATION

SL521 A CM **5962-90792 (SMD)**
SL521 B CM
SL521 C CM

ABSOLUTE MAXIMUM RATINGS
(Non-simultaneous)

Storage temperature range	-65°C to +150°C
Operating temperature range	-55°C to +125°C
Chip operating temperature	+175°C
Chip-to-ambient thermal resistance	225°C/W
Chip-to-case thermal resistance	65°C/W
Maximum instantaneous voltage at Video output	+12V
Supply voltage	+9V

APPLICATIONS

- Logarithmic IF Strips wlth Gains up to 108dB and Linearity better than 1dB

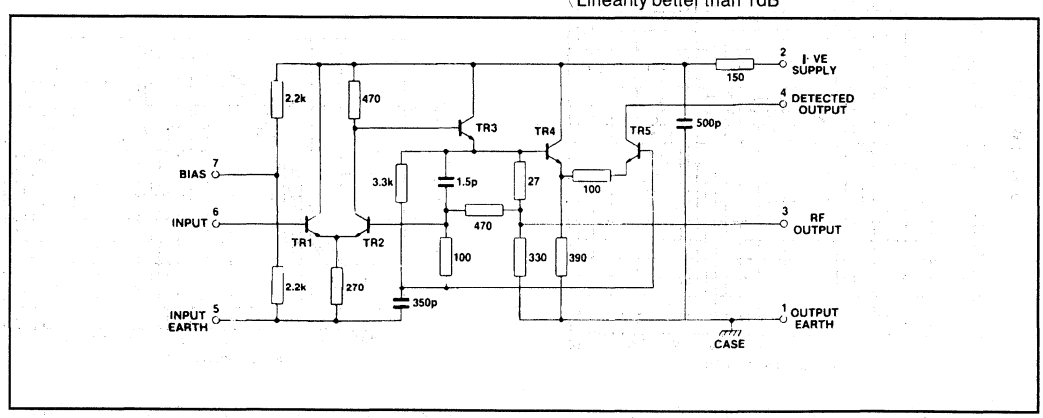


Fig.2 Circuit diagram SL521

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated)

Temperature = +22°C + 2°C
Supply voltage = +6V
DC connection between input and bias pins.

Characteristic	Circuits	Value			Units	Conditions
		Min.	Typ.	Max.		
Voltage gain, f = 30MHz	A	11.5		12.5	dB	10 ohms source, 8pF load
	B	11 .3		1 2.7	dB	
	C	11.0		13.0	dB	
Voltage gain, f = 60MHz	A	11.3		12.7	dB	
	B	11.0		13.0	dB	
	C	10.7		13.3	dB	
Upper cut-off frequency (Fig. 3)	A	150	170		MHz	10 ohms source, 8pF load
	B	140	170		MHz	
	C	130	170		MHz	
Lower cut-off frequency (Fig. 3)	A B C		5	7	MHz	10 ohms source, 8pF load
Propagation delay	A B C		2		ns	
Maximum rectified video output current (Fig. 4 and 5)	A	1.00		1.10	mA	f = 60MHz, 0.5V rms input
	B	0.95		1.15	mA	
	C	0.90		1.20	mA	
Variation of gain with supply voltage	A B C		0.7		db/V	
Variation of maximum rectified output current with supply voltage	A B C		25		%/V	
Maximum input signal before overload	A B C	1.8	1.9		V rms	See note below
Noise figure (Fig. 6)			4	5.25	dB	f = 60MHz, Rs = 450 ohms
Supply current	A	12.5	15.0	18.0	mA	
	B	12.5	15.0	18.0	mA	
	C	11.5	15.0	19.0	mA	
Maxiumum RF output voltage			1.2		Vp-p	

Note: Overload occurs when the input signal reaches a level sufficient to forward bias the base-collector junction to TR2 on peaks.

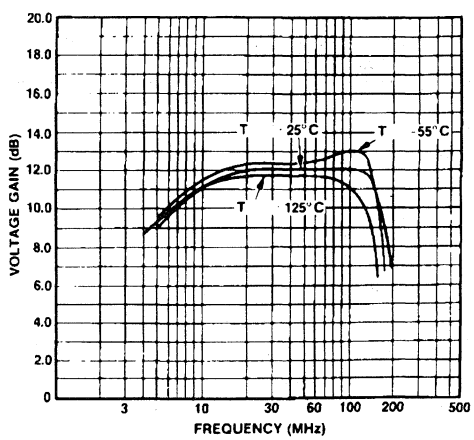


Fig.3 Voltage gain v. frequency (typical)

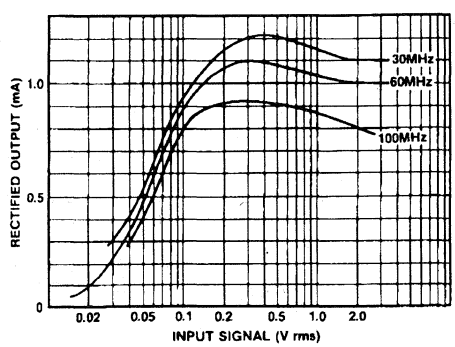


Fig.4 Rectified output current v. input signal (typical)

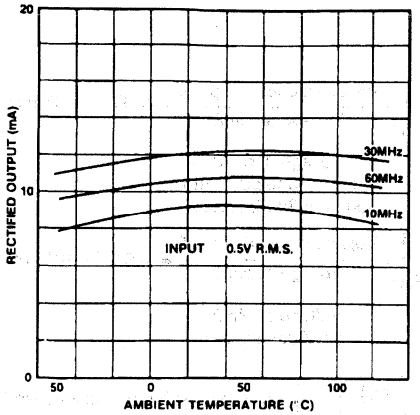


Fig.5 Maximum rectified output current v. temperature (typical)

OPERATING NOTES

The amplifiers are intended for use directly coupled, as shown in Fig 8.

The seventh stage in an untuned cascade will be giving virtually full output on noise.

Noise may be reduced by inserting a single tuned circuit in the chain As there is a large mismatch between stages a simple shunt or series circuit cannot be used The choice of network is also controlled by the need to avoid distorting the logarithmic law; the network must give unity voltage transfer at resonance A suitable network is shown in Fig 9. The value of C1 must be chosen so that at resonance its admittance equals the total loss conductance across the tuned circuit Resistor R1 may be introduced to improve the symmetry of filter response, providing other values are adjusted for unity gain at resonance.

A simple capacitor may not be suitable for decoupling the output line if many stages and fast rise times are required. Alternative arrangements may be derived, based on the parasitic parameters given.

Values of positive supply line decoupling capacitor required for untuned cascades are given below. Smaller values can be used in high frequency tuned cascades.

	Number of stages			
	6 or more	5	4	3
Minimum capacitance	30nF	10nF	3nF	InF

The amplifiers have been provided with two earth leads to avoid the introduction of common ground lead inductance between input and output circuits. The equipment designer should take care to avoid the subsequent introduction of such inductance.

The 500pF supply decoupling capacitor has a resistance of, typically, 1 0Q. It is a junction type having a low breakdown voltage and consequently the positive supply current will increase rapidly if the supply voltage exceeds 7.5V (see Absolute Maximum Ratings).

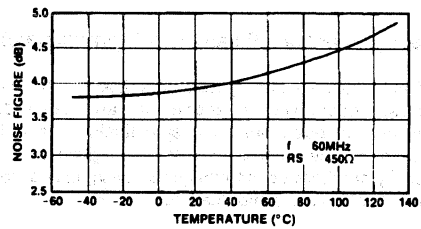


Fig.6 Noise figure v. temperature (typical)

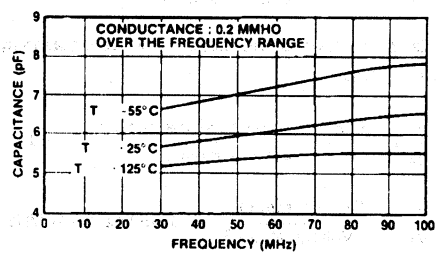


Fig.7 Input admittance with open-circuit output (typical)

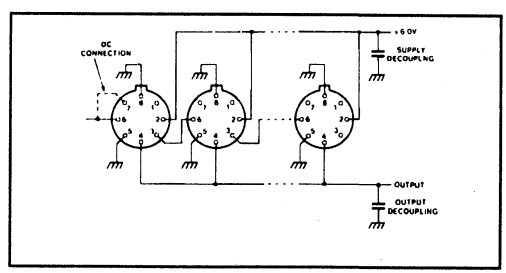


Fig.8 Direct Coupled amplifiers

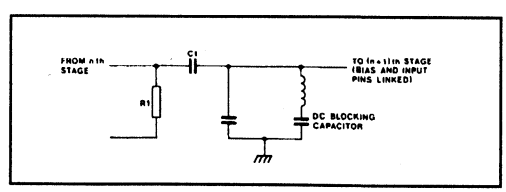


Fig.9 Suitable interstagetuned circuit

Parasitic Feedback Parameters (Approximate)

The quotation of these parameters does not indicate that elaborate decoupling arrangements are required, the amplifier has been designed specifically to avoid this requirement. The parameters have been given so that the necessity or otherwise of further decoupling, may become a matter of calculation rather than guesswork.

$$\frac{\tilde{I}_4}{V_6} = \frac{\text{RF current component from pin 4}}{\text{Voltage at pin 6}} = 20 \text{ mmhos}$$

(This figure allows for detector being forward biased by noise signals).

$$\frac{V_4}{V_6} = \frac{\text{Effective voltage induced at pin 6}}{\text{Voltage at pin 4}} = 0.003$$

$$\frac{I_2}{V_6} = \frac{\text{Current from pin 2}}{\text{Voltage at pin 6}} = 6 \text{ mmhos (f = 10MHz)}$$

$$\left[\frac{V_6}{V_2}\right]_a = \frac{\text{Voltage induced at pin 6}}{\text{Voltage at pin 2}} = 0.03 \text{ (f = 10MHz)}$$

Voltage at pin 2
(pin joined to pin 7 and fed from 300Ω source)

$$\left[\frac{V_6}{V_2}\right]_b = \frac{\text{Voltage induced at pin 6}}{\text{Voltage at pin 2}} = 0.01 \text{ (f = 10MHz)}$$

Voltage at pin 2
(pin 7 decoupled)

$\frac{I_2}{V_6}$ $\left[\frac{V_6}{V_2}\right]_a \left[\frac{V_6}{V_2}\right]_b$ decrease with frequency above 10MHz at 6dB/octave

SL523

100MHz DUAL WIDEBAND LOG AMPLIFIER

The SL523B and C are wideband amplifiers for use in successive detection logarithmic IF strips operating at centre frequencies between 10 and 100MHz They are pin compatible with the SL521 series of logarithmic amplifiers and comprise two amplifiers internally connected in cascade Small signal voltage gain is 24dB and an internal detector with an accurate logarithmic characteristic over a 20dB range produces a maximum Output of 2.1 mA. A strip of SL523s can be directly coupled and decoupling is provided on each amplifier RF limiting occurs at an input voltage of 25mV RMS but the device will withstand input voltages up to 1 8V RMS without damage

The device is also available as the 5962-89803 which has guaranteed operation over the full Military Temperature Range and is screened to MIL-STD-883 Class B. Data is available separately.

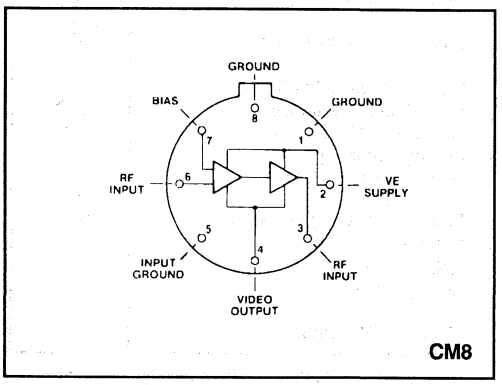


Fig.1 Pin connections (view from beneath)

FEATURES

- Small Size/Weight
- Low Power Consumption
- Readily Cascadable
- Accurate Logarithmic Detector Characteristic

QUICK REFERENCE DATA

- Small Signal Voltage Gain: 24dB
- Detector Output Current: 21mA
- Noise Figure: 4dB
- Frequency Range: 10-100MHz
- Supply Voltage +6V
- Supply Current 30mA

ABSOLUTE MAXIMUM RATINGS

(Non-simultaneous)

Storage temperature range	-65°C to +150°C
Operating temperature range	-55°C to +125°C
Thermal resistance	
Chip-to-ambient	200°C/W
Chip-to-case	52°C/W
Maximum instantaneous voltage at video output	+12V
Supply voltage	+9V

ORDERING INFORMATION

SL523 B CM
SL523 C CM
SL523 CB CM
5962-89803 (SMD)

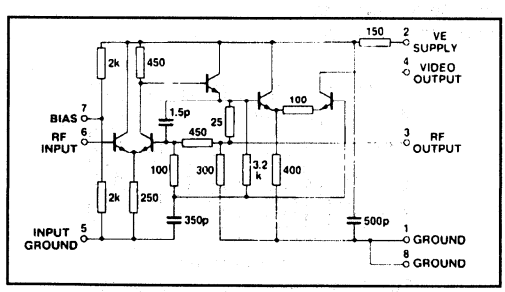


Fig.2 Circuit diagram (one amplifier)

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated)

Ambient temperature = 22°C ± 2°C; Source impedance = 10Ω; Supply voltage = +6V; Load impedance = 8pF; Frequency = 60MHz; DC connection between Pin 6 and 7

Characteristic	Circuits	Value			Units	Conditions
		Min.	Typ.	Max.		
Small signal voltage gain	B	22.6	24	25.4	dB	} Frequency = 30MHz
	C	22	24	26	dB	
Small signal voltage gain	B	22	24	26	dB	} Frequency = 60MHz
	C	21.4	24	26.6	dB	
Gain variation (set of 8)			0.5	0.75	dB	Frequency = 60MHz
Upper cut-off frequency	B, C	120	150		MHz	
Lower cut-off frequency	B, C		10	15	MHz	
Propagation delay	B, C		4		ns	
Maximum rectified video output current	B	1.9	2.1	2.3	mA	
	C	1.8	2.1	2.4	mA	
Maximum input signal before overload	B, C	1.8	1.9		V RMS	See note below
Noise figure			4	5.25	dB	Source impedance 450Ω
Supply current	B	25	30	36	mA	
	C	23	30	38	mA	
Maximum RF output voltage	B, C		1.2		V p-p	

Note:- Overload occurs when the input signal reaches a level sufficient to forward bias the base-collector junction to the input transistor on peaks

OPERATING NOTES

The amplifier is designed to be directly coupled (seeFig.5)

The fourth stage in an untuned cascade will give full output on the broad band noise generated by the first stage.

Noise may be reduced by inserting a single tuned circuit in the chain As there is a large mismatch between stages a simple shunt or series circuit cannot be used The network chosen must give unity voltage gain at resonance to avoid distorting the log law The typical value for input impedance is 500Ω in parallel with 5pF and the output impedance is typically 30Ω.

Although a 1nF supply line decoupling capacitor is included in the can an extra capacitor is required when the amplifiers are cascaded Minimum values for this capacitor are: 2 stages - 3nF, 3 or more stages 30nF

In cascades of 3 or more stages care must be taken to avoid oscillations caused either by inductance common to the input and output earths of the strip or by feedback along the common video line The use of a continuous earth plane will avoid earth inductance problems and a common base amplifier in the video line isolating the first two stages as shown in Fig 6 will eliminate feedback on the video line

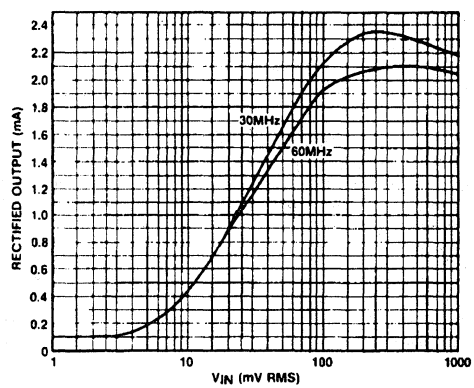


Fig.3 Rectified output current v. input signal (typical)

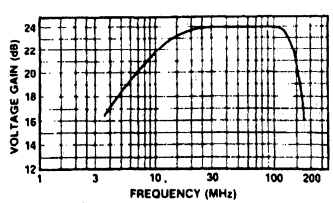


Fig.4 Voltage gain v. frequency (typical)

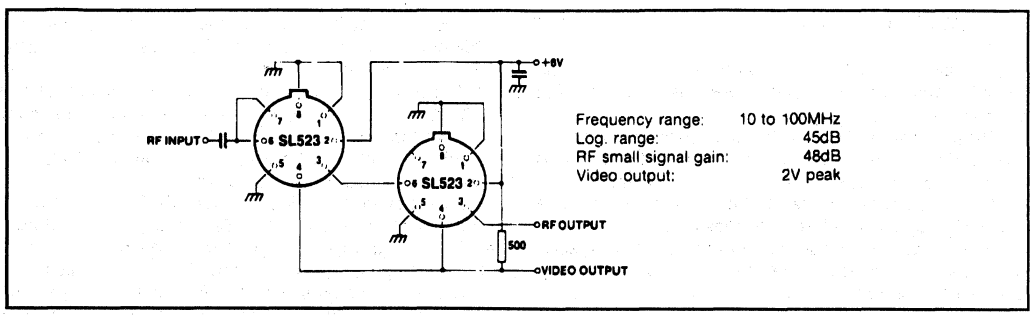


Fig.5 Simple log. IF strip

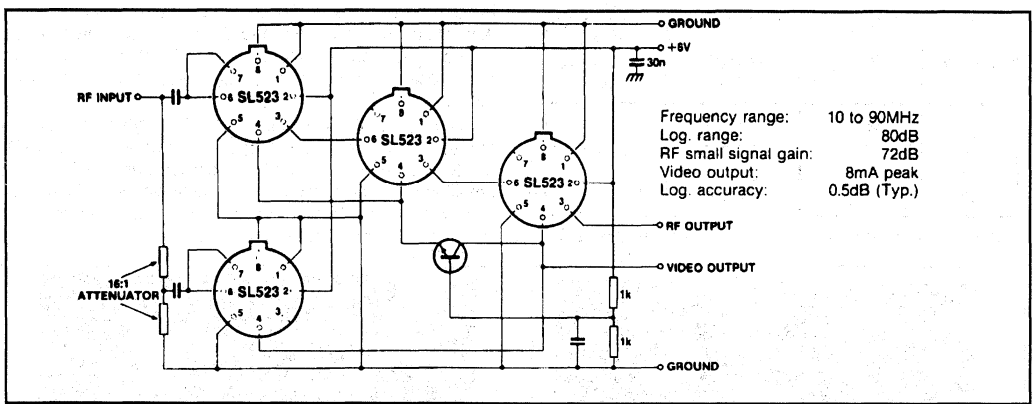


Fig.6 Wide dynamic range log. IF strip

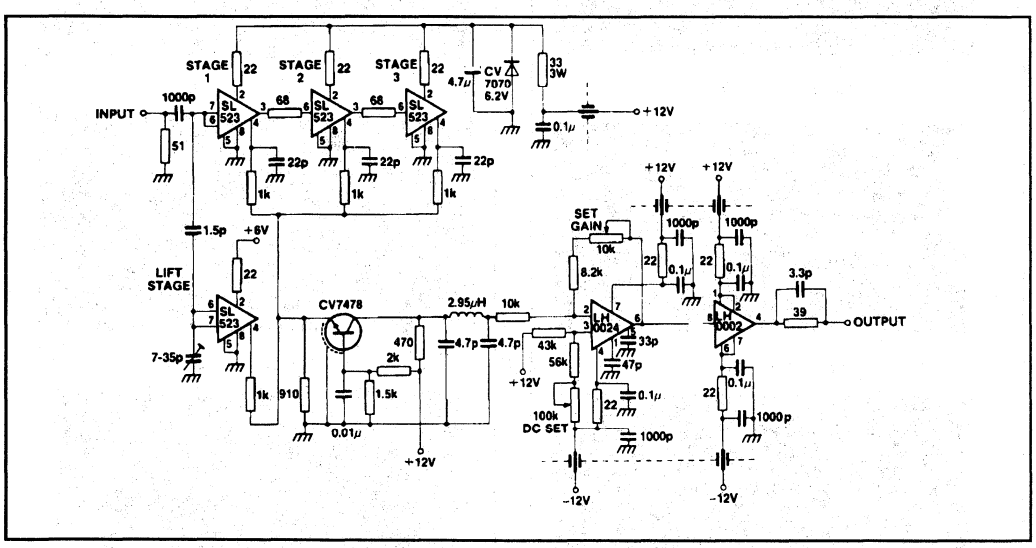


Fig.7 Wideband logarithmic amplifier

TYPICAL PERFORMANCE

Unselected SL523B devices were tested in a wideband logarithmic amplifier. described in RSRE Memo No 3027 and shown in Fig 7

The amplifier consists of six logarithmic stages and two 'lift' stages, giving an overall dynamic range of greater than 80dB The response and error curves were plotted on an RHG Log Test Set and bandwidth measurements were made with a Telonic Sweeper and Tektronix oscilloscope

Fig 8 shows the dynamic range error curve and f requency response obtained. The stage gains of the SL523 devices used were as shown in Table 1

Stages	fo (MHz)	Gain (dB)	Max. Deviation (dB)
1	60	24.1 23	
2	60	24.089	0.235
3	60	23.888	
Lift	60	24.086	

Table 1 Stage gains of SL523 used in performance tests

The input v output characteristic (Fig.8a) is calibrated at 10dB/cm in the X axis and 1 V/cm in the Y axis 80dB of dynamic range was attained

The error characteristic (Fig 8b) is calibrated at 10dB/cm in the X axis and 1dB/cm in the Y axis; this shows the error between the log input v. output characterisitc and a mean straight line and shows that a dynamic range of 80dB was obtained with an accuracy of ±0.5dB

As a comparison, the log amplifier of Fig 7 was constructed with randomly selected SL521 Bs (two SL521 Bs replacing each SL523B). Again, a dynamic response of 80dB was obtained (Fig 9a) with an accuracy of 1 0 75dB (Fig.9b)

Bandwidth curves are shown in Figs.8c and 9c, where the amplitude scale is 2dB/cm, with frequency markers at 10MHz intervals from 20 to 100MHz Using SL523Bs (Fig.8c), the frequency response at 90MHz is 4dB down on maximum and there is a fall-off in response after 50MHz Fig 9c shows that the frequency response of the amplifier falls off more gradually after 40MHz but again the response at 90MHz is 4dB down on maximum

These tests show that the SL523 is a very successful dual stage log amplifier element and, since it is pin-compatible with the SL521 enables retrofit to be carried out in existing log amplifiers It will be of greatest benefit however, in the design of new log amplifiers, enabling very compact units to be realised with a much shorter summation line

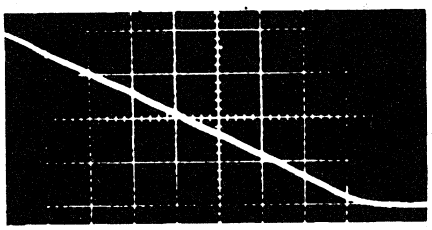


Fig.8a Input/output

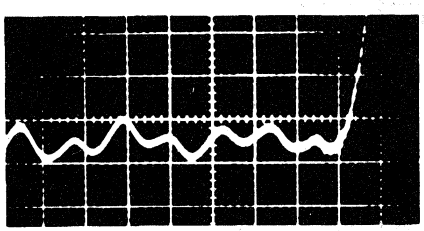


Fig.8b Error curve

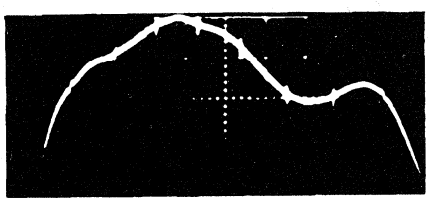


Fig.8c Frequency response, detected output

Fig.8 Characteristics of circuit shown in Fig 7 using SL523Bs

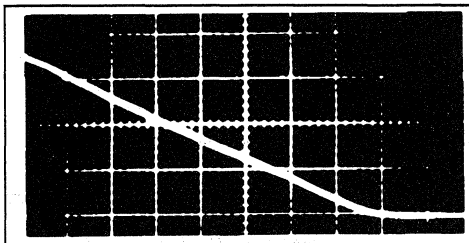


Fig.9a Input/output

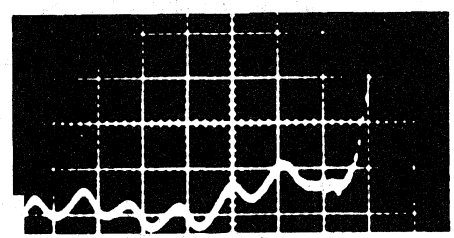


Fig.9b Error curve

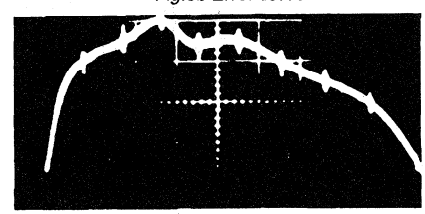


Fig.9 Characteristics of circuit shown in Fig 7 using SL523Bs

SL531

250MHz TRUE LOG IF AMPLIFIER

The SL531 C is a wide band amplifier designed for use in logarithmic IF amplifiers of the true log type. The input and log output of a true log amplifier are at the same frequency i e detection does not occur. In successive detection log amplifiers (using SL521 SL1521 types) the log output is detected.

The small signal gain is 10dB and bandwidth is over 500MHz. At high signal levels the gain of a single stage dropstounity. A cascade of such stages give a close approximation to a log characteristic at centre frequencies between 10and 200MHz.

An important feature of the device is that the phase shift is nearly constant with signal level. Thus any phase information on the input signal is preserved through the strip.

The device is also available as the 5962-92084 which has guaranteed operation over the full Military Temperature Range and is screened to MIL-STD-883 Class B. Data is available separately

FEATURES

- Low Phase Shift vs Amplitude
- On-Chip Supply Decoupling
- Low External Components Count

APPLICATIONS

True Log Strips with:-

- Log Range 70dB
- Centre frequencies 10 - 200MHz
- Phase Shift ± 0.5 degrees / 10dB

ABSOLUTE MAXIMUM RATINGS

(Non-simultaneous)

Supply voltage	+12 volts
Storage temperature range	-65°C to +150°C
Operating temperature range	-55°C to +125°C
	See operating notes
Max junction temperature	175°C
Junction - ambient thermal resistance	220°C/Watt
Junction - case thermal resistance	80°C/Watt

CIRCUIT DESCRIPTION

The SL531 transfer characteristic has two regions For small input signals it has a nominal gain of 10 dB. at large signals the gain falls to unity (see Fig 7) This is achieved by operating a limiting amplifier and a unity gain amplifier in parallel (see Fig 3) Tr1 and Tr4 comprise the long tailed pair limiting amplifier, the tail current being supplied byTrS, see Fig 2 Tr2 and Tr3 form the unity gain amplifier the gain of which is defined by the emitter resistors The outputs of both stages are summed in the 300 ohm resistor and Tr7 acts as an emitter follower output buffer. Important features are the amplitude and phase linearity of the unity gain stage which is achieved by the use of 5GHz transistors with carefully optimised geometries.

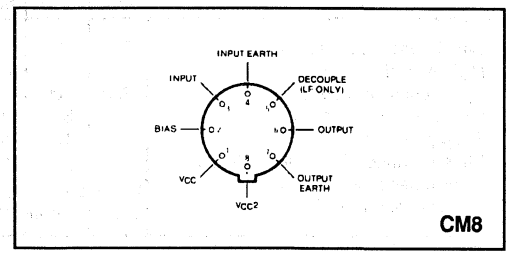


Fig.1 Pin connections

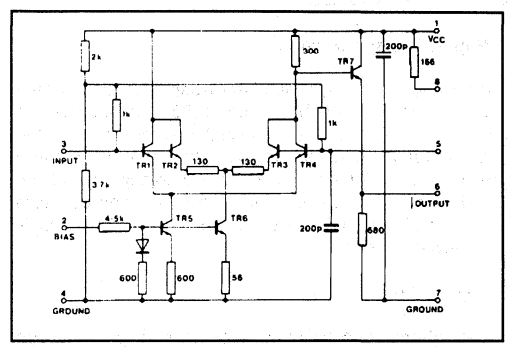


Fig.2 Circuit diagram

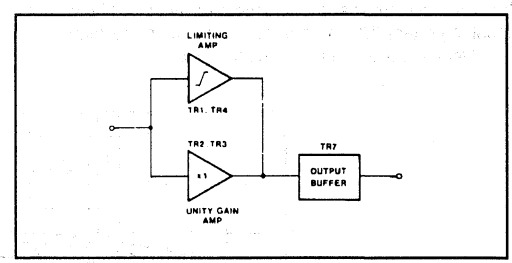


Fig.3 Block diagram

ORDERING INFORMATION

5962-92084 (SMD)
SL531 C CM

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated)

Test circuit Fig (4)
Frequency 60MHz
Supply voltage 9 volts
Ambient temperature 22±2°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Small signal voltage gain	8	10	12	dB	Vin = -30dBm
High level slope gain	-1	0	+1	dB	
Upper cut off frequency	250	500		MHz	
Lower cut off frequency		3	10	MHz	-3dB w.r.t. ± 60MHz
Supply current		17	25	mA	
Phase change with input amplitude		1.1	3	degress	-Vin = 30dBm to +10dBm
Input impedance	2.pF parallel with 1kΩ				f = 10 - 200MHz
Output impedance	15Ω series with 25nH				

OPERATING NOTES

1. Supply Voltage Options

An on chip resistor is provided which can be used to drop the supply voltage instead of the external 180 ohms shown in the test circuit. The extra dissipation in this resistor reduces the maximum ambient operating temperature to 100°C. It is also possible to use a 6 volt supply connected directly to pins 1 and 2 Problems with feedback on the supply line etc may occur in this connection and RF chokes may be required in the supply line between stages.

2. Layout P recautions

The internal decoupling capacitors help prevent high frequency instability however normal high frequency layout precautions are still necessary. Coupling capacitors should be physically small and be connected with short leads. It is most important that the ground connections are made with short leads to a continuous ground plane.

3. Low Frequency Response

The LF response is determined by the on chip capacitors. It can be extended by extra external decoupling on pins 5 and 1.

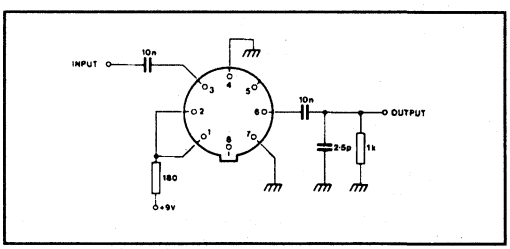


Fig.4 Test ciruit

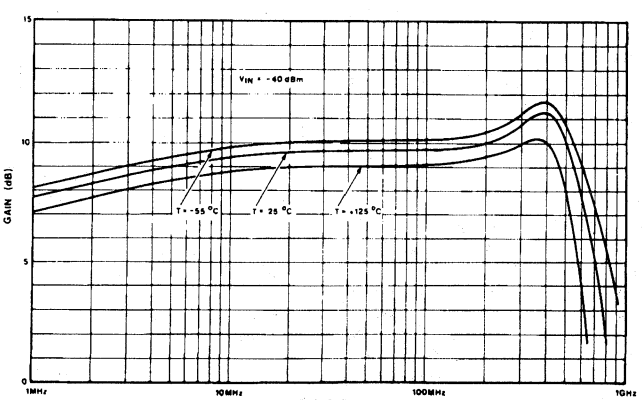


Fig.5 Small signal frequency response

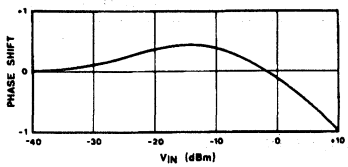


Fig.6 Phase v. input

TYPICAL APPLICATION—6 STAGE LOG STIP

Input log range OdBm to—70dBm
Low level gain 60dB (—70dBm in)
Output dynamic range 20dB
Phase shift (over log range) ±3°
Frequency range 10—200MHz

The circuit shown in Fig 9 is designed to illustrate the use of the SL531 in a complete strip The supply voltage is fed to each stage via an external 180Ω resistor to allow operation to 125°C ambient If the ambient can be limited to +100°C then the internal resistor can be used to reduce the external component count Interstage coupling is very simple with just a capacitor to isolate bias levels being necessary. No connection is necessary to pin 5 unless operation below 10MHz is required. It is important to provide extra decoupling on pin 1 of the first stage to prevent positive feedback occuring down the supply line. An SL560 is used as a unity gain buffer the output of the log strip being attenuated before the SL560 to give a nominal 0dBm output into 50Ω.

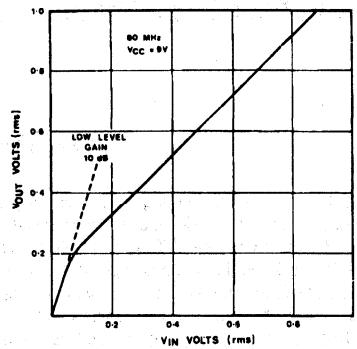


Fig.7 Transfer characteristics linear plot

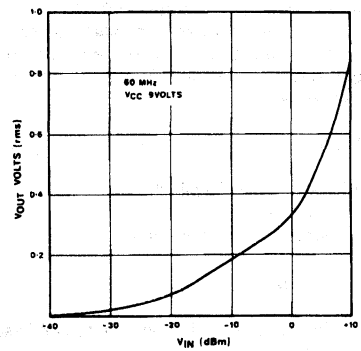


Fig.8 Transfer characteristics logarithmic input scale

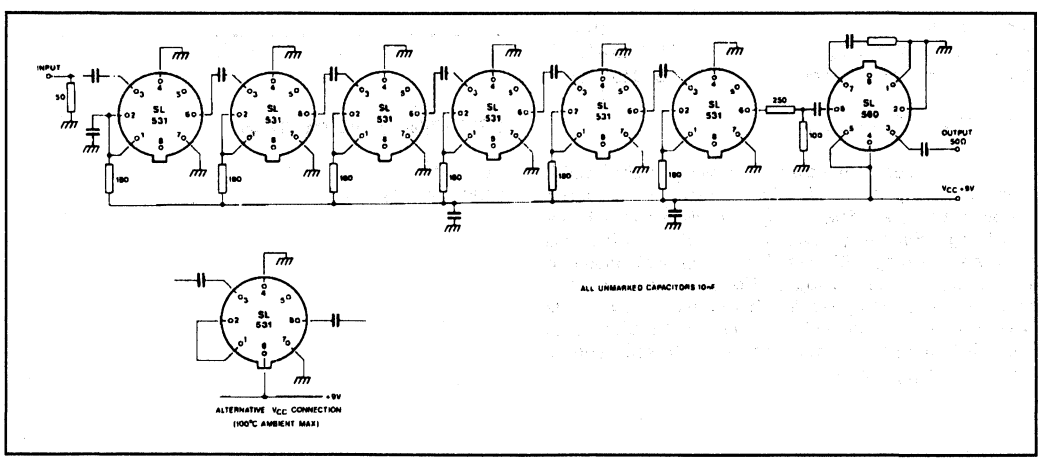


Fig.9 Circuit diagram 6 stage strip

SL532

LOW PHASE SHIFT LIMITER

The SL532C is a monolithic integrated circuit designed for use in wideband limiting IF strips It offers a bandwidth of over 400MHz and very low phase shift with amplitude The small signal gain is 12dB and the limited output is 1V peak to peak The use of a 5GHz IC process has produced a circuit which gives less than 1° phase shift when overdriven by 12dB The amplifier has internal decoupling capacitors to ease the construction of cascaded strips and the number of external components required has been minimised.

The device is also available as the DES9052101/AC/CMAR which has guaranteed operation over the full Military Temperature Range and is screened in accordance with the DESC approved Standardised Military Drawing Data is available separately.

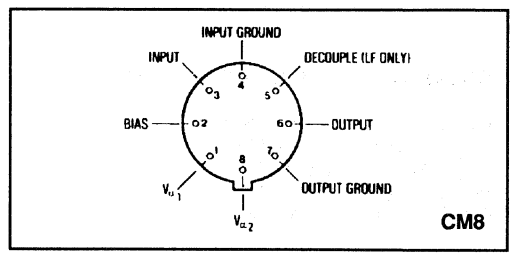


Fig.1 Pin connections

FEATURES

- Low Phase Shift V. Amplitude
- Wide band width
- Low External Component Count

APPLICATIONS

- Phase Recovery Strips in Radar and ECM Systems (e.g. Doppler)
- Limiting Amps for SAW Pulse Compression Systems
- Phase Monopulse Radars
- Phase Array Radars
- Low Noise Oscillators

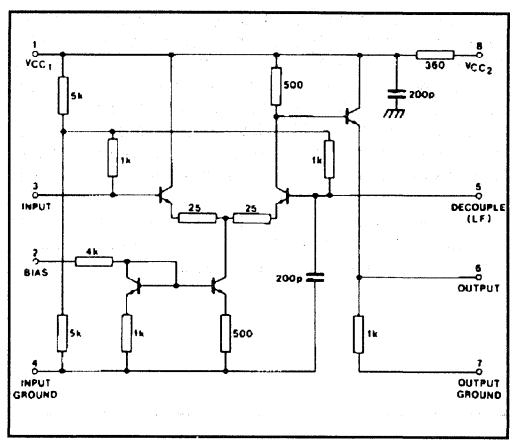


Fig.2 Circuit diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage	+15 volts
Storage temperature range	-55°C to +150°C
Operating temperature range	-55°C to +125°C

CIRCUIT DESCRIPTION

The SL532 uses a long-tailed pair limiting amplifier which combines low phase shift with a symmetrical limiting characteristic. This is followed by a simple emitter follower output stage. Each stage of a strip is capable of driving to full output a succeeding SL532 but a buffer amplifier is needed to drive lower impedance loads. No external decoupling capacitors are normally required but for use below 10MHz extra decoupling can be added on pins 1 and 5. Bias for the long-tailed pair is provided by connecting the bias (pin 2) to the decoupled supply (pin 1).

ORDERING INFORMATION

SL532 C CM
5962-90521 (SMD)

ELECTRICAL CHARACTERISTICS

These characteristics are guaranted over the following conditions (unless otherwise stated):

Temperature (ambient) 25°C ± 2°C
Frequency 60MHz : R_L = 1kΩ/<5pF : V_{IN} = -30dBm
V_{CC} = +9.0V : R_S = 50Ω

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Small signal voltage gain	11	12.8	14	dB	
Small signal voltage gain		12.5		dB	f = 150MHz
-1dB compression point		-10		dBm	
Limited output voltage	1.0	1.15	14	V p-p	V_{IN} = +10dBm
Limited output voltage		1.10		V p-p	f = 150MHz
Upper cut-off frequency	250			MHz	-3dB w.r.t. 60MHz
Lower cut-off frequency			10	MHz	May be extended by decoupling pin 5
Supply current	6	8.5	11	mA	No signal
Phase variation with signal level		±1	±3	Degrees	-30dBm to +10dBm
		±1.5		Degrees	-30dBm to 0dBm. f = 150MHz
Absolute phase shift input to output		-21		Degrees	f = 60MHz
		-34		Degrees	f = 100MHz
		-43		Degrees	f = 150MHz
		-69		Degrees	f = 200MHz
Input impedance		1kΩ/2.5pF			
Output impedance		30Ω			
Noise figure		7		dB	400Ω source impedance. f = 60MHz
Gain variation with temperature		±2		dB	-40°C to 85°C
Phase variation with temperature		±0.5		Degrees	-40°C to +85°C at any level between -30dBm to +10dBm
Limited output voltage variation with temperature		±0.05		V p-p	V_{IN} = +10dBm -40°C to +85°C

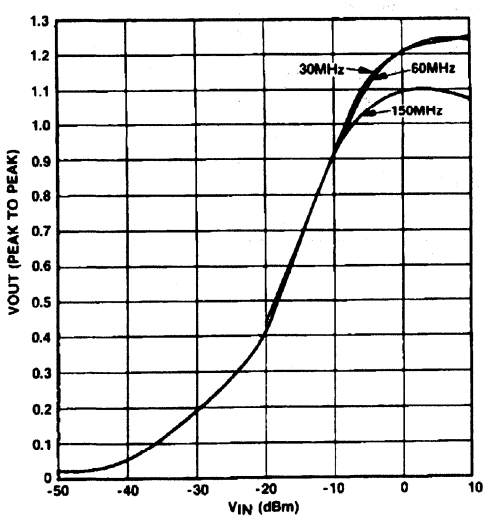


Fig.3 Transfer characteristic of a single stage

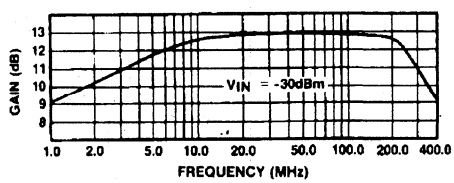


Fig.4 Gain/frequency curve of a typical device

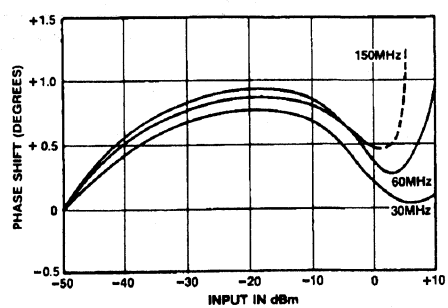
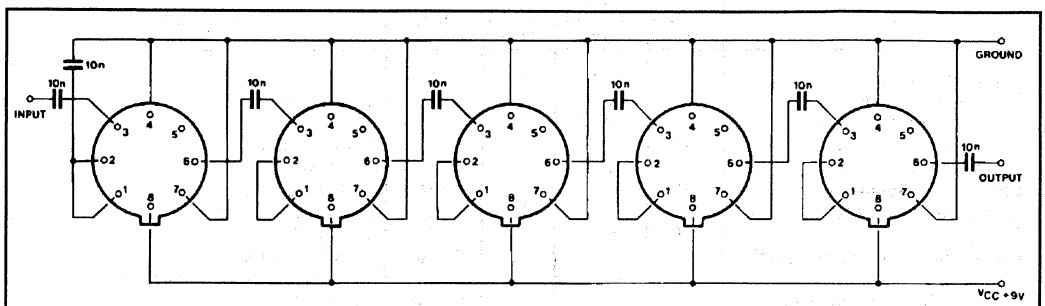


Fig.5 Phase change with input level

TYPICAL APPLICATION

Five stage strip

Input signal for full limiting	300μV rms -57dBm
Limited output	1V p-p
Phase shift (V_{IN} - 57 → +10dBm)	±3°typ.



The recommended output buffer amplifier to drive 50Ω loads is the SL560C

Fig.6 Five stage IF strip

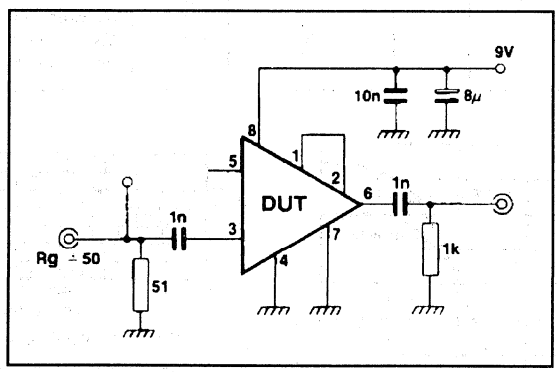


Fig.7 SL532 test circuit

SL541

HIGH SLEW RATE OPERATIONAL AMPLIFIER

The SL541 is a monolitic amplifier designed for optimum pulse response and applications requiring high slew rate with fast setting time to high accuracy. The high open loop gain is stable with temperature, allowing the desired closed loop gain to be achieved using standard operational amplifier techniques. The device has been designed for optimum response at a gain of 20dB when no compensation is required. The SL541B has a guaranteed input offset voltage of ±5mV maximum and replaces the SL541C.

FEATURES

- High Slew Rate 175V/μs
- Fast Setting Time 1% in 50ns
- Open Loop Gain 70dB (SL541B)
- Wide Bandwidth DC to 100MHz at 10dB Gain
- Very Low Thermal Drift 0.02dB/°C Temperature Coefficient of Gain
- Guaranteed 5mV input offset maximum

APPLICATIONS

- Wideband IF Amplification
- Wideband Video Amplifiaction
- Fast setting Pulse Amplifiers
- High Speed Integrators
- D/A and A/D Conversion
- Fast Multiplier Preamps

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V+to V–)		24V
Input voltage(Inv. I/P to non inv. I/P)		±9V
Storage temperature–55°C to +150°C		
Chip operating temperature		+150°C
Thermal resistances		
Chip to ambient	TO–5	220°C/W
	DIL	125°C/W
Chip to case	TO–5	65°C/W
	DIL	40°C/W

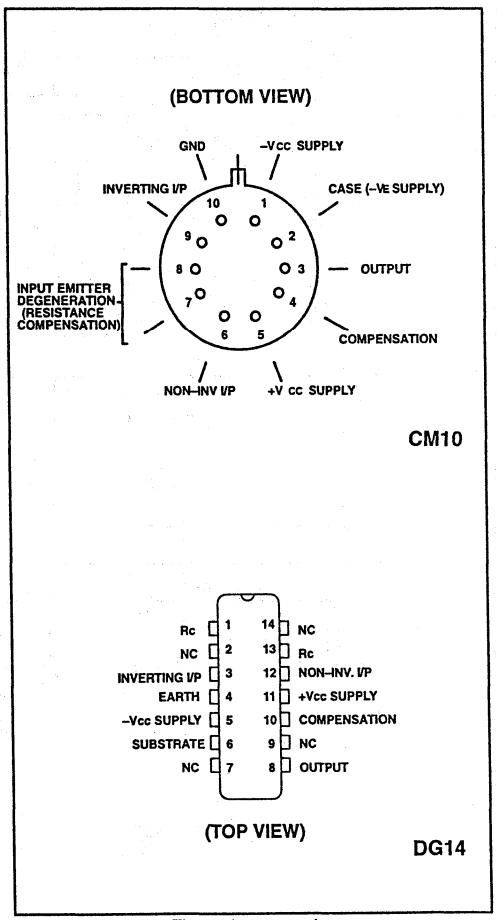


Fig. 1 pin connections

ORDERING INFORMATION

SL541 B CM
SL541 B DG
SL541 NA IC (NAKED DIE)

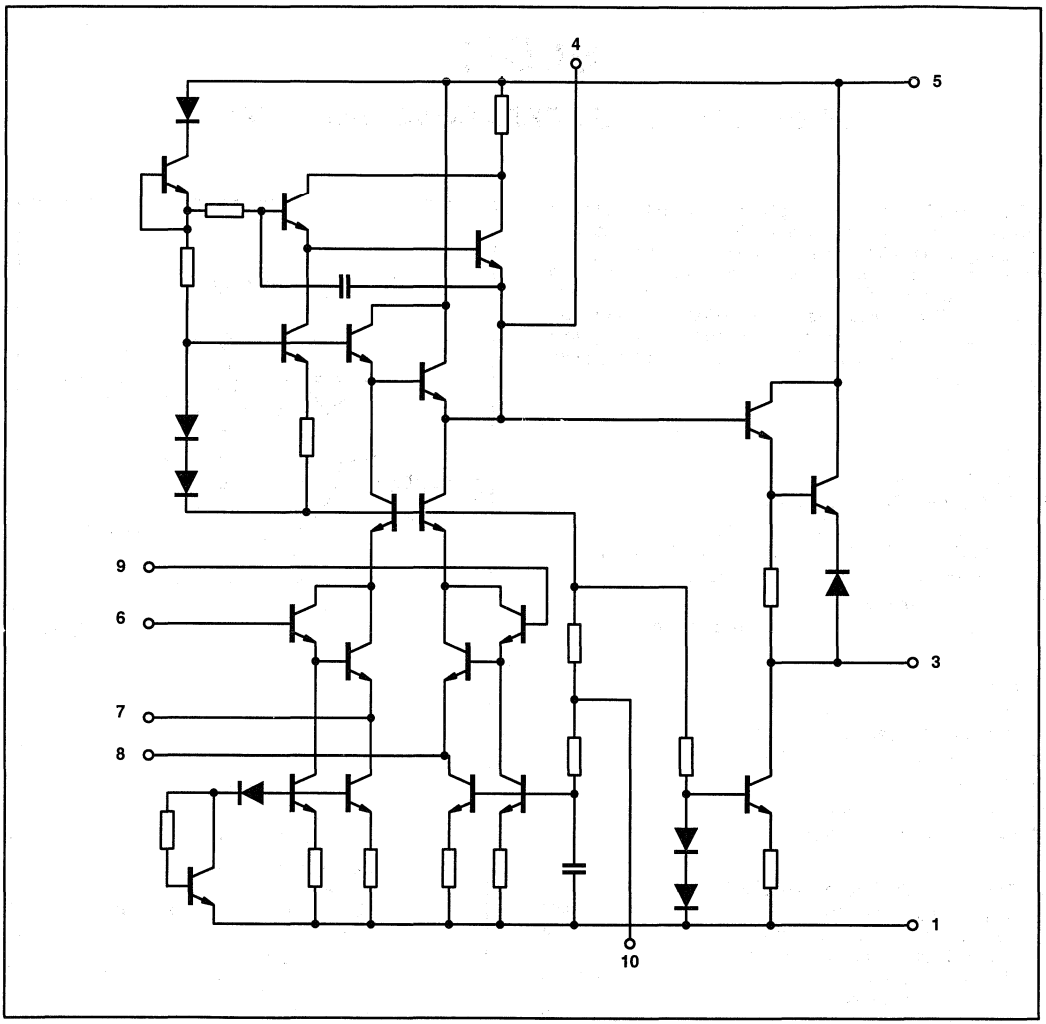


Fig. 2 SL541 circuit diagram (TO–5 pin nos)

ELECTRICAL CHARACTERISTICS

T_{amb}= 22°C ±2°C, Rc=0Ω. These characteristics are guaranteed over the following conditions. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Circuit	Value			Units	Conditions
		Min	Typ	Max		
Static nominal supply current	A, B		16	21	mA	
Input bias current	A, B		7	25	µA	
Input offset voltage	B			5	mV	
Input offset voltage	A			10	mV	
Dynamic open loop gain	A	45	54		dB	600Ω load
	B	60	71		dB	
Open loop temperature coefficient	A, B		–0.02		dB/°C	
Closed loop bandwidth (–3dB)	A, B		100		MHz	X10 gain
Slew rate (4V peak)	A, B	100	175		V/µs	X10 gain
Setting time to 1%	A, B		50	100	ns	
Maximum output voltage						
(+ve)	A	5.5	5.7		V	
(–ve)	A		–1.9	–1.5	V	
(+ve)	B	2.5	3.0		V	
(–ve)	B		–3.0	–2.5	V	
Maximum output current	A, B	4	6.5		mA	
Maximum input voltage						
(+ve)	A			5	V	
(–ve)	A	–1			V	Non–inverting
(+ve)	B			3	V	Modes
(–ve)	B	–3			V	
Supply line rejection						
(+ve)	A, B	54	66		dB	
(–ve)	A, B	46	54		dB	
Input offset current	A, B			9.85	µA	
Common mode rejection	A, B	60.7			dB	
Input offset voltage drift	A		25		µV/°C	

ELECTRICAL CHARACTERISTICS (Typical)

T_{amb}= –40°C to 85°C, Rc=0Ω. Test circuit B These characteristics are guaranteed over the following conditions. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Value			Units	Conditions
	Min	Typ	Max		
Static nominal supply current		16	25	mA	
Input bias current			35	μA	
Input offset voltage (+ve)			8	mV	
(–ve)	–8			mV	
Maximum output current	3.5	6.5		mA	
Maximum input voltage (+ve)			3	V	Non–inverting modes
(–ve)	–3			V	
Supply line rejection (+ve)	50			dB	
(–ve)	42			dB	
Maximum output voltage (+ve)	2.3			V	
(–ve)			2.5	V	
Common mode rejection	55			dB	
Input offset current			16	μA	
Output voltage drift		15		μV/°C	
Input bias current drift		60		nA/°C	
Output current drift		40		nA/°C	

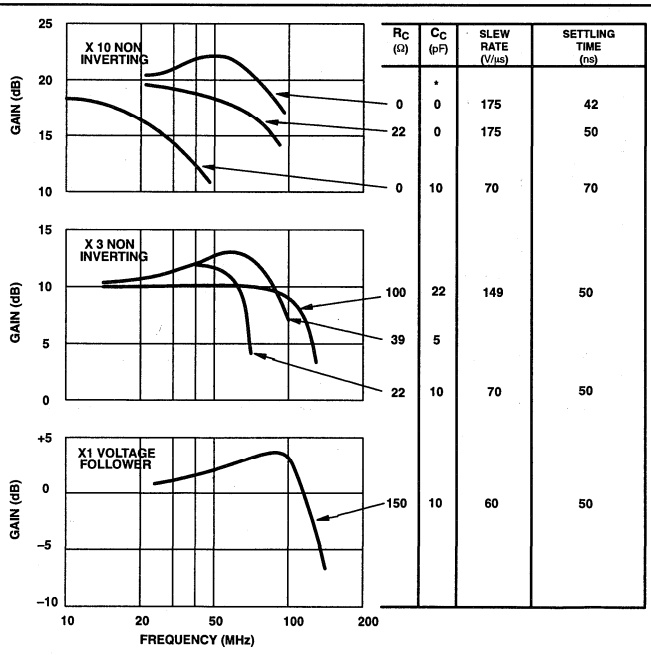


*Fig. 3 Performance graphs – gain v. frequency (load=2kΩ/10pF) *See operating note 2*

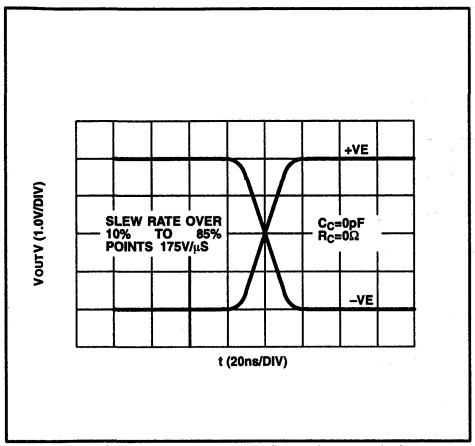


Fig. 4. Slew rate –X10 non inverting mode input square wave 0.4V p/p

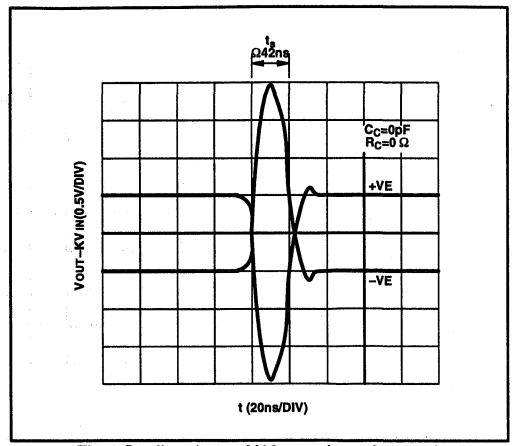


Fig.5 Settling time – X10 non–inverting mode

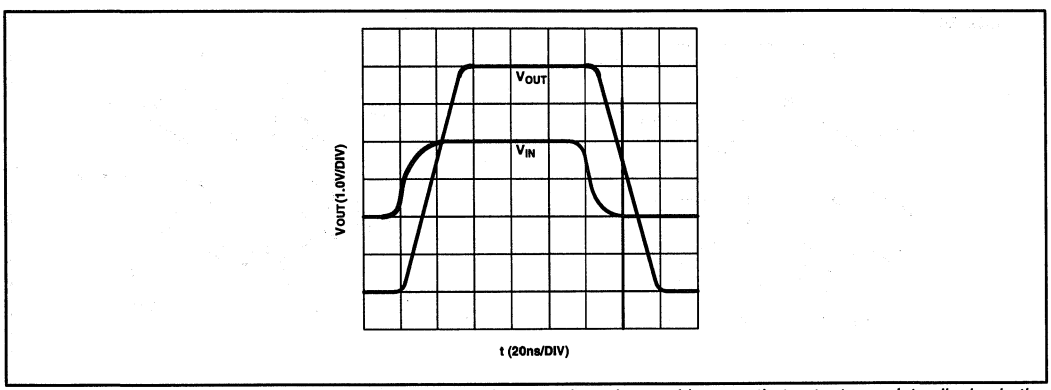


Fig.6 Output clipping levels – X10 non – inverting mode input moderately overdriven, so that output goes into clipping both sides.

OPERATING NOTES

The SL541 may be used as a normal, but non saturating operational amplifier, in any of the usual configurations (amplifiers, integrators etc.), provided that the following points are observed:

1. Positive supply line decoupling back to the output load earth should always be provided close to the device terminals.

2. Compensation capacitors should be connected between pins 4 and 5. These may have any value greater than that necessary for stability without causing side offsets.

3. The circuit is generally intended to be fed from a fairly low impedance (<1kΩ), as seen from pins 6 and 9–100Ω or less results in optimum speed.

4. The circuit is designed to withstand a certain degree of capacitive loading (up to 20pF) with virtually no effect. However, very high capacitive loads will cause loss of speed due to the extra compensation required and asymmetric output slew rates.

5. Pin 10 does not need to be connected to zero volts except where the clipping levels need to be defined accurately w.r.t. zero. If disconnected, an extra ±0.5 volt uncertainty inthe clipping levels results, but the separation remains. However, the supply line rejection is improved if pin 10 can be left open–circuit (circuit B only).

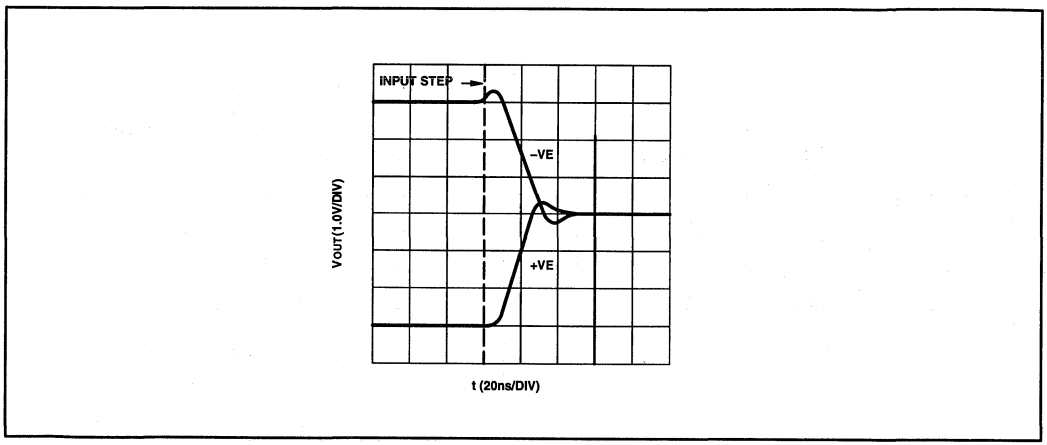


Fig. 7 Output clippings level – X10 non–inverting mode. Output goes from clipping to zero volts. V_{IN}=3V peak step, offset +ve or –ve.

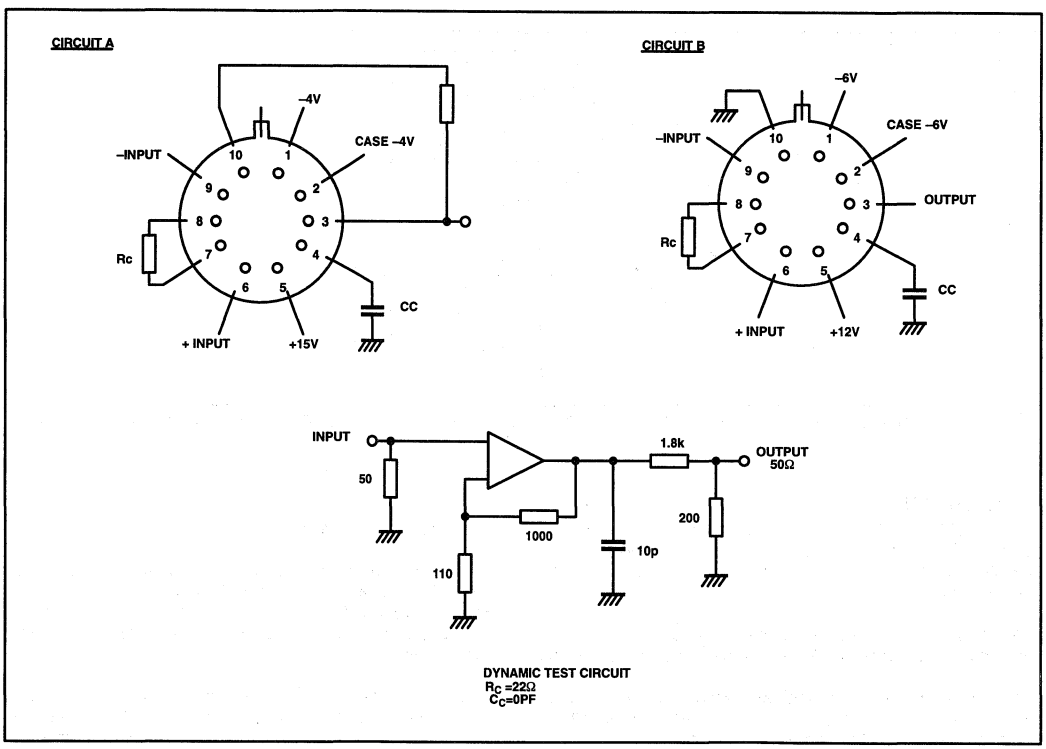


Fig. 8 Test circuit

TEST CONDITIONS AND DEFINITIONS

Both slew rate and settling time are measures of an amplifier's speed of response to an input. Slew rate is an inherent characteristic of the amplifier and is generally less subject to misinterpretation than is settling time, which is often more dependant upon the test circuit than the amplifier's ability to perform.

Slew rate defines the maximum rate of change of output voltage for a large step input change and is related to the full power frequency response (fp) by the relationship.

$$S = 2\pi f_p E_o$$

where E_o is the peak output voltage

Settling time is defined as the time elapsed from the application of a fast input step to the time when the amplifier output has entered and remained within a specified error band that is symmetrical about the final value. Settling time, therefore, is comprised of an initial propagation delay, an additional time for the amplifier to slew to the vincinity of some value of the output voltage, plus a period to recover from overload and settle within the given error band.

The SL541 is tested for slew rate in a X10 gain configuration.

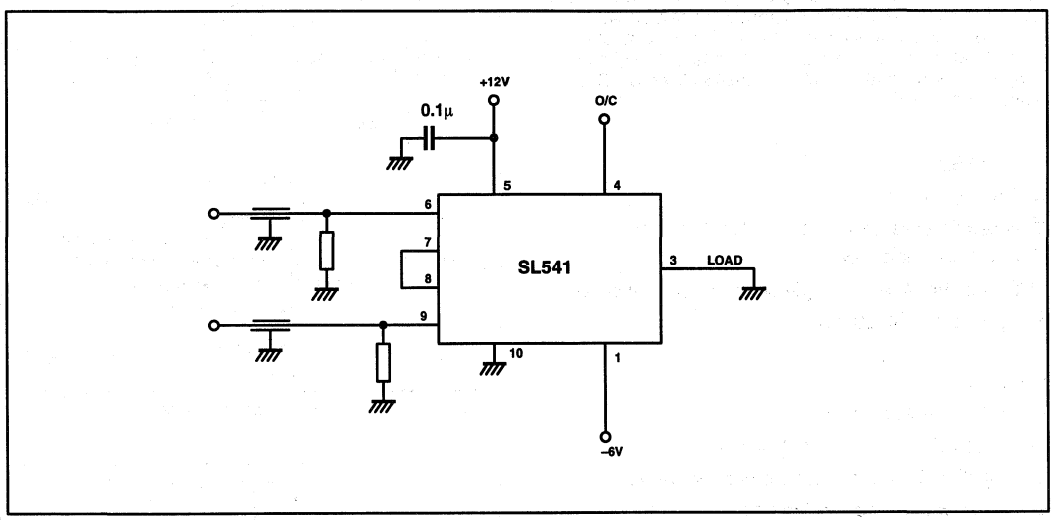


Fig. 9 Non saturating sense amplifier (30V/µs for 5mV).
Note: the output may be caught at a pre determined level. (T0–5 pin nos.)

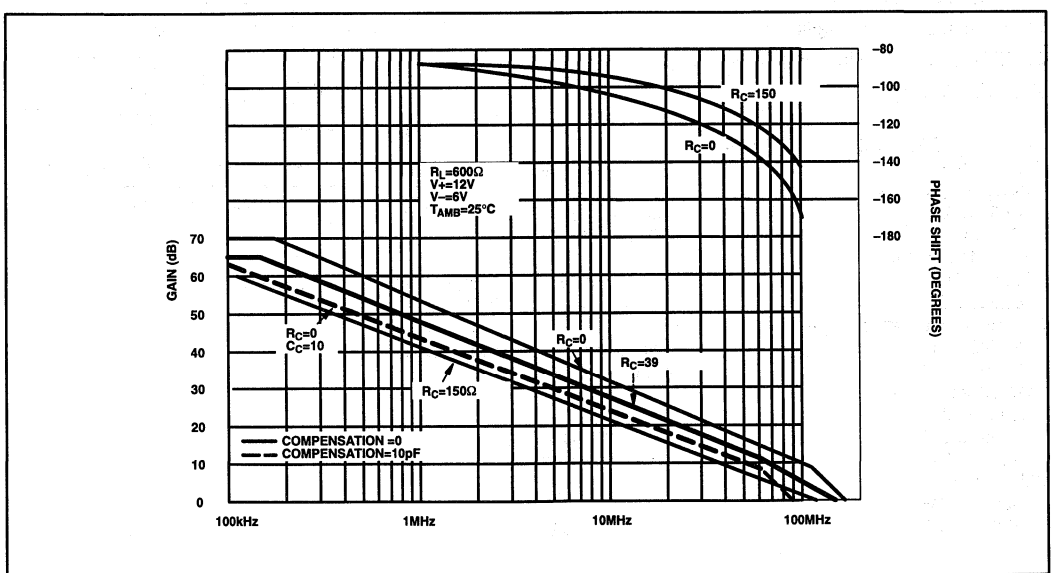


Fig. 10 SL541B open loop gain and phase shift v. frequency

SL560

300MHz LOW NOISE AMPLIFIER

This monolithic circuit contains three very high performance transistors and associated biasing components in an eight-lead TO-5 package forming a 300MHz low noise amplifier. The configuration employed permits maximum flexibility with minimum use of external components. The SL560C is a general purpose low noise, high frequency gain block.

The device is also available as the SL560AC which has guaranteed operation over the fully Military Temperatures Range and is screened to MIL-STD-883 Class B. Data is available separately.

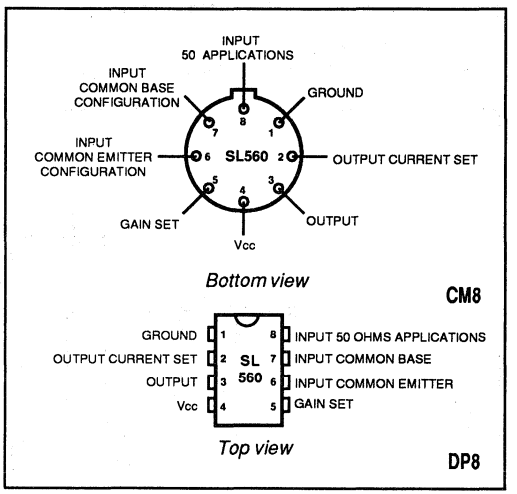


Fig.1 Pin connections

FEATURES

- Gain up to 40dB
- Noise Figures less than 2dB (Rs 200 ohm)
- Bandwidth 300MHz
- Supply Voltage 2-15V (Depending on Configuration)
- Low Power Consumption

APPLICATIONS

- Radar IF Preamplifiers
- Infra-Red Sysems Head Amplifiers
- Amplifiers in Noise Measurement Systems
- Low Power Wideband Amplifiers
- Instrumentation Preamplifiers
- 50 ohm Line Drivers
- Wideband Power Amplifiers
- Wideband Dynamic Range IF Amplifiers
- Aerial Preamplifiers

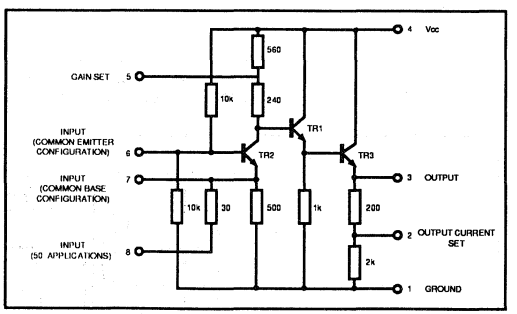


Fig.2 SL560C circuit diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage	+15V
Storage temperature	
SL560C DP	-55°C to +150°C
SL560C CM	-65°C to +150°C
Junction temperature	
SL560C DP	+150°C
SL560C CM	+175°C
Operating temperature range	
SL560C DP	-30°C to +85°C
SL560C CM	-55°C to +125°C
Thermal resistance	
Chip-to-ambient	
SL560C CM	225°C/W
SL560C DP	111°C/W
Chip-to-case	
SL560C CM	65°C/W
SL560C DP	71°C/W

ORDERING INFORMATION

SL560 C CM
SL560 C DP
5962-90520 (SMD)

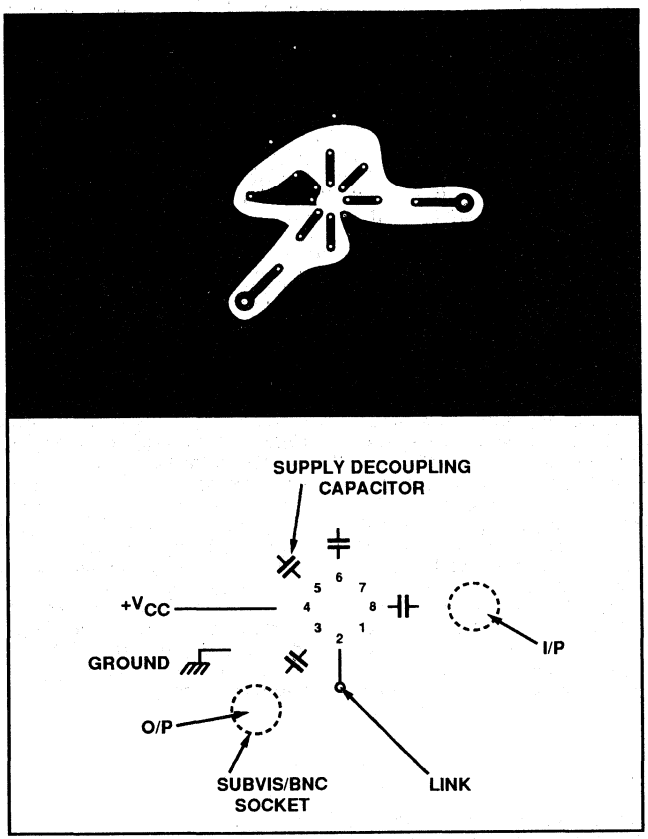


Fig.3 PC layout for 50Ω line driver (see Fig.6)

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated)

Frequency = 30MHz; V_{CC}=6V; $R_S = R_L$ =50Ω; T_{AMB}=22°C ± 2°C; Test Circuit: Fig.6

Characteristic	Min.	Typ.	Max.	Units	Conditions
Small signal voltage gain	11	14	17	dB	
Gain flatness		±1.5		dB	10MHz - 220MHz
Upper cut-off frequency		250		MHz	
Output swing	+5	+7		dBm	V_{CC}6V
		+11		dBm	V_{CC} = 9V
Noise figure (common emitter)		1.8		dB	R_S = 200Ω
		3.5		dB	R_S = 50Ω
Supply current		20	30	mA	

CIRCUIT DESCRIPTION

Three high performance transistors of identical geometry are employed. Advanced design and processing techniques enable these devices to combine a low base resistance (Rbb') of 17Ω (for low noise operation) with a small physical size - giving a transition frequency, f_T, in excess of 1GHz.

The input transistor (TR1) is normally operating in common base, giving a well defined low input impedance. The full voltage gain is produced by this transistor and the output voltage produced at its collector buffered by the two emitter followers (TR2 and TR3). To obtain maximum bandwidth the capacitance at the collector of TR1 must be minimised. Hence, to avoid bonding pad and can capacitances, this point is not brought out of the package. The collector load resistance of TR1 is split, the tapping being accessible via pin 5. If required, an external roll-off capacitor can be fixed to this point.

The large number of circuit nodes accessible from the outside of the packages affords great flexibility, enabling the operating current and circuit configuration to be optimised for any application. In particular, the input transistor (TR1) can be operated in common emitter mode by decoupling pin 7 and using 6 as the input. In this configuration, a 2dB noise figure (R_S = 200Ω) can be achieved. This configuration can give a gain of 35dB with a bandwidth of 300MHz (see figs. 10 and 11).

Because the transistors used in the SL560C exhibit a high value of f_T, care must be taken to avoid high frequency instability. Capacitors of small physical size should be used, the leads of which must be short as possible to avoid oscillation brought about by stray inductance. The use of a ground plane is recommended.

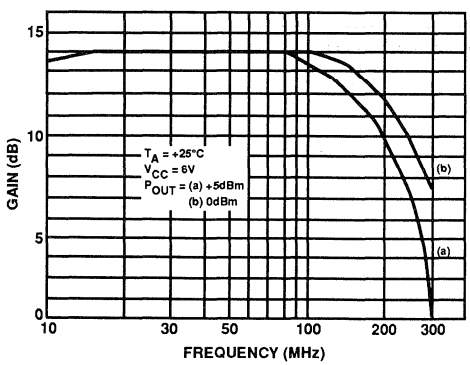


Fig.4 Frequency response, small signal gain is of a typical device

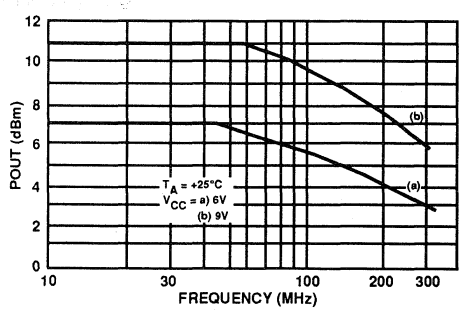


Fig.5. Frequency response, output capability (loci of maximum output power with frequency for 1dB gain compression (typical)

TYPICAL APPLICATIONS

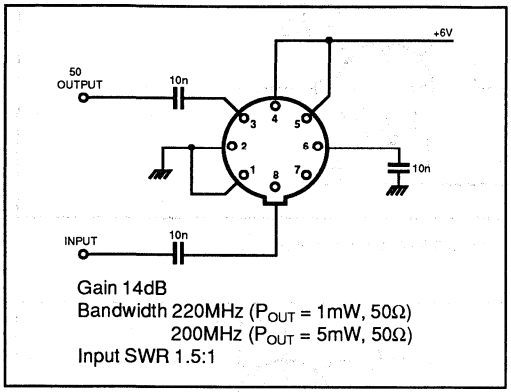


Fig.6 50Ω lin driver. The response of this configuration is shown in Fig.4

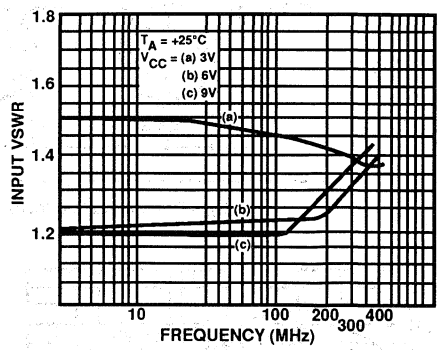


Fig.7 Input standing wave ratio plot of circuit shown in Fig.6 (typical)

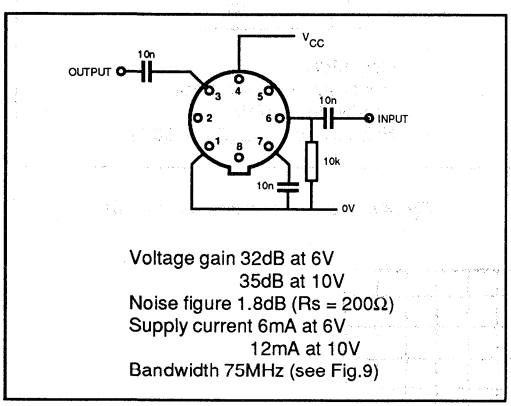


Fig.8 Low Noise preamplifier

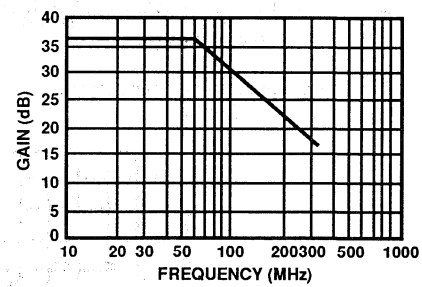


Fig.9 Frequency response of circuit shown in Fig.8 (typical)

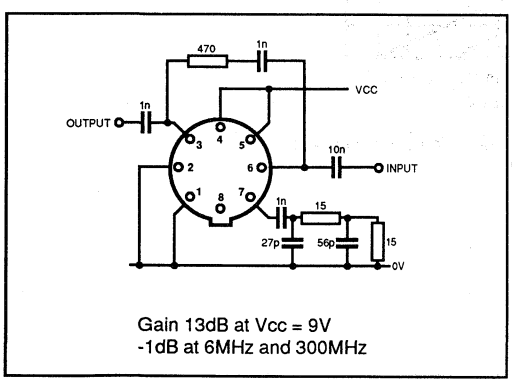


Fig.10 Wide bandwidth amplifier

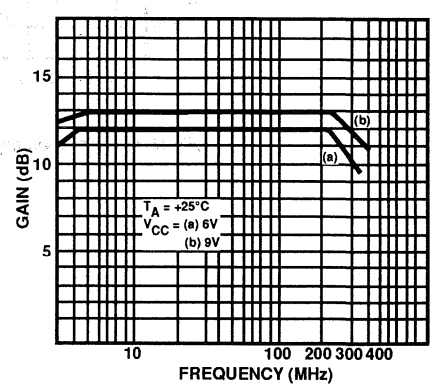


Fig.11 Frequency response of circuit shown in Fig.10 (typical)

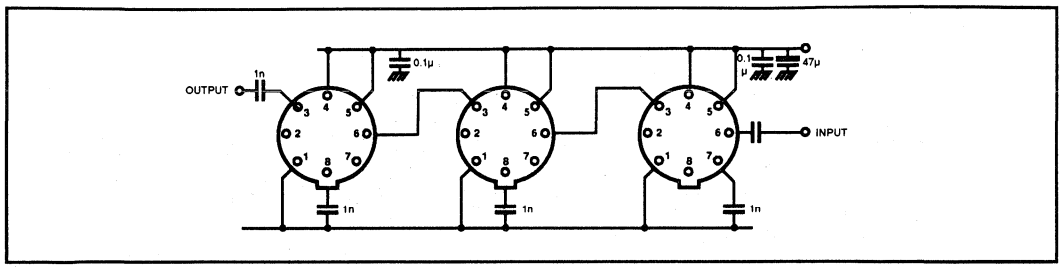


Fig.12 Three-stage directly-coupled high gain low noise amplifier

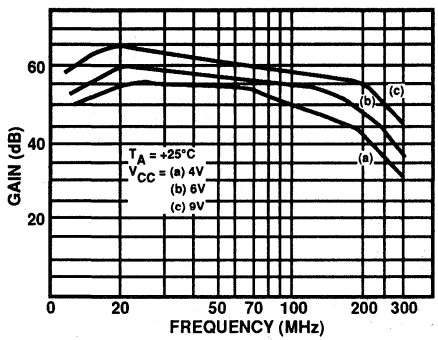


Fig.13 Frequency response of circuit shown in Fig.12 (typical)

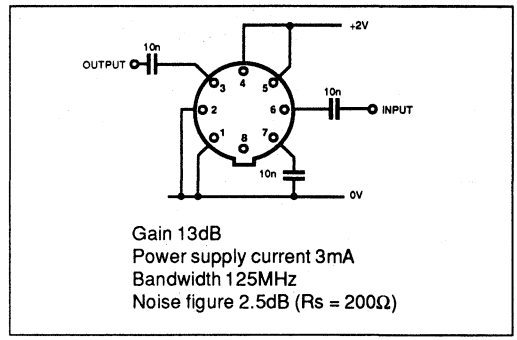


Fig.14 Low power consumption amplifier

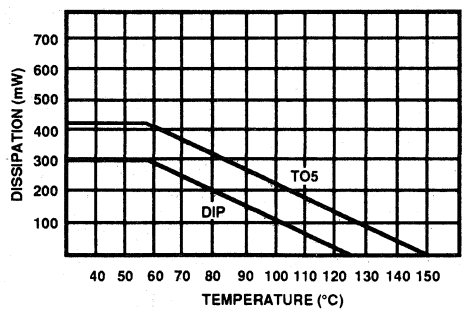


Fig.15 Ambient operating temperature V. degrees centigrade (typical)

SL561

ULTRA LOW NOISE PREAMPLIFIERS

This integrated circuit is a high gain, low noise preamplifier designed for use in audio and video systems at frequencies up to 6MHz. Operation at low frequencies is eased by the small size of the external components and the low 1/f noise. Noise performance is optimised for source impedances between 20Ω and 1 kΩ making the device suitable for use with a number of transducers including photo-conductive IR detectors, magnetic tape heads and dynamic microphones.

The SL561 B is only available in the TO-5 package

The SL561 C is only available in the Plastic package.

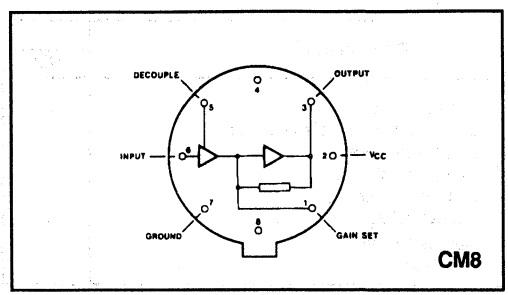


Fig.1 Pin connections (view as above) SL561B

FEATURES

- High Gain 60dB
- Low Noise 0.8nV/√Hz (Rs = 50Ω)
- Bandwidth 6MHz
- Low Power Consumption 10mW (V_{CC} = 5V)

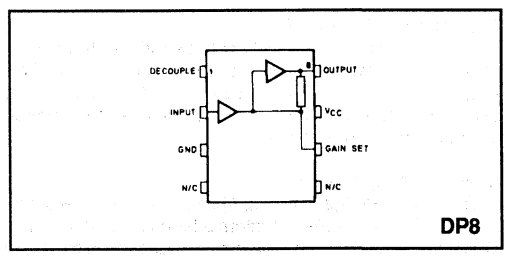


Fig.2 Pin connections (view as above) SL561C

APPLICATIONS

- Audio Preamplifiers (low noise from low impedance source)
- Video Preamplifier
- Preamplifier for use in Low Cost Infra-Red Systems

ORDERING INFORMATION

SL561 AC CM
SL561 C DP

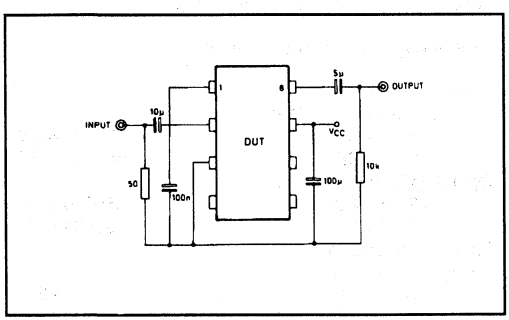


Fig.3 Test circuit

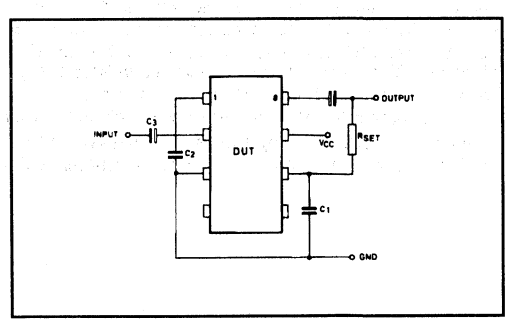


Fig.4 Typical application

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated):

V_{cc}	5V
Source impedance	50Ω
Load impedance	10kΩ
T_{amb}	25°C

SL561C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Voltage gain	57	60	63	dB	Pin 6 O/C
Equivalent input noise voltage		0.8		nV/√Hz	100Hz to 6MHz
Input resistance		3		kΩ	
Input capacitance		15		pF	
Output impedance		50		Ω	
Output voltage	2	3		V p-p	See note
Supply current		2	3	mA	
Bandwidth		6		MHz	

OPERATING NOTES (Pin numbers refer to DIL package)

Upper cut-ott frequency

The bandwidth of the amplifier can be reduced from 6MHz to any desired value by a capacitor from pin 6 to ground. This is shown in Fig.5. No degradation in noise or output swing occurs when this capacitor is used. The high frequency roll off is approximately 6dB/octave.

Low frequency response

The capacitors C_2 and C_3 (Fig.4) determine the lower cut-off frequency C_2 decouples an internal feedback loop and if its value is close to that of C_3 an increase in gain at low frequencies can occur. For a flat response either make C_2 less than 0.05 C_3 or make C_2 greater than 5 C_3.

Gain set facility

Provision is made to adjust the gain by means of a resistor between pin 6 and the output. Gains as low as 10dB can be selected. This resistor increases the feedback around the output stage and stability problems can result if the bandwidth of the amplifier is not reduced as indicated in Note 1. Fig.6 shows recommended values of C_1 for each gain range. Since the input stage is a common emitter stage without emitter degeneration (for best noise) at values of gain less than 40dB this input stage, rather than the output stage, determines the maximum output voltage swing. For a distortion of less than 10% the input voltage should be restricted to less than 5mV (see Fig.9).

Driving low impedance loads

The quiescent current of the output emitter follower is 0.5mA. If larger voltage swings are required into low impedance loads this current can be increased by a resistor from pin 8 to ground. To avoid exceeding the ratings of the output transistor the resistor should not be less than 200Ω.

Noise performance

The equivalent input voltage for the amplifier is shown in Fig.7. From this the input noise voltage and current generators can be derived. They are:

$$e_n = 0.8nV/\sqrt{Hz}$$
$$i_n = 2.0pA/\sqrt{Hz}$$

Flicker or 1/f noise is not normally a problem, the knee frequency being typically below 100Hz.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+10V
Storage Temperature Range	
SL561 CM	-65°C to +150°C
SL561 DP	-55°C to +150°C
Operating Temperature Range	
SL561 AC	-55°C to +125°C
SL561 C	-30°C to +85°C
Thermal Resistance	
Chip - to - Ambient	
SL561 CM	225°C/W
SL561 DP	111°C/W
Chip - to - case	
SL561 CM	65°C/W
SL561 DP	71°C/W

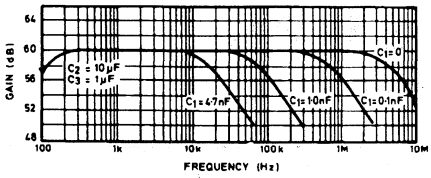


Fig.5 Gain v. frequency

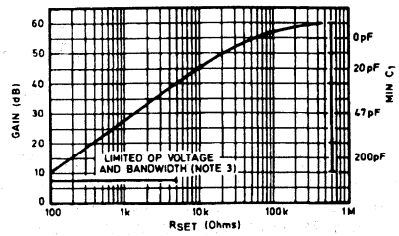


Fig.6 Gain v. R_{set}

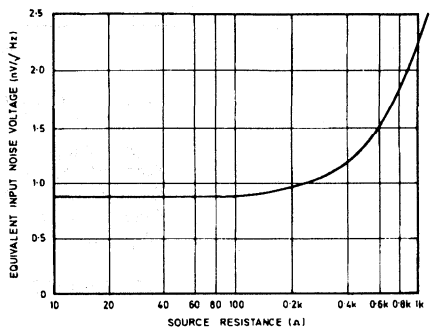


Fig.7 Noise v. source impedance

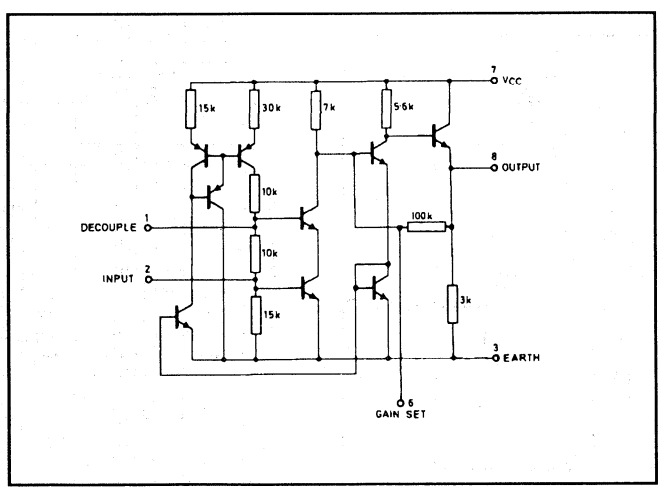


Fig.8 Circuit diagram

SL610, SL611 & SL612

RF/IF AMPLIFIER

The SL610C, SL611C and SL612C are RF voltage amplifier with AGC facilities. The voltage gain is 10, 20 and 50 times respectively and the upper frequency response varies from 15MHz to 120MHz according to type .

FEATURES

- Wide AGC Range: 50dB
- Easy Interfacing
- Integral Power Supply RF Decoupling

APPLICATIONS

- RF Amplifiers
- IF Amplifiers

QUICK REFERENCE DATA

- Supply Voltage: 6V
- Voltage Gain: 20dB to 34dB

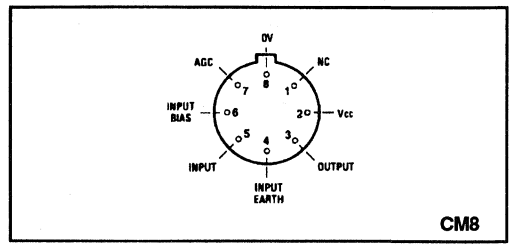


Fig.1 Pin connections (top view)

ABSOLUTE MAXIMUM RATINGS

Supply voltage:	12V
Storage temperature:	-65°C to +150°C
Operating temperature range	-30°C to +85°C
Chip-to-ambient	225°C/W
Chip-to-case	65°C/W

ORDERING INFORMATION

SL610/1/2 C CM
SL610 NA 1C
SL612 NA 1C

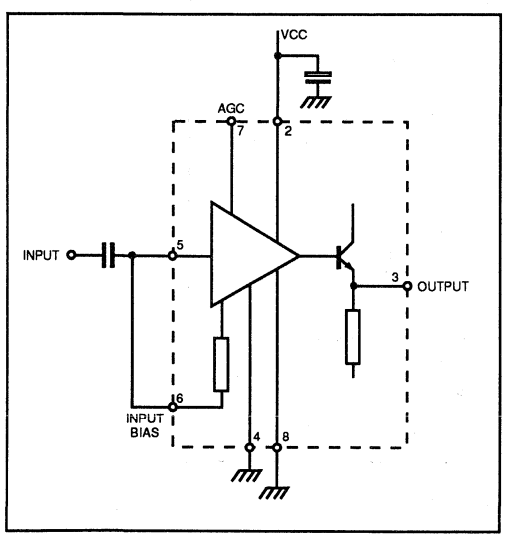


Fig.2 Block diagram

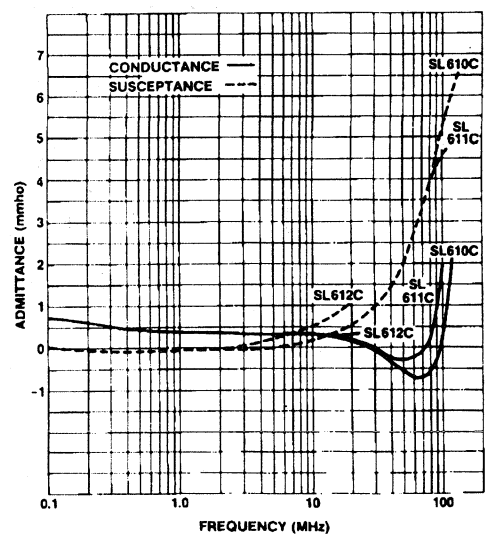


Fig.3 Input admittance with o/c output (G_{11})

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated)

Supply voltage VCC: 6V
Ambient temperature: 22°C ± 2°C
Test frequency: SL610C 30MHz
SL611C 30MHz
SL612C 1.75MHz

Characteristics	Circuit	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	SL610C		15	20	mA	
	SL611C		15	20	mA	No signal, Pin 3 open circuit
	SL612C		3.3	5	mA	
Voltage gain	SL610C	18	20	22	dB	R_S = 50Ω
	SL611C	24	26	28	dB	R_L = 22°C
	SL612C	32	34	36	dB	T_{amb} = 22°C
Cut-off frequency (-3dB)	SL610C	85	120		MHz	
	SL611C	50	80		MHz	
	SL612C	10	15		MHz	
Max. output signal (max. AGC)			1.0		V rms	RL = 150Ω (SL610C/611C) RL = 1.2kΩ (SL612C)
Max.input signal (max. AGC)						
AGC range			250		mV rms	
	SL610C	40	50		dB	
	SL611C	40	50		dB	Pin 7 0V to 5.1V
	SL612C	60	70		dB	
AGC current			0.15	0.6	mA	Current into pin 7 at 5.1V

APPLICATION NOTES

Input circuit

The SL610C, SL611C and SL612C are normally used with pins 5 and 6 connected together and with the input connected via a capacitor as shown in Fig.2.

The input impedance is negative between 30MHz and 100MHz (SL610C, SL611C only) and is shown in Fig.3. The source and inductive is should be shunted by a 1kΩ resistor to prevent oscillation.

An alternative circuit with improved noise figure is shown in Fig.4.

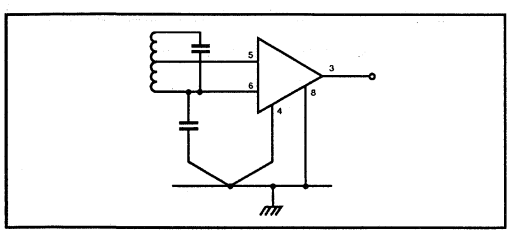


Fig.4 Alternative input circuit

Output circuit

The output stage is an emitter follower and has a negative output impedance at certain frequencies as shown in Fig.5.

To prevent oscillation when the load is capacitive a 47Ω resistor should be conncted in series with the output.

AGC

When pin 7 is open circuit or connected to a voltage less than 2V the voltage gain is normal. As the AGC voltage is increased there is a reduction in gain as shown in Fig.6. This reduction varies with temperature.

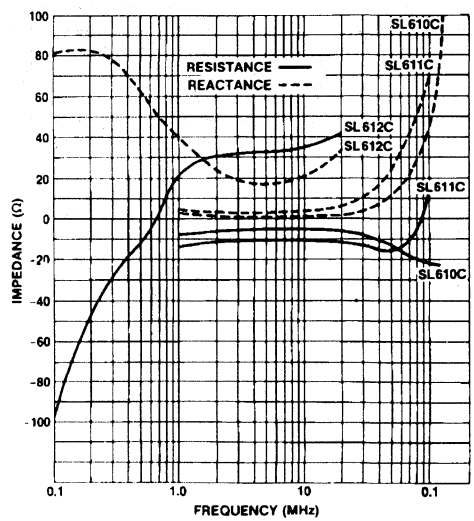


Fig.5 Typical output impedance with s/c input (G22)

Typical applications

The circuit of Fig.7 is a general purpose RF preamplifier. The voltage gain (from pin 5 to pin 3) is shown in Fig.8. Fig.9 is the IF section of a simple SSB transceiver. At 9MHz it has a gain of 100dB.

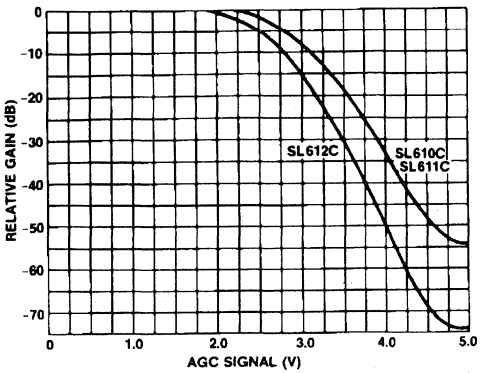


Fig.6 AGC characteristics (typical)

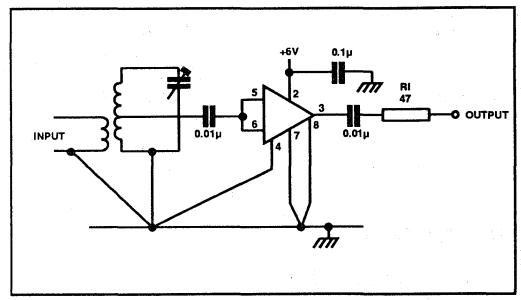


Fig.7 RF preamplifier

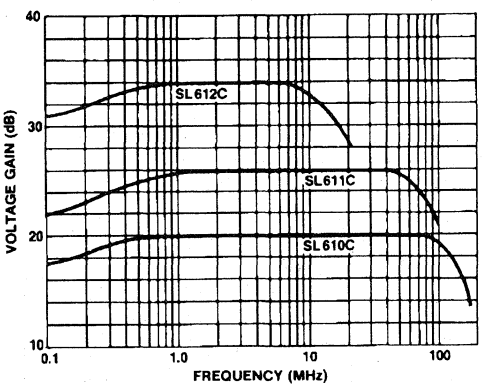


Fig.8 Typical voltage gain (RS = 50Ω)

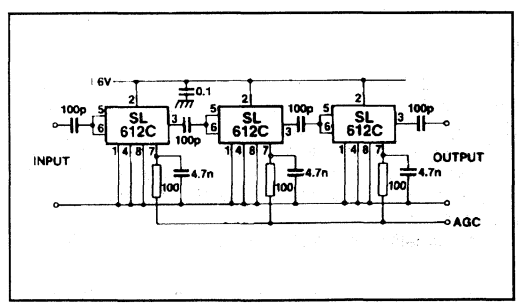


Fig.9 IF amplifier using SL1612

SL1613

WIDEBAND LOG IF STRIP AMPLIFIER

The SL1613 is a bipolar monolithic integrated circuit wideband amplifier intended for use in successive detection logarithmic IF strips, operating at centre frequencies between 10MHz and 60MHz. The device provides amplification, limiting and rectification, is suitable for direct coupling and incorporates supply line decoupling. The mid-band voltage gain of the SL1613 is typically 12dB.

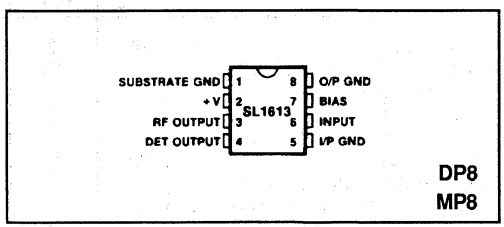


Fig.1 Pin connections (top)

FEATURES

- Well Defined Gain
- 4.5dB Noise Figure
- High I/P impedance
- Low O/P impedance
- 150MHz Bandwidth
- On-Chip Supply Decoupling
- Low External Component Count

APPLICATIONS

- Logarithmic IF Strips with Gains up to 108dB and Linearity Better than 2dB
- Low Cost Radar
- Radio Telephone Filed Strength Meters

ABSOLUTE MAXIMUM RATINGS

Storage temperature range	-55°C to +150°C
Operating temperature range	-30°C to +85°C
Thermal resistance	
Chip-to-ambient	
SL1613 DP	111°C/W
SL1613 MP	163°C/W
Chip-to-case	
SL1613 DP	71°C/W
SL1613MP	57°C/W
Maximum instantaneous voltage at video output	+12V
Supply voltage	9V

ORDERING INFORMATION

SL1613 C DP
SL1613 C MP

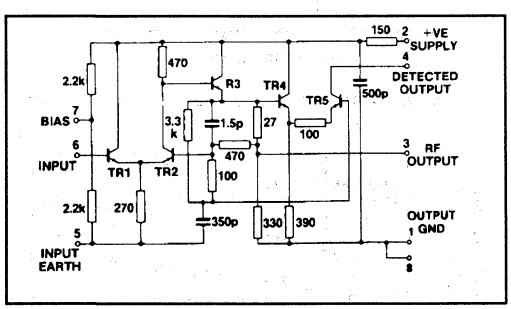


Fig.2 Circuit diagram

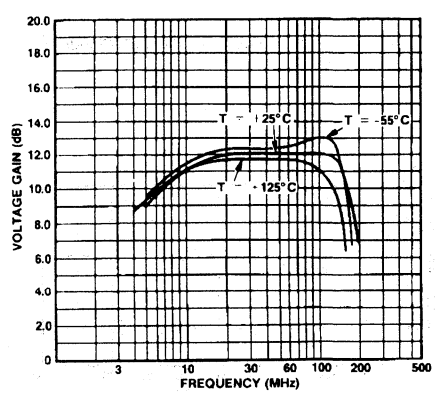


Fig.3 Voltage gain v. frequency

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following condiotns (unless otherwise stated)

TA = +22°C ±2°C
Supply voltage = +6V
DC connection between input and bias pins

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Voltage gain	10	12	14	dB	f = 30MHz, R_S = 10Ω, C_L = 8pF
Upper cut-off frequency (Fig. 3)		150		MHz	R_S = 10Ω, C_L = 8pF
Lower cut-off frequency (Fig. 3)		5		MHz	R_S = 10Ω, C_L = 8pF
Propagation delay		2		ns	
Max. rectified video output current (Fig. 4 and 5)	0.8	1	1.4	mA	f = 60MHz, V_{IN} = 500mV rms
Variation of gain supply voltage		0.7		dB/V	
Variation of maximum rectified output current with supply voltage		25		%/V	
Maximum input signal before overload		1.9		V rms	See Note 1
Noise figure (Fig. 6)		4.5		dB	f = 60MHz, R_S = 450Ω
Maximum RF output voltage		1.2		Vp-p	
Supply current		1.5	20	mA	

Note 1. Overload occurs when the input signal reaches a level sufficent to forward bias the base-collector junction of TR1 on peaks

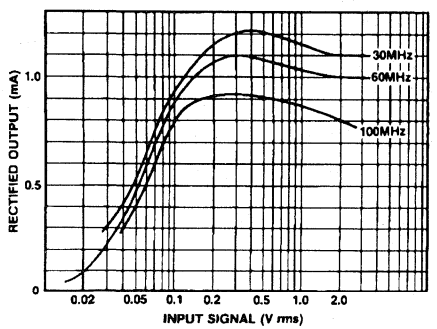


Fig.4 Rectified output current v. input signal

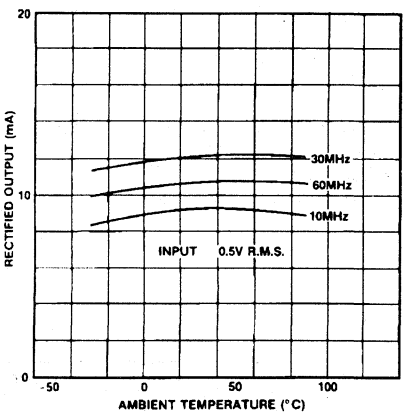


Fig.5 Maximum rectified output current v. temperature

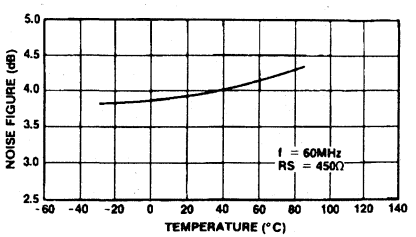


Fig.6 Typical figure v. temperature

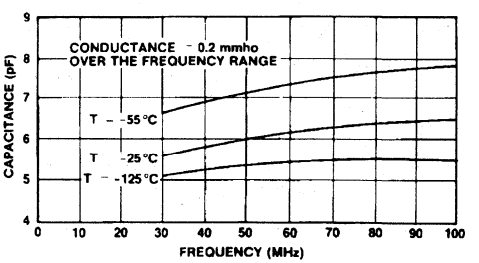


Fig.7 Input admittance with open circuit output

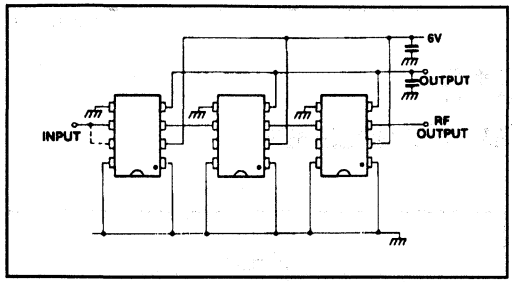


Fig.8 Direct coupled amplifiers

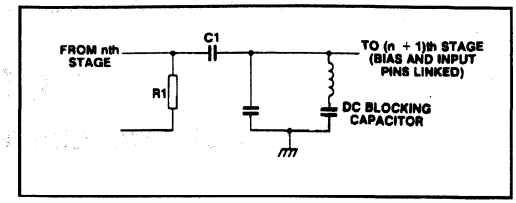


Fig.9 Suitable interstage tuned circuit

OPERATING NOTES

The amplifiers are intended for use directly coupled, as shown in Fig. 8.

The seventh stage in an untuned cascade will be giving virtually full output on noise.

Noise may be reduced by inserting a single tuned circuit in the chain. As there is a large mismatch between stages a simple parallel or series circuit cannot be used. This choice of network is also controlled by the need to avoid distorting the logarithmic law: the network must give unity voltage transfer at resonance. A suitable network is shown in Fig. 9. The value of C1 must be chosen so that at resonance its admittance equals the total loss conductance across the tuned circuit. Resistor R1 may be introduced to improve the symmetry of filter response, providing other values are adjusted for unity gain at resonance.

A single capacitor may not be suitable for decoupling the output line if many stages and fast rise times are required. Values of supply line decoupling capacitor required for untuned cascades are given below. Smaller values can be used in high frequency tuned cascades.

The amplifiers have been provided with two ground leads to avoid the introduction of common ground lead inductance between input and output circuits. The equipment designer should take care to avoid the subsequent introduction of such inductance.

	Number of stages			
	6 or more	5	4	3
Minimum capacitance	30nF	10nF	3nF	InF

The on-chip 500pF supply decoupling capacitor has a resistance of, typically 10Ω. It is a junction type having a low breakdown voltage and consequently the positive supply current will increase rapidly if the supply voltage exceeds 7.5V. (See Absolute Maximum Ratings).

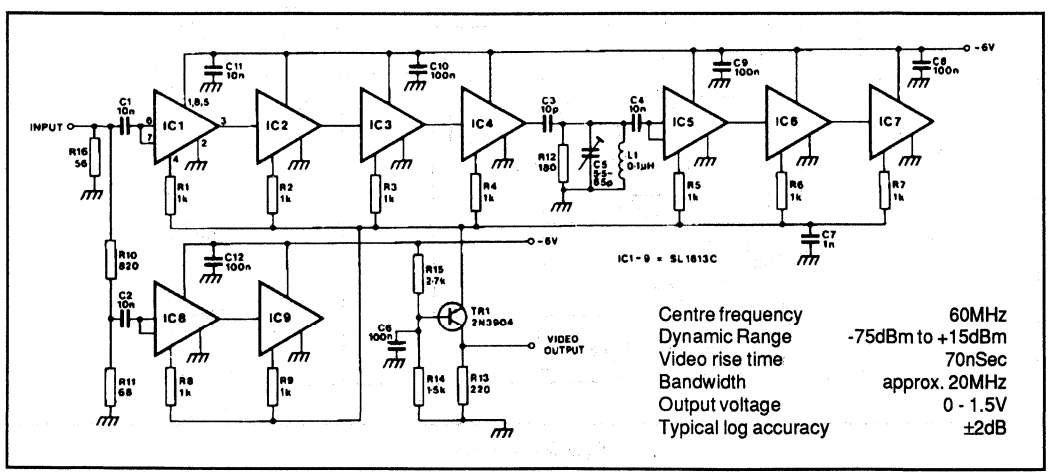


Fig.10 Circuit diagram of low strip

SL1615

WIDEBAND LOG IF STRIP AMPLIFIER

The SL1615 is a bipolar monolithic integrated circuit wideband amplifier intended for use in successive detection logarithmic IF strips, operating at centre frequencies between 10MHz and 60MHz. The device provides amplification, limiting and rectification, is suitable for direct coupling and incorporates supply line decoupling. The mid-band voltage gain of the SL1615 is typically 12dB.

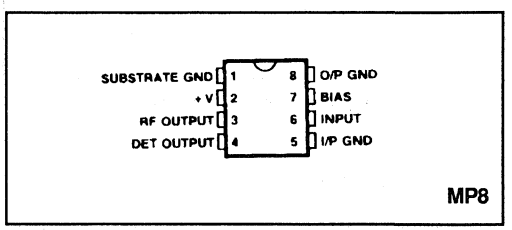


Fig.1 Pin connections - top view

FEATURES

- Well Defined Gain
- 4.5dB Noise Figure
- High I/P impedance
- Low O/P impedance
- 150MHz Bandwidth
- On-Chip Supply Decoupling
- Low External Component Count

APPLICATIONS

- Logarithmic IF Strips with Gains up to 108dB and Linearity Better than 2dB
- Low Cost Radar
- Radio Telephone Filed Strength Meters

ABSOLUTE MAXIMUM RATINGS

Storage temperature range	-55°C to +150°C
Operating temperature range	-30°C to +85°C
Thermal resistance	
Chip-to-ambient	163°C/W
Chip-to-case	57°C/W
Maximum instantaneous voltage at video output	+12V
Supply voltage	9V

ORDERING INFORMATION

SL1615 NA MP

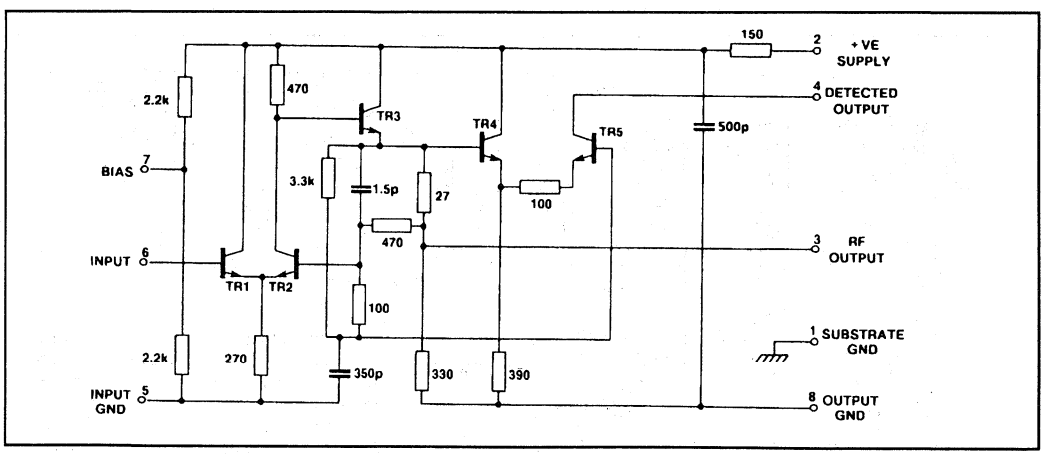


Fig.2 Circuit diagram

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated)
Temperature = +22°C ±2°C, Supply Voltage = +6V, DC Connection between Input and Bias Pins

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Voltage Gain, f = 30MHz	10		14	dB	10Ω Source, 8pF Load
Voltage Gain, f = 60MHz	10.7		13.3	dB	10Ω Source, 8pF Load
Upper Cut-off frequency (Fig.3)	130	170		MHz	10Ω Source, 8pF Load
Lower Cut-off frequency (Fig.3)		5		MHz	10Ω Source, 8pF Load
Propagination Delay		2		ns	
Maximum rectified Video Output Current (Fig.4 and 5)	0.80		1.40	mA	f = 60MHz, 0.5V rms Input
Variation of Gain with Supply Voltage		0.7		db/V	
Variation of Maximum Rectified Output Current with Supply Voltage		25		%/V	
Maximum Input Signal before Overload	1.8	1.9		V/rms	See Note below
Noise Figure (Fig.6)		4		dB	f = 60MHz, Rs = 450Ω
Supply Current	11.5		20	mA	
Maximum RF Output Voltage		1.2		Vp-p	

Note: Overload occurs when the input signal reaches a level sufficent to forward bias the base-collector junction of TR1 on peaks

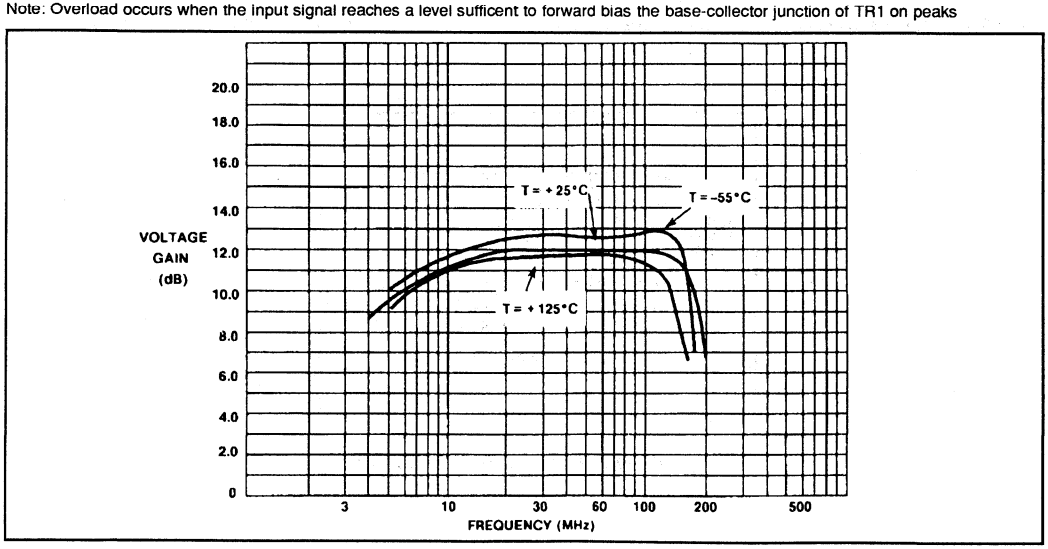


Fig.3 Voltage gain v. frequency

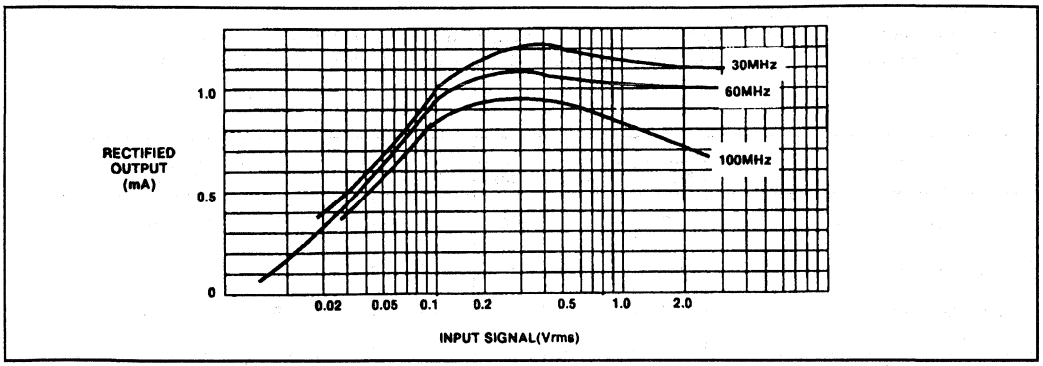


Fig.4 Rectified Output Current v. Input Signal

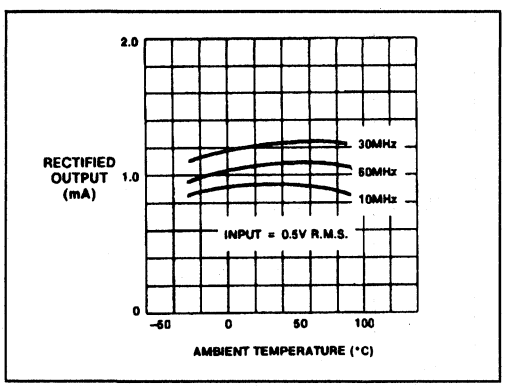


Fig.5 Maximum Rectified Output Current v. Temperature

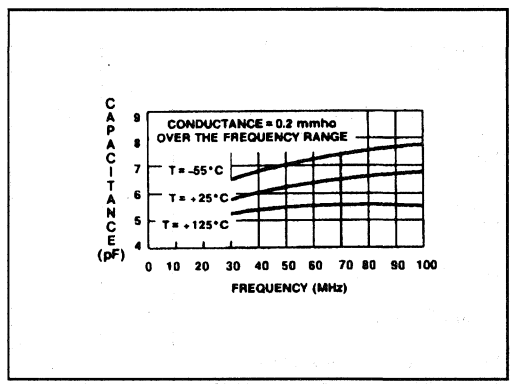


Fig.7 Input Admittance with Open Circuit Output

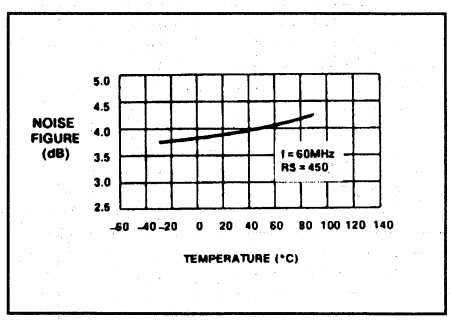


Fig.6 Typical Noise Figure v. Temperature

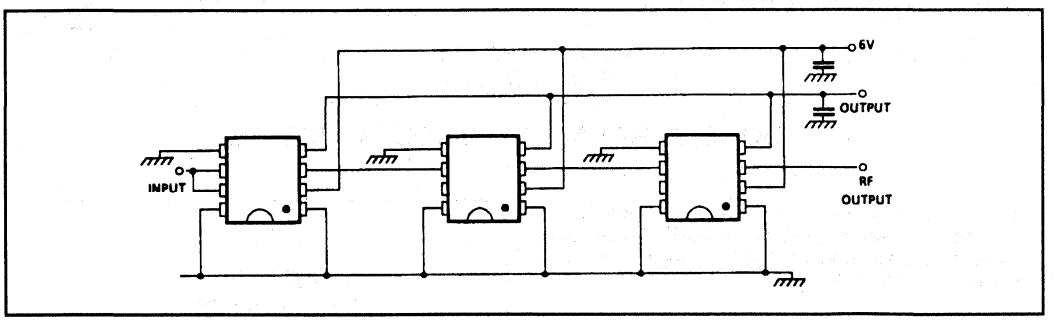


Fig.8 Direct coupled amplifiers

OPERATING NOTES

The amplifiers are intended for use directly coupled, as shown in Fig. 8.

The seventh stage in an untuned cascade will be giving virtually full output on noise.

Noise may be reduced by inserting a single tuned circuit in the chain. As there is a large mismatch between stages a simple parallel or series circuit cannot be used. This choice of network is also controlled by the need to avoid distorting the logarithmic law: the network must give unity voltage transfer at resonance. A suitable network is shown in Fig. 9. The value of C3 must be chosen so that at resonance its admittance equals the total loss conductance across the tuned circuit. Resistor R12 may be introduced to improve the symmetry of filter response, providing other values are adjusted for unity gain at resonance.

A single capacitor may not be suitable for decoupling the output line if many stages and fast rise times are required.

Values of supply line decoupling capacitor required for untuned cascades are given below. Smaller values can be used in high frequency tuned cascades.

The amplifiers have been provided with two ground leads to avoid the introduction of common ground lead inductance between input and output circuits. the equipment designer should take care to aviod the subsequent introduction of such inductance.

	Number of stages			
	6 or more	5	4	3
Minimum capacitance	30nF	10nF	3nF	InF

The on-chip 500pF supply decoupling capacitor has a resistance of, typically 10Ω. It is a junction type having a low breakdown voltage and consequently the positive supply current will increase rapidly if the supply voltage exceeds 7.5V. (See Absolute Maximum Ratings).

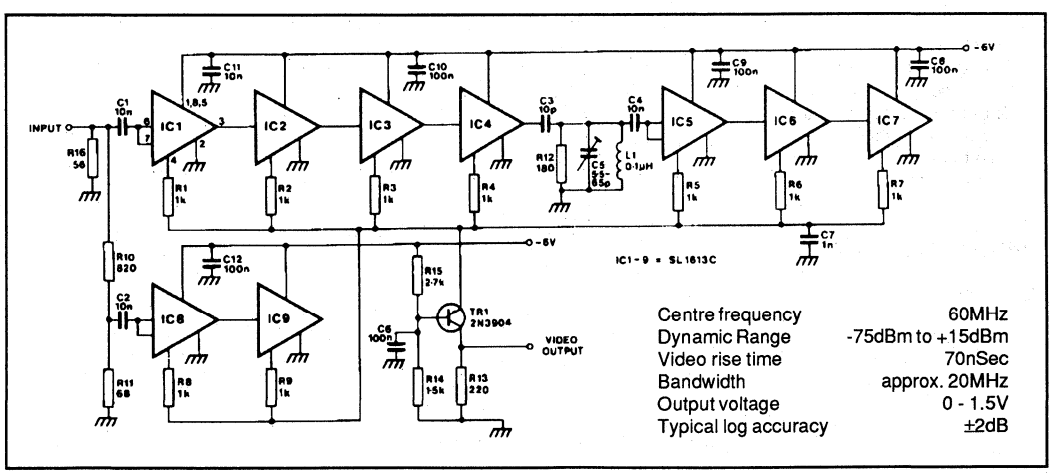


Fig.9 Circuit diagram of low strip

SL1640 IS FOR MAINTENANCE PURPOSES ONLY AND IS NOT RECOMMENDED FOR NEW DESIGNS

SL1640

DOUBLE BALANCED MODULATORS

The SL1640 is a double balanced modulator intended for use in radio systems at frequencies up to 75MHz. The SL1640 has an integral output load resistor (Pin 5) together with an emitter follower output (Pin 6).

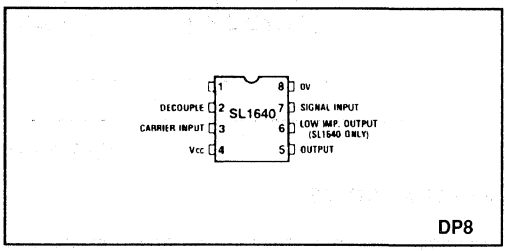


Fig.1 Pin connections (top view)

FEATURES

- No External Bias Networks Needed
- Easy Interfacing
- Choice of Voltage or Current Outputs

APPLICATIONS

- Mixers In Radio Transceivers
- Phase Comparators
- Modulators

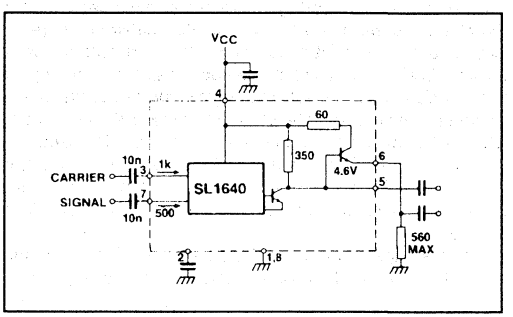


Fig.2 Block diagram (SL1640)

QUICK REFERENCE DATA

- Supply Voltage: 6V
- Conversion Gain: 0dB
- Maximum Inputs: 200mV rms

ABSOLUTE MAXIMUM RATINGS

Supply voltage:	9V
Storage temperature:	-55°C to +150°C
Operating temperature range:	0°C to +70°C
Chip operating temperature:	+150°C
Thermal resistance	
Chip-to-ambient	111°C/W
Chip-to-case	71°C/W

ORDERING INFORMATION

SL1640 C DP

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated)
Supply voltage Vcc: 6V
Ambient temperature: 22°C ± 2°C

Characteristics	Circuit	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	SL1640		12	17	mA	
Conversion gain	SL1640	-3	0	+3	dB	
Noise figure			10		dB	
Carrier input impedance			1		KΩ	
Signal input impedance	SL1640		500		Ω	
			210		KΩ	
Maximum input voltage	SL1640				mV rms	
Signal leak	SL1640		-30		dB	Signal: 70mVrms, 1.75MHz Carrier: 100mV rms, 28.25MHz Output: 30MHz
Signal leak	SL1640		-18		dB	Signal: 70mVrms, 30MHz Carrier: 100mV rms, 28.25MHz Output: 1.75MHz
Intermodulation products	SL1640		-45		dB	Signal 1: 42.5mVrms, 1.75MHz Signal 2: 42.5mV rms, 2MHz Carrier: 100mV rms, 28.25MHz Output: 29.75MHz

APPLICATION NOTES

The SL1640 requires input and output coupling capacitors which normally should be chosen to present a low reactance compared with the input and output impedances (see Electrical Characteristics). However, for minimum carrier leak at high frequencies the signal input should be driven from a low impedance source, in which case the signal input capacitor reactance should be comparable with the source impedance. Pin 2 must be decoupled to earth via a capacitor which presents the lowest possible impedance at both carrier and signal frequencies. The presence of these frequencies at Pin 2 would give rise to poor rejection figures and to distortion

There are two outputs from the SL1640: one is a voltage source of output impedance 350 ohms and 8pF and the other is the emitter of an emitter follower connected to the first output. The output on pin 6 requires a discrete load resistor of not less than 1500 ohms to ground. The emitter follower output should not be used to drive capacitive loads as emitter followers act as detectors under such circumstances with resultant distortion and harmonic generation. Frequency shaping components may be connected to the voltage output and the shaped signal taken from the emitter follower.

Signal and carrier leak may be reduced by altering the bias on the carrier and signal input pins, as shown in Fig.3. With carrier but no signal R1 is adjusted for minimum carrier leak A similar network is connected to the carrier input and with signal and carrier present, signal leak is minimised by means of R2.

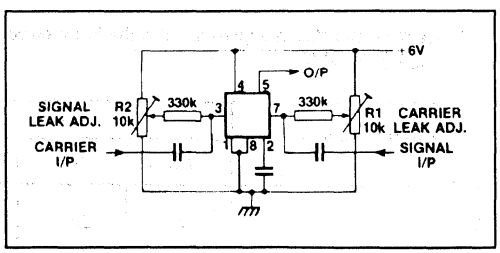


Fig.3 Signal and carrier leak adjustment

SL2364

VERY HIGH PERFORMANCE TRANSISTOR ARRAYS

The SL2364 is an array of transistors internally connected to form a dual long-tailed pair with tail transistors. This is a monolithic integrated circuit manufactured on a very high speed bipolar process which has a minimum useable f_T of 2.5GHz, (typically 5GHz).

The SL2364 is in a 14 SO package and a high performance Dilmon encapsulation.

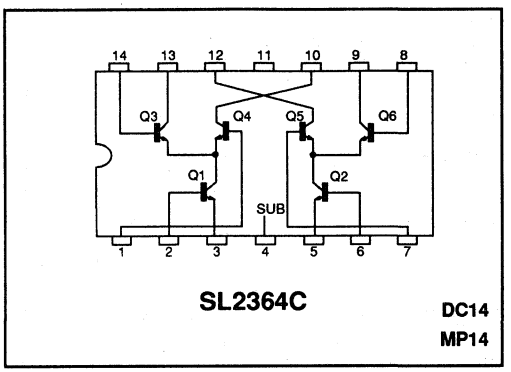


Fig. 1 Pin connections (top view)

FEATURES

- Complete Dual Long-Tailed Pair in One Package
- Very High f_T - Typically 5 GHz
- Very Good Matching Including Thermal Matching

APPLICATIONS

- Wide Band Amplification Stages
- 140 and 560 MBit PCM Systems
- Fibre Optic Systems
- High Performance Instrumentation
- Radio and Satellite Communications

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed of the following conditions (unless otherwise stated):
T_{amb} = 22°C ±2°C

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
BV_{CBO}	10	20		V	I_C = 10µA
LV_{CEO}	6	9		V	I_C = 5mA
BV_{EBO}	2.5	5.0		V	I_E = 10µA
BV_{CIO}	16	40		V	I_C = 10µA
h_{FE}	50	80			I_C = 8mA, V_{CE} = 2V
f_T	2.5	5		GHz	I_C Tail) = 8mA, V_{CE} = 2V
ΔV_{BE} (See note 1)		2	5	mV	I_C Tail) = 8mA, V_{CE} = 2V
$\Delta V_{BE} / T_{AMB}$		-1.7		mV/°C	I_C Tail) = 8mA, V_{CE} = 2V
C_{CB}		0.5	0.8	pF	V_{CB} = 0
C_{CI}		1.0	1.5	pF	V_{CI} = 0

NOTE 1. ΔV_{BE} applies to $|V_{BEQ3} - V_{BEQ4}|$ and $|V_{BEQ5} - V_{BEQ6}|$

TYPICAL CHARACTERISTICS

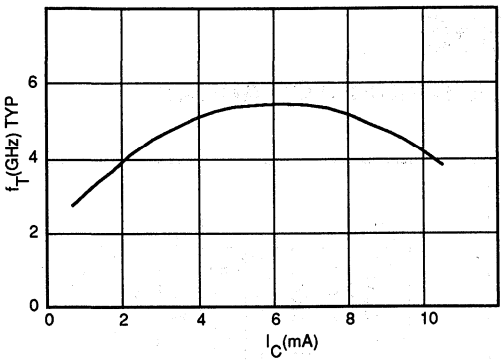


Fig. 2 Collector current

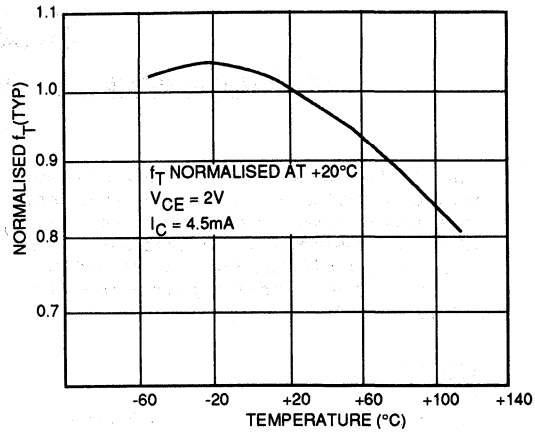


Fig. 3 Chip temperature

ABSOLUTE MAXIMUM RATINGS

Maximum individual transistor dissipation 200mW

Storage temperature -55°C to + 150°C
Maximum junction temperature + 150°C
Package thermal resistance (°C/W):
Chip to case 45 (MP14) 35 (DC14)
Chip to ambient 123 (MP14) 120 (DC14)
VCBO = 10V, VEBO = 2 5V VCEO = 6V. VCIO = 15V IC (any one transistor) = 20mA

The substrate should be connected to the most negative point of the circuit to maintain electrical isolation between the transistors.

SL2365

VERY HIGH PERFORMANCE TRANSISTOR ARRAY

The SL2365 is an array of transistors internally connected to form a dual long-tail pair with current mirrors whose bases and collectors are connected internally. The ICs are manufactured on a very high speed bipolar process which has a minimum usable fT of 2.5GHz (typically 5GHz). The current mirror enables a well defined gain at low current levels to be achieved.

FEATURES

- Complete Dual Long Tailed Pair in One Package
- Very High fT - Typically 5GHz
- Well Defined Gain at Low Current Levels
- Available in Small Outline Package

CAUTION

Pins 4 and 11 should be equal and at the most negative voltage on the array.

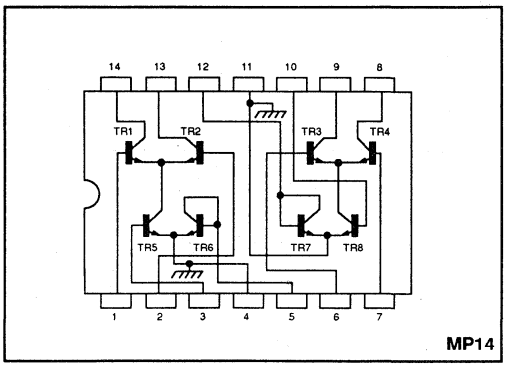


Fig. 1 Pin connections (top view)

ELECTRICAL CHARACTERISTICS

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
BV_{CBO}	10	20		V	I_C = 10μA
LV_{CEO}	6	9		V	I_C = 5mA
BV_{EBO}	2.5	5		V	I_E = 10μA
BV_{CIO}	16	40		V	I_C = 10μA
H_{fe}	50	80			I_C = 8mA, V_{CE} = 2V
f_T	2.5	5		GHz	I_C Tail) = 8mA, V_{CE} = 2V
ΔV_{BE}		2	5	mV	I_C Tail) = 8mA, V_{CE} = 2V
$\Delta V_{BE} / T_{AMB}$		-7		mV/°C	I_C Tail) = 8mA, V_{CE} = 2V
C_{CB}		0.5	0.8	pF	V_{CB} = 0
C_{CI}		1.0	1.5	pF	V_{CI} = 0

SL2524

1.3GHz DUAL WIDEBAND LOGARITHMIC AMPLIFIER

The SL2524 is a pin compatable replacement for the SL2521 and SL2522 series of log amplifiers, and exhibits a superior stability performance. The amplifier is a successive detection type which provides linear gain and accurate logarithmic signal compression over a wide bandwidth. The two stages can be operated independently.

When six stages (three SL2524s) are cascaded the strip can be used for IFs between 30–650MHz whilst achieving greater than 65dB dynamic range with a log accuracy of <±1.0dB. The balanced limited output also offers accurate phase information with input amplitude.

FEATURES

- 1.3GHz Bandwidth (–3dB)
- Balanced IF limiting
- 3ns Rise Times/5ns Fall Times (six stages)
- 20ns Pulse Handling (six stages)
- Temperature Stabilised
- Surface Mountable

APPLICATIONS

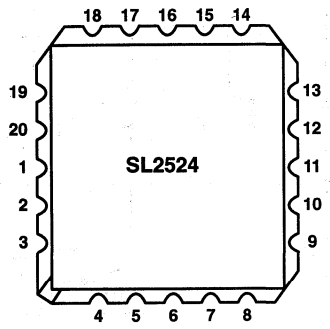
- Ultra Wideband Log Receivers
- Channelised Receivers
- Monopulse Applications

ABSOLUTE MAXIMUM RATINGS

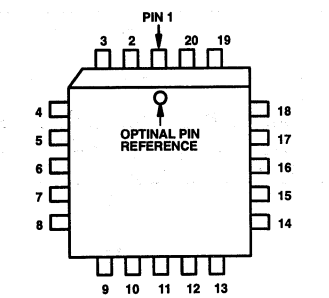
Supply voltage (V_{CC} above V_{EE})		+7.0V
Storage temperature		–65°C to + 150°C
Operating temperature range		
SL2524/B/LC		–40°C to +85°C
SL2524/C/HP		–30°C to +85°C
Junction temperature	–LC20	+175°C
	–HP20	+150°C
Applied DC voltage to RF input		±0.4V (between RF I/P pins)
Applied RF power to RF input		+15dBm
Value of R_{SET} resistors		NOT less than 180Ω
Thermal resistance:–		
Die to case	–LC20	28°C/W
	–HP20	20°C/W
Die to ambient	–LC20	73°C/W
	–HP20	82°C/W

ORDERING INFORMATION

SL2524/B/LC (Ceramic leadless chip carrier package)
SL2524/C/HP (Plastic J lead chip carrier package)
SL2524/NA/1C (DC probe tested bare die)
5962 – 92315 (SMD)



LC20



HP20

PIN	DESCRIPTION	PIN	DESCRIPTION
1	SUB V_{EE}	11	N/C
2	IF OUTPUT (A)	12	R SET (B)
3	IF OUTPUT (A)	13	DET. OUTPUT (B)
4	V_{EE} (A)	14	V_{CC} (B)
5	OUTPUT V_C (A)	15	IF OUTPUT (B)
6	IF INPUT (A)	16	IF OUTPUT (B)
7	IF INPUT (A)	17	OUTPUT V_{CC} (B)
8	V_{CC} (A)	18	V_{EE} (B)
9	DET. OUTPUT (A)	19	IF INPUT (B)
10	R SET (A)	20	IF INPUT (B)

Fig. 1 Pin connections top view

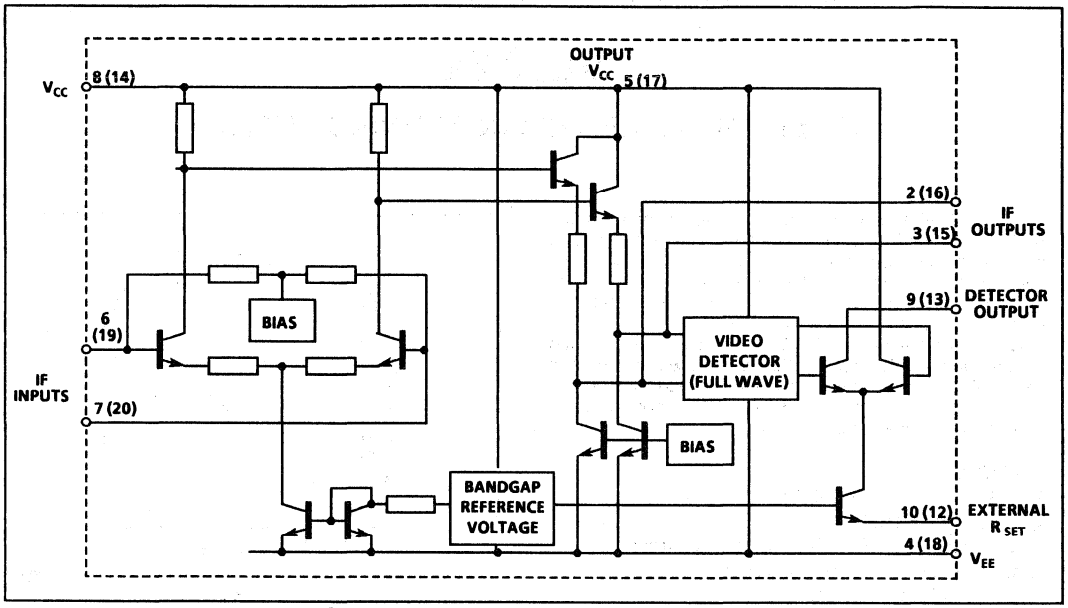
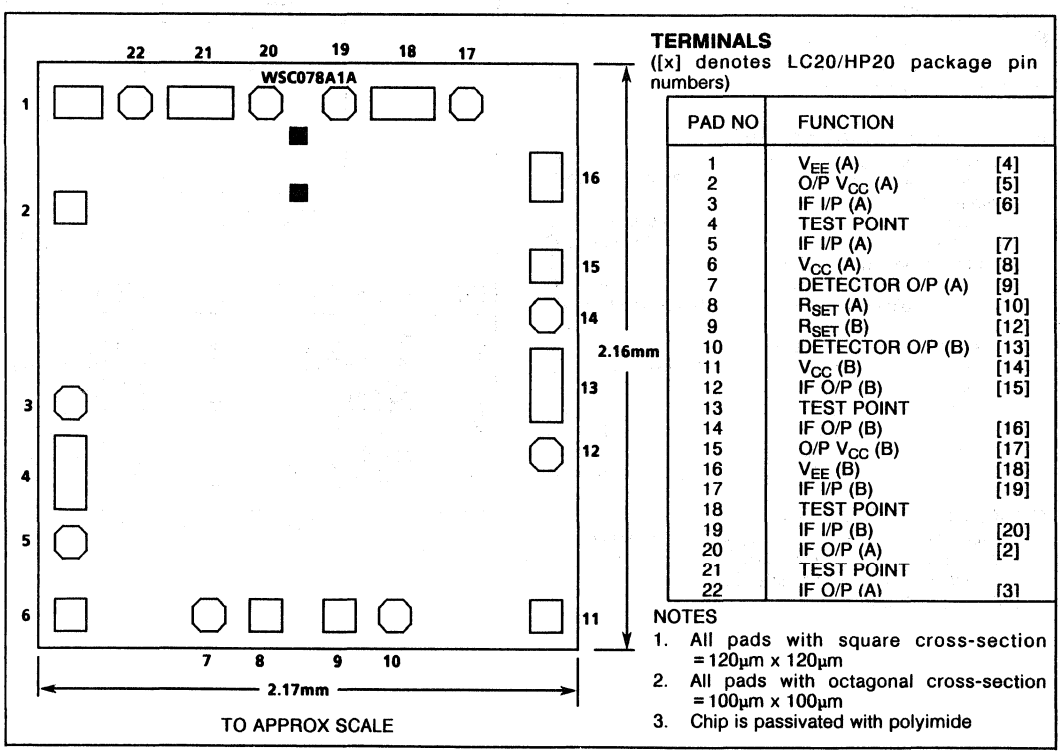


Fig. 2 Circuit diagram of single stage A - (stage B pin Nos bracketed)



TERMINALS

([x] denotes LC20/HP20 package pin numbers)

PAD NO	FUNCTION	
1	V_{EE} (A)	[4]
2	O/P V_{CC} (A)	[5]
3	IF I/P (A)	[6]
4	TEST POINT	
5	IF I/P (A)	[7]
6	V_{CC} (A)	[8]
7	DETECTOR O/P (A)	[9]
8	R_{SET} (A)	[10]
9	R_{SET} (B)	[12]
10	DETECTOR O/P (B)	[13]
11	V_{CC} (B)	[14]
12	IF O/P (B)	[15]
13	TEST POINT	
14	IF O/P (B)	[16]
15	O/P V_{CC} (B)	[17]
16	V_{EE} (B)	[18]
17	IF I/P (B)	[19]
18	TEST POINT	
19	IF I/P (B)	[20]
20	IF O/P (A)	[2]
21	TEST POINT	
22	IF O/P (A)	[3]

NOTES

1. All pads with square cross-section = 120µm x 120µm
2. All pads with octagonal cross-section = 100µm x 100µm
3. Chip is passivated with polyimide

Fig 3. Pad map for SL2524 naked die

ELECTRICAL CHARACTERISTICS -SL2524B

Guaranteed at the following test conditions unless otherwise stated

Frequency = 200MHz, T_{amb} = 25°C Input power = -30dBm, V_{CC} = 6V ±0.1V, Source Impedance = 50Ω. Load impedance = 50Ω Test Circuit = Fig. 4 R_{SET} = 300Ω. Tested as a dual stage.

Characteristic	Value			Units	Conditions
	Min	Typ	Max		
Supply current	70	87	100	mA	
Small signal gain (dual stage, single ended)	9.6	11.4	13.0	dB	T_{amb} = +25°C f = 25MHz See Notes 1, 3
	10.1	11.6	13.1	dB	T_{amb} = -40°C f = 200MHz. See Notes 2, 3
	9.9	11.3	12.7	dB	T_{amb} = +25°C f = 200MHz. See Note 3
	9.5	11.0	12.5	dB	T_{amb} = +85°C f = 200MHz. See Notes 2, 3
	9.7	11.2	12.7	dB	T_{amb} = -40°C f = 500MHz. See Notes 2, 3
	9.3	10.7	12.1	dB	T_{amb} = +25°C f = 500MHz. See Note 3
	8.2	9.7	11.2	dB	T_{amb} = +85°C f = 500MHz. See Notes 2, 3
Detected output current (max)	3.20	3.45	3.70	mA	T_{amb} = +25°C, V_{IN} = 0dBm, f = 25MHz. See Note 1
	3.05	3.25	3.45	mA	T_{amb} = -40°C, V_{IN} = 0dBm, f = 200MHz See Note 2
	3.15	3.30	3.45	mA	T_{amb} = +25°C, V_{IN} = 0dBm, f = 200MHz
	3.10	3.30	3.50	mA	T_{amb} = +85°C, V_{IN} = 0dBm, f = 200MHz See Note 2
	2.80	3.10	3.30	mA	T_{amb} = -40°C, V_{IN} = 0dBm, f = 500MHz See Note 2
	2.90	3.15	3.45	mA	T_{amb} = +25°C, V_{IN} = 0dBm, f = 500MHz
	2.85	3.10	3.65	mA	T_{amb} = +85°C, V_{IN} = 0dBm, f = 500MHz See Note 2
Detected output current (no signal)	0.85	0.95	1.15	mA	T_{amb} = -40°C, See Note 2
	0.80	0.93	1.10	mA	T_{amb} = +25°C, See Note 2
	0.80	0.90	1.10	mA	T_{amb} = +85°C, See Note 2
Upper cut off frequency (RF)	600	1100		MHz	-3dB w.r.t. 200MHz, T_{amb} = -40°C See Note 2
	900	1100		MHz	-3dB w.r.t. 200MHz, T_{amb} = +25°C
	600	800		MHz	-3dB w.r.t. 200MHz, T_{amb} = +85°C See Note 2
Lower cut off frequency (RF)		0.35	1	MHz	-3dB w.r.t. 200MHz, T_{amb} = +25°C
Detector cut off frequency		700		MHz	50% O/P current w.r.t. 200MHz
Limited IF O/P voltage	135	155	175	mV	I/P power = 0dBm, T_{amb} = +25°C
Phase variation with input level (normalised to -30dBm)		0 ± 2.0	0 ± 3.0	Degree	Frequency = 70MHz, -55 to +3dBm See Note 2
		-4.0 ± 2.0	-4.0 ± 3.0	Degree	Frequency = 200MHz, -55 to +3dBm See Note 2
Limited O/P var with temp.		±12	±25	mV	See Note 1
Noise figure		14		dB	
Max I/P before overload		15		dBm	
Input impedance		1		kΩ	1kΩ in parallel with 2pF
Output impedance		50		Ω	

NOTES

1. Parameter guaranteed but not tested
2. Tested at 25°C only, but guaranteed at temperature
3. Gain will typically increase by 6dB, when RF outputs use 1KΩ loads in place of 50Ω

ELECTRICAL CHARACTERISTICS -SL2524C

Guaranteed at the following test conditions unless otherwise stated
Frequency = 200MHz, T_{amb} = +25°C, Input power = -30dBm, V_{CC} = 6V ±0.1V, Source Impedance = 50Ω.
Load impedance = 50Ω Test Circuit = Fig. 4 R_{SET} = 300Ω. Tested as a dual stage.

Characteristic	Value			Units	Conditions
	Min	Typ	Max		
Supply current	70	87	100	mA	
Small signal gain (dual stage, single ended)	9.6	11.4	13.0	dB	T_{amb} = +25°C, f = 25MHz See Note 3
	9.6	11.6	13.6	dB	T_{amb} = -30°C f = 200MHz. See Notes 2, 3
	9.4	11.3	13.2	dB	T_{amb} = +25°C f = 200MHz. See Note 3
	9.0	11.0	13.0	dB	T_{amb} = +85°C f = 200MHz. See Notes 2, 3
	9.2	11.2	13.2	dB	T_{amb} = -30°C f = 500MHz. See Notes 1, 3
	8.8	10.7	12.6	dB	T_{amb} = +25°C f = 500MHz. See Note 1
	7.7	9.7	11.7	dB	T_{amb} = +85°C f = 500MHz. See Notes 1, 3
Detected output current (max)	3.20	3.45	3.70	mA	T_{amb} = +25°C, V_{IN} = 0dBm, f = 25MHz.
	2.95	3.25	3.55	mA	T_{amb} = -30°C, V_{IN} = 0dBm, f = 200MHz See Note 2
	3.05	3.30	3.55	mA	T_{amb} = +25°C, V_{IN} = 0dBm, f = 200MHz
	3.00	3.30	3.50	mA	T_{amb} = +85°C, V_{IN} = 0dBm, f = 200MHz See Note 2
	2.70	3.10	3.30	mA	T_{amb} = -30°C, V_{IN} = 0dBm, f = 500MHz See Note 1
	2.80	3.15	3.55	mA	T_{amb} = +25°C, V_{IN} = 0dBm, f = 500MHz See Note 1
	2.75	3.10	3.75	mA	T_{amb} = +85°C, V_{IN} = 0dBm, f = 500MHz See Note 1
Detected output current (no signal)	0.75	0.95	1.25	mA	T_{amb} = -30°C, See Note 2
	0.70	0.93	1.20	mA	T_{amb} = +25°C,
	0.70	0.90	1.20	mA	T_{amb} = +85°C, See Note 2
Upper cut off frequency (RF)		1000		MHz	-3dB w.r.t. 200MHz, T_{amb} = +25°C See Note 1
Lower cut off frequency (RF)		0.35	2	MHz	-3dB w.r.t. 200MHz, T_{amb} = +25°C
Detector cut off frequency		600		MHz	50% O/P current w.r.t. 200MHz
Limited IF O/P voltage	105	135	175	mV	I/P power = 0dBm, T_{amb} = +25°C
Phase variation with input level (normalised to -30dBm)		0 ± 2.0		Degree	Frequency = 70MHz, -55 to +3dBm See Note 1
		-4.0 ± 2.0		Degree	Frequency = 200MHz, -55 to +3dBm See Note 1
Limited O/P var with temp.		±12	±25	mV	See Note 1
Noise figure		14		dB	
Max I/P before overload		15		dBm	
Input impedance		1		kΩ	1kΩ in parallel with 2pF
Output impedance		50		Ω	

NOTES
1. Parameter guaranteed but not tested
2. Tested at 25°C only, but guaranteed at temperature
3. Gain will typically increase by 6dB, when RF outputs use 1KΩ loads in place of 50Ω

GENERAL DESCRIPTION

The SL2524 is primarily intended for use in Radar and EW receivers. Six stages (3 chip carriers) can be cascaded to form a very wideband logarithmic amplifier offering >65dB of input dynamic range, with pulse handling of better than 25ns. (See figs 5 and 6).

A six stage strip also offers balanced IF limiting, linearity (log accuracy) of $< \pm 1.0$dB, temperature stabilisation and programmable detector characteristics.

The detector has an external resistor set (R_{SET})pin which allows the major characteristics of the detector to be programmed. With a six stage strip it is possible to vary the value of R_{SET} on each detector and so improve the overall log error/linearity.

The detector is full wave and good slew rates are achieved with 2ns rise and 5ns fall times (no video filter). The video bandwidth of a six stage strip is typically 600MHz (-3dB).

The amplifier also offers balanced IF limiting, low phase shift versus input amplitude, and at an IF of 120MHz, less than 5° of phase change is achievable over the input level of -55dBm to +5dBm.

The IF and Video ports can be used simultaneously, so offering phase, frequency and pulse (video) information. A slight loss of dynamic range (2dB) will be observed when the IF ports are used in conjunction with the video.

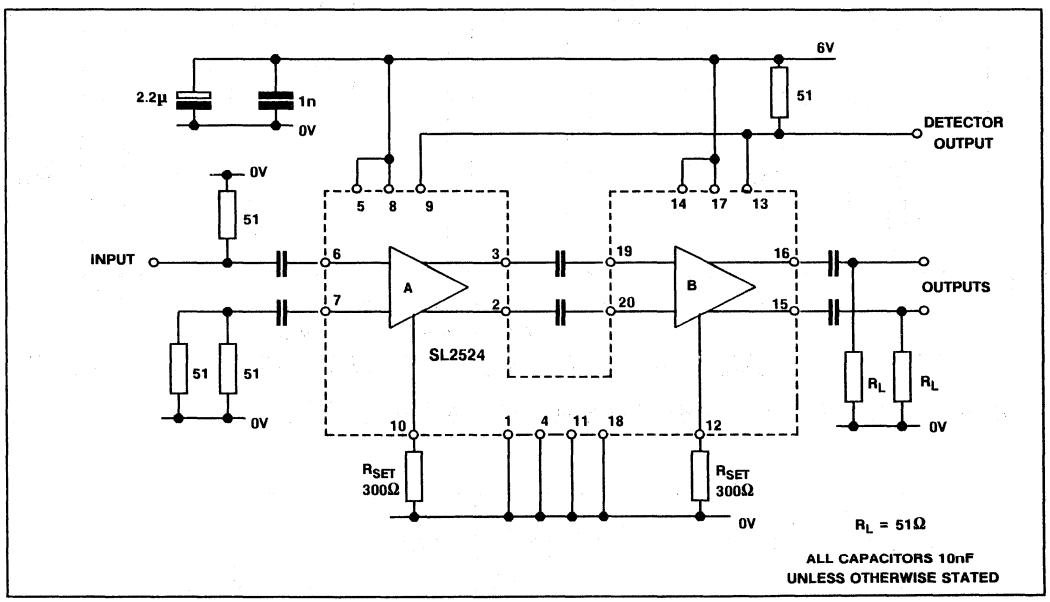


Fig. 4 Test circuit

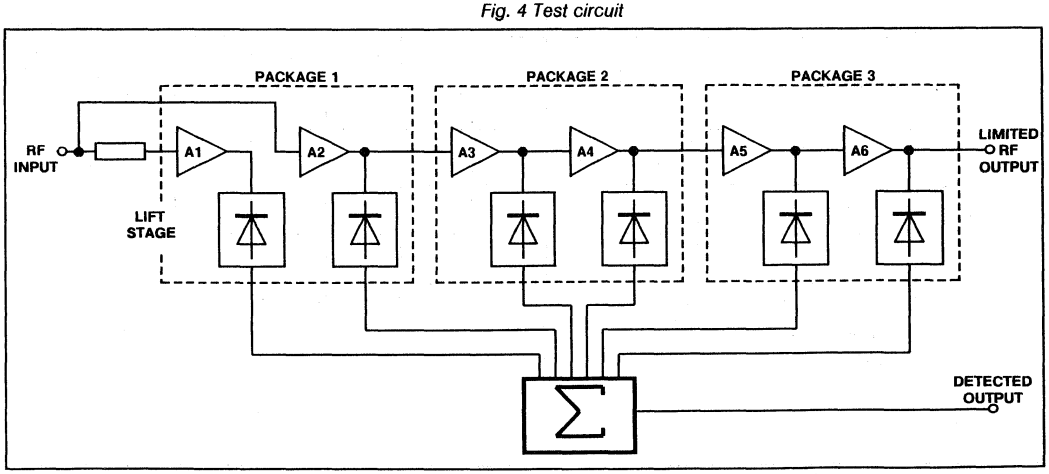


Fig. 5 Schematic diagram showing configuration of SD Log strip

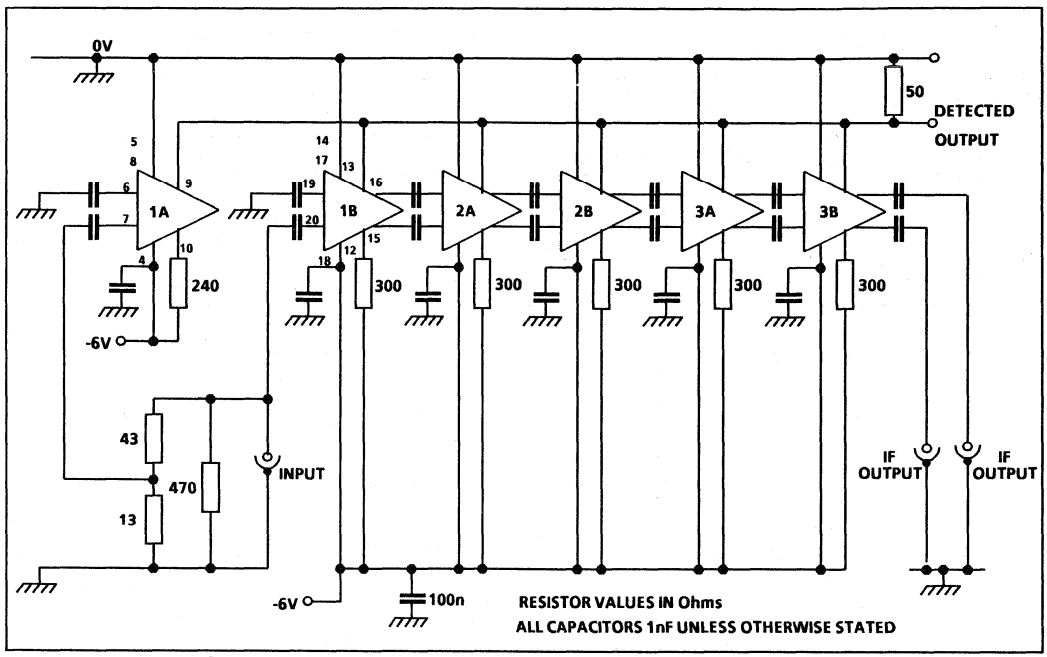


Fig. 6 Circuit diagram for 6-log strip (results shown in figs. 11 to 24 were achieved with this circuit)

Typical characteristics for a dual - stage amplifier (i.e. One SL2524)

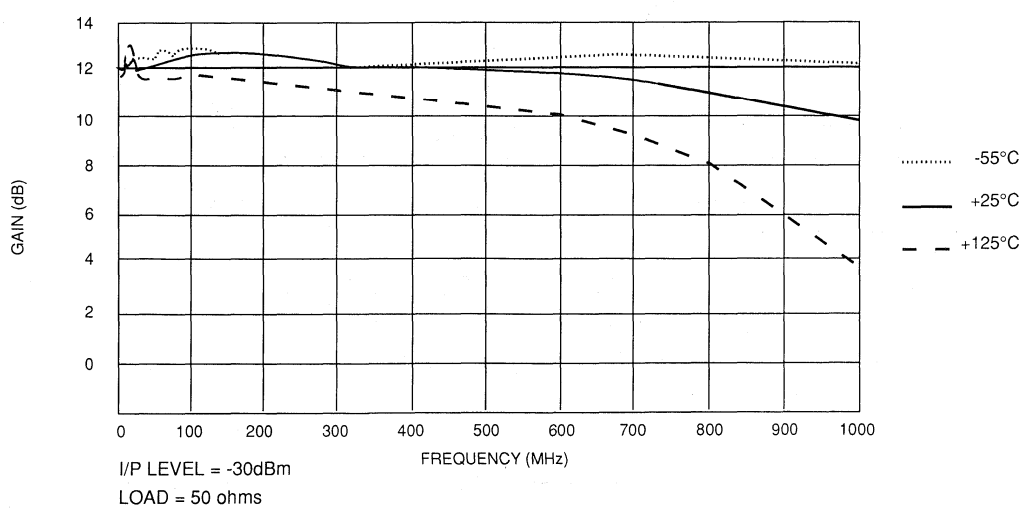


Fig. 7 IF Gain vs frequency of 2 amplifiers (One SL2524)

Typical characteristics for a dual - stage amplifier (i.e. One SL2524) cont.

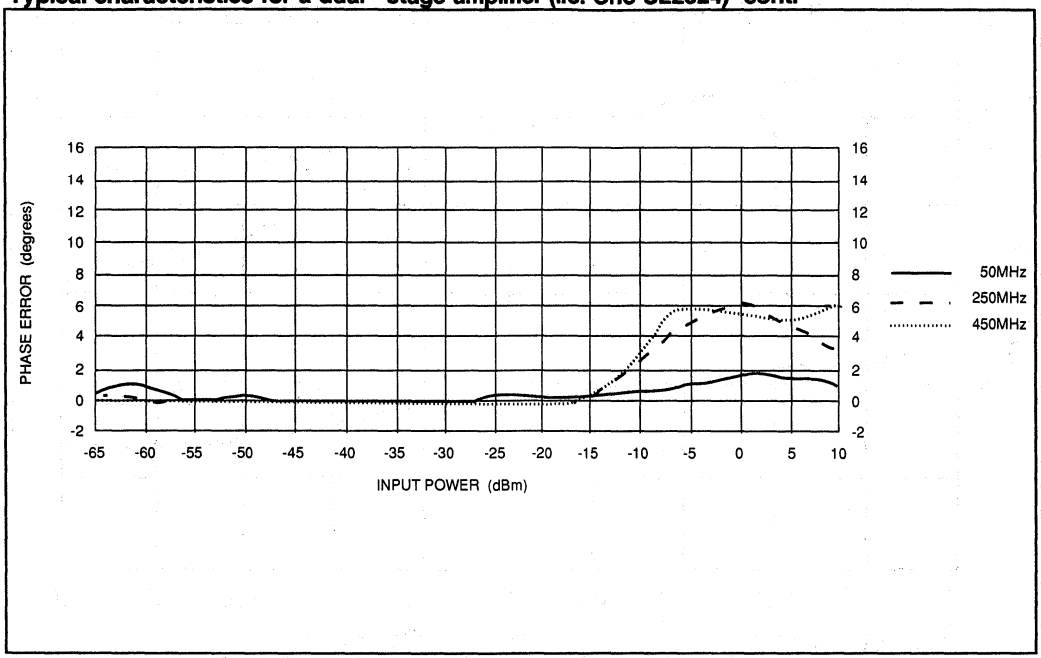


Fig. 8 Normalised phase vs CW input level at 50, 250 and 450MHz for 50Ω O/P termination (25°C)

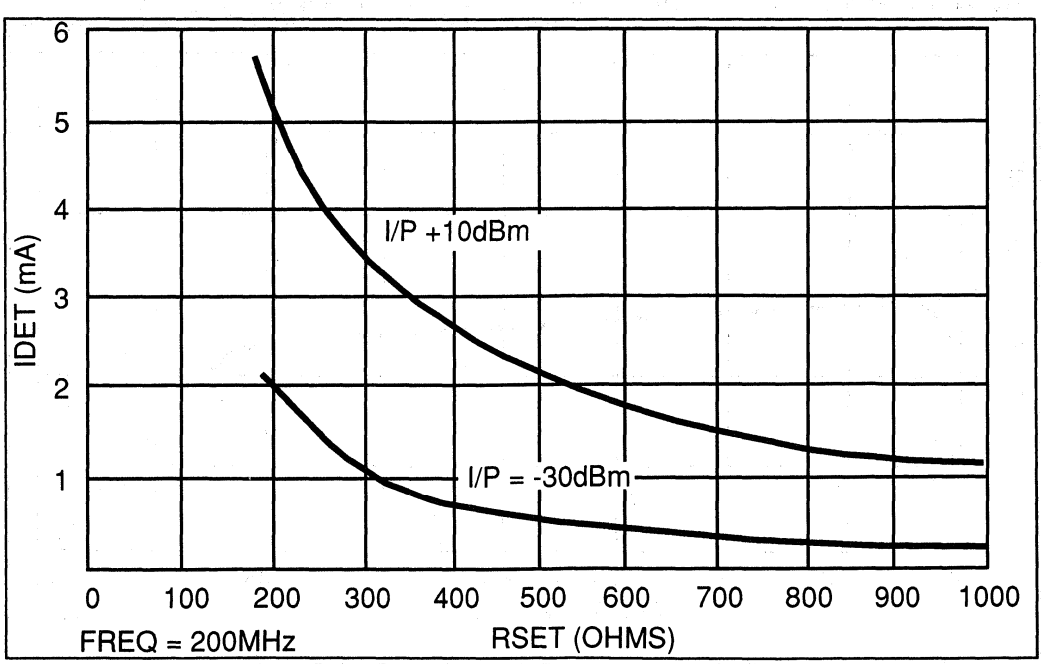


Fig. 9 Detector current vs R_{SET} at 200MHz (25°C)

Typical characteristics for a dual - stage amplifier (i.e. One SL2524) cont.

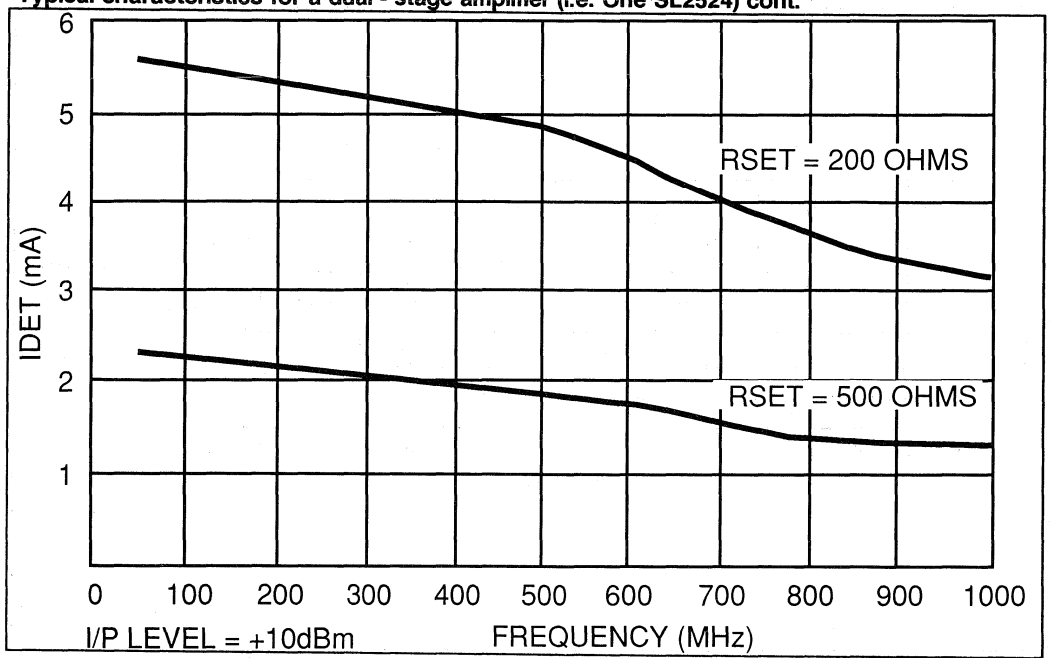


Fig. 10 Detector current vs frequency at RSET =200Ω and 500Ω (25°C)

Typical characteristics for a six stage strip, using detected output (Ref. figs. 5 & 6)

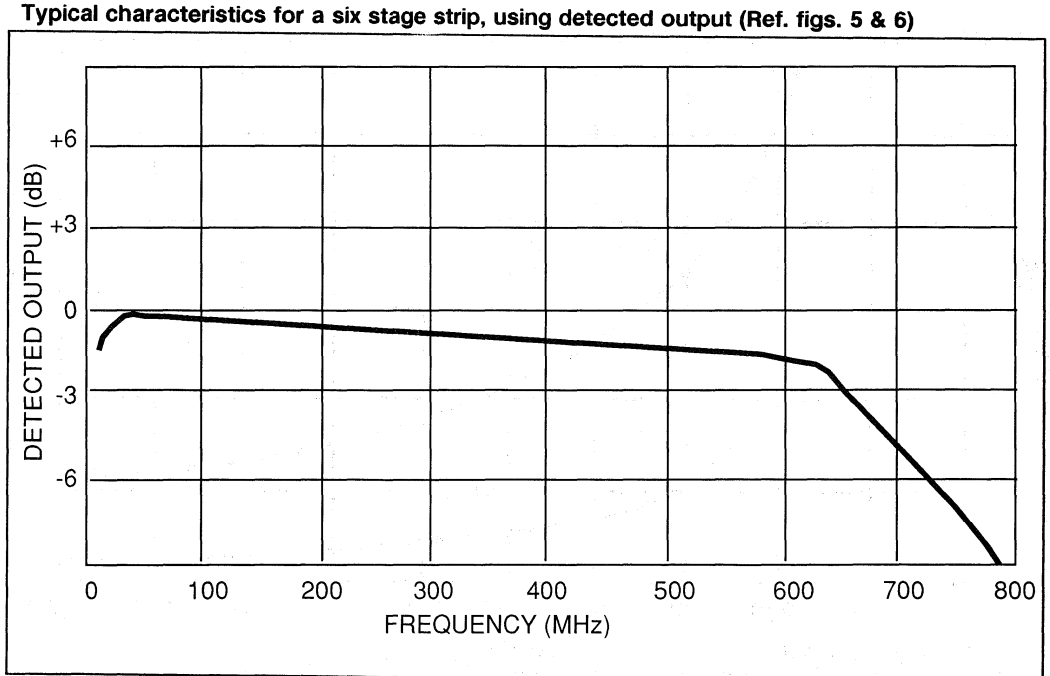


Fig. 11 Detector bandwidth (25°C)

Typical characteristics for a six stage strip, using detected output (Ref. figs. 5 & 6) cont.

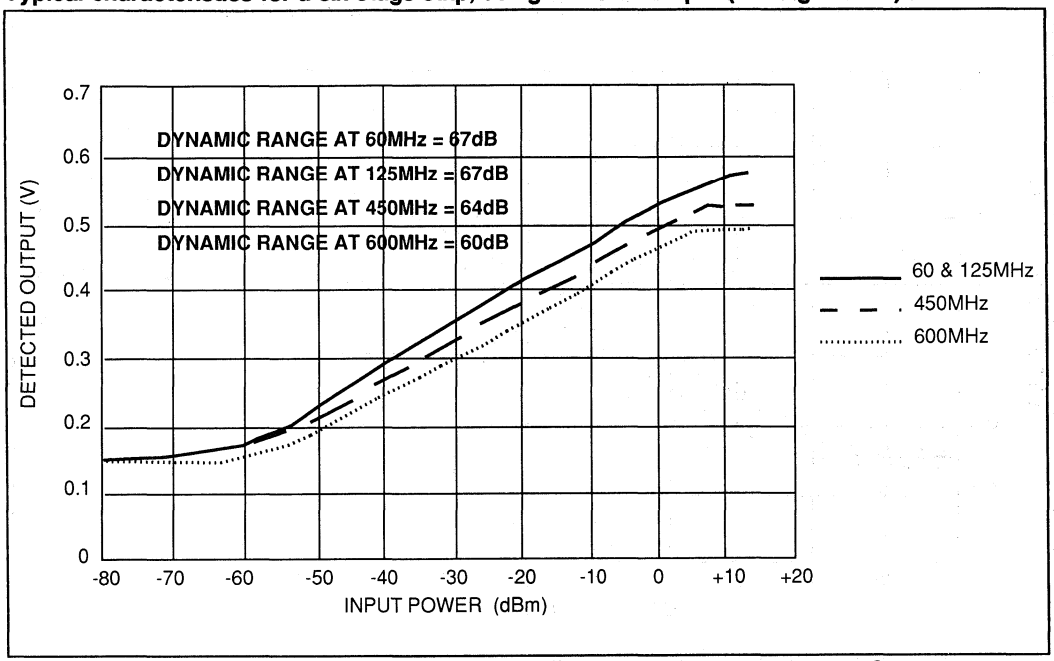


Fig. 12 Detected O/P vs CW input at 60, 125, 450 and 600MHz at 25°C

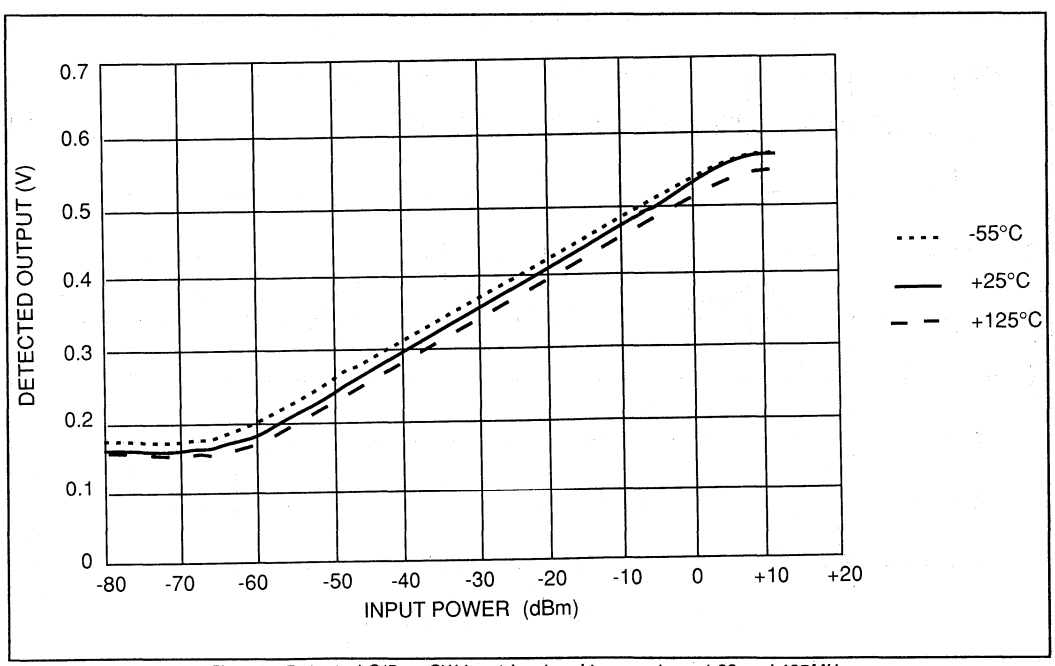


Fig. 13 Detected O/P vs CW input level and temperature at 60 and 125MHz

Typical characteristics for a six stage strip, using detected output (Ref. figs. 5 & 6) cont.

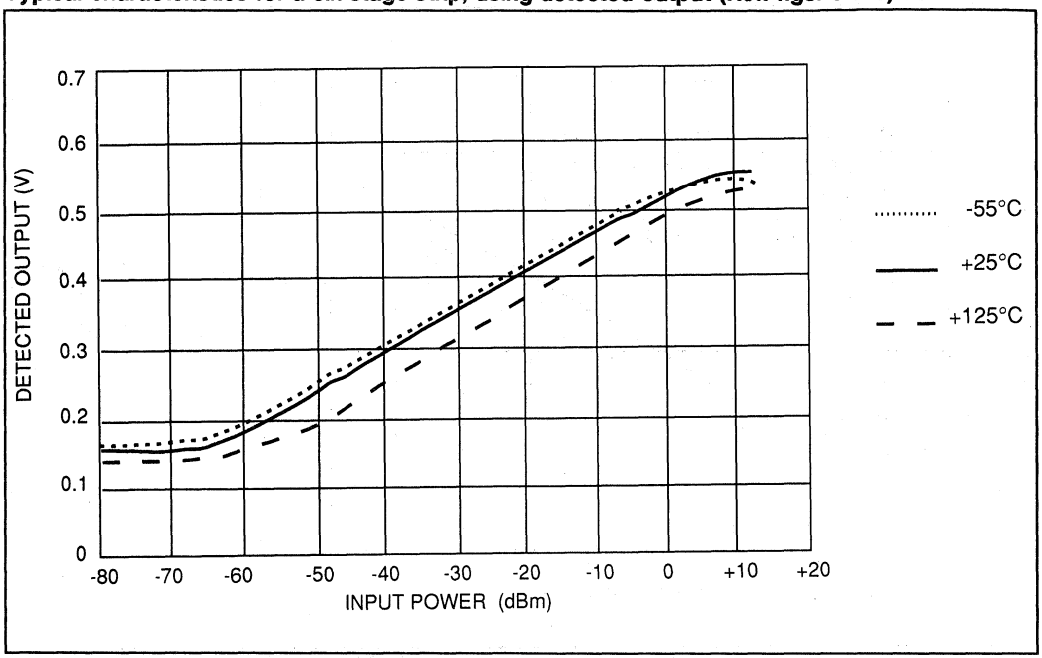


Fig. 14 Detected O/P vs CW input level at 450 MHz across temperature

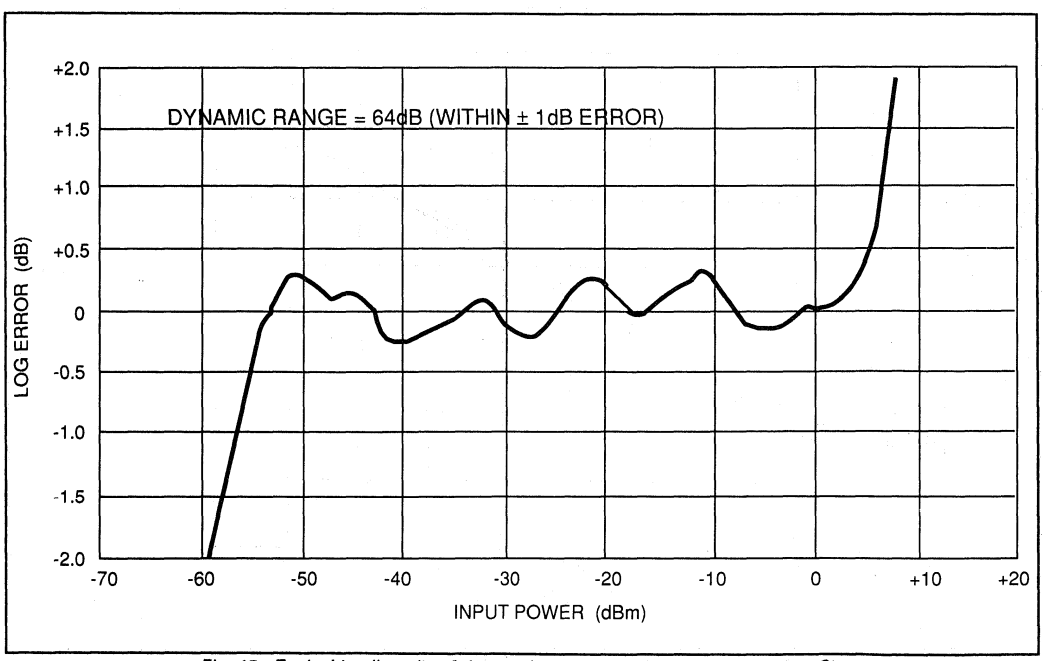


Fig. 15 Typical log linearity of detected output measured at 450MHz (25°C)

Typical characteristics of a six-stage strip as a low phase shift wideband limiter (Ref. figs. 5 & 6)

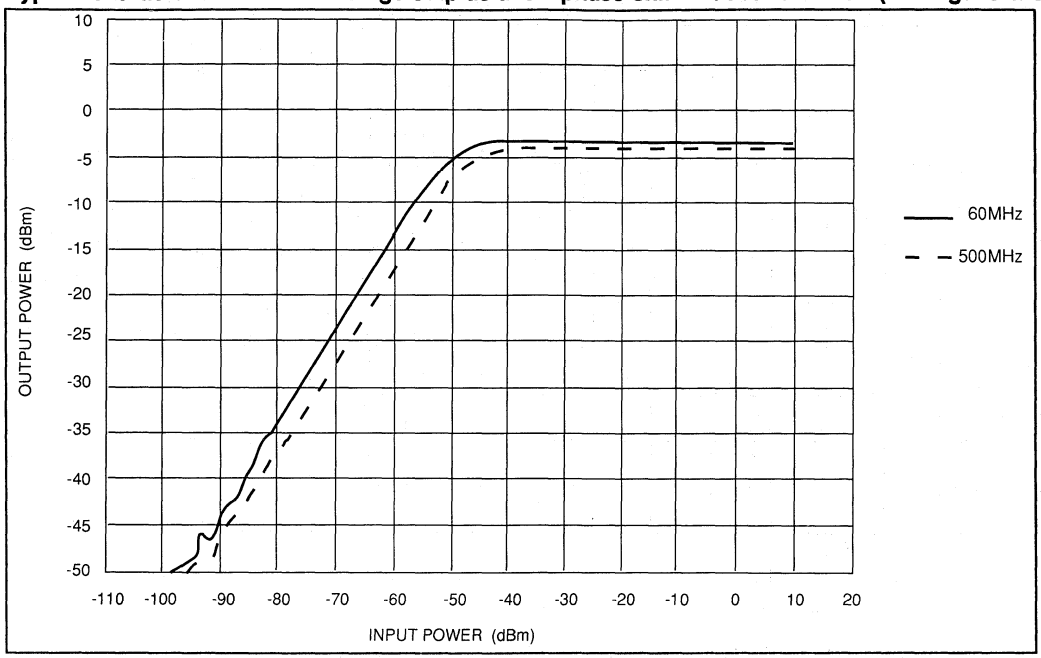


Fig. 16 IF limiting characteristic at 60MHz and 500MHz (25°C)

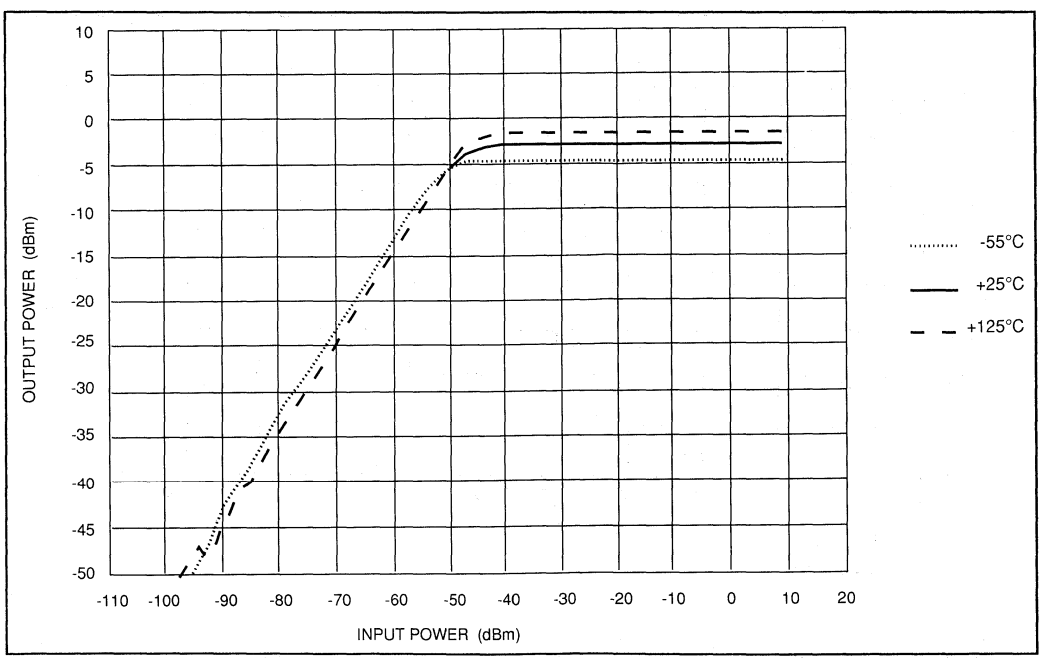


Fig. 17 IF limiting characteristic at 60MHz across temperature

Typical characteristics of a six-stage strip as a low phase shift wideband limiter (Ref. figs. 5 & 6)

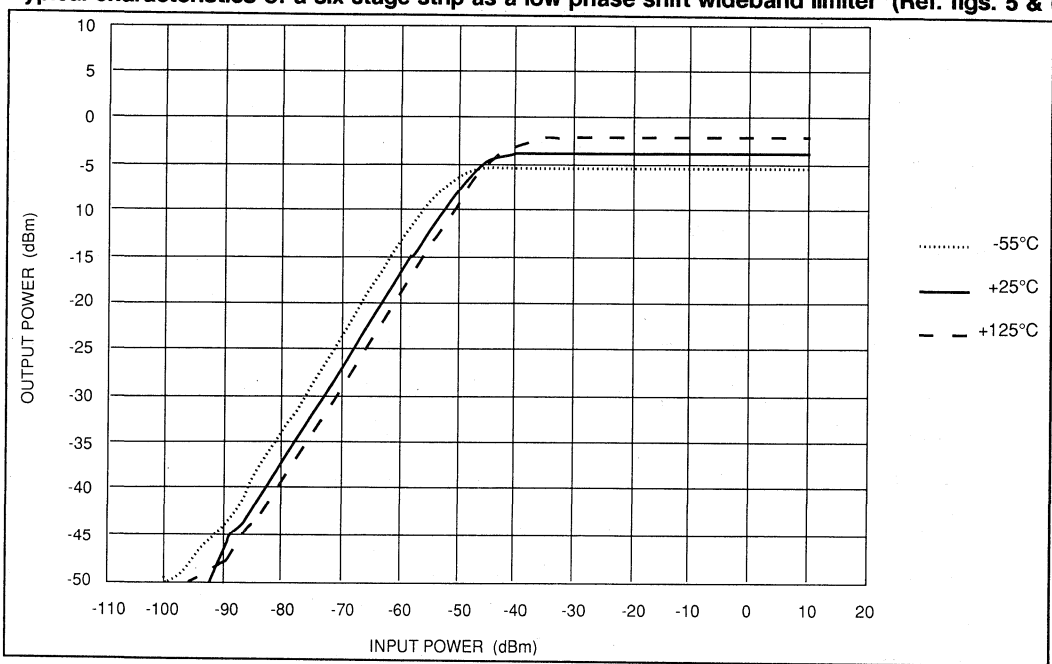


Fig. 18 IF limiting characteristic at 500MHz across temperature

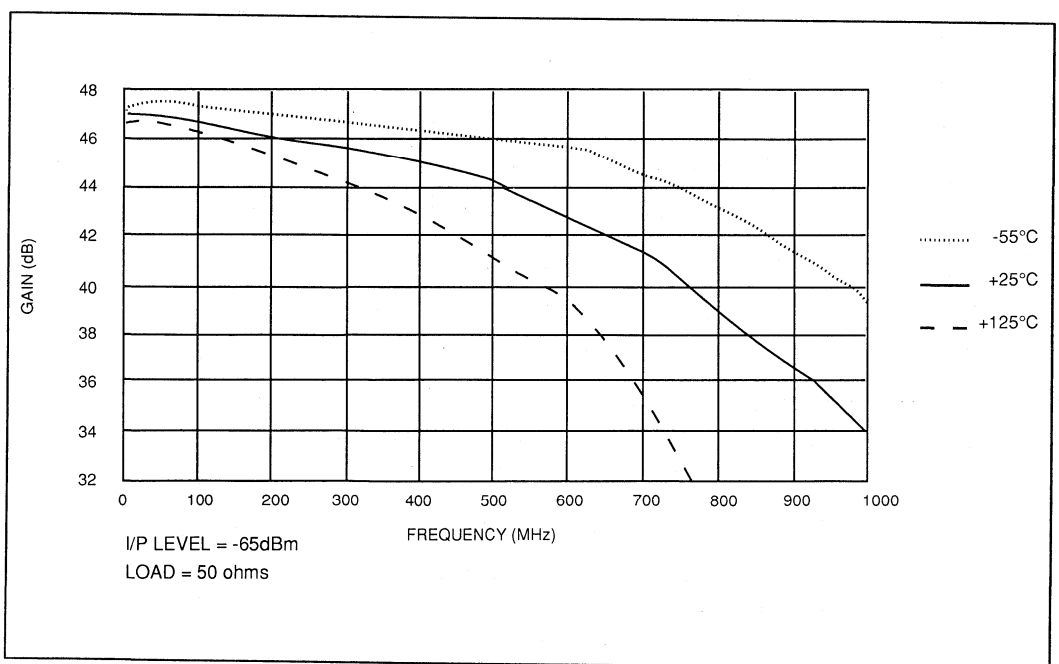


Fig. 19 Small signal gain vs frequency across temperature

Typical characteristics of a six-stage strip as a low phase shift wideband limiter (Ref. figs. 5 & 6)

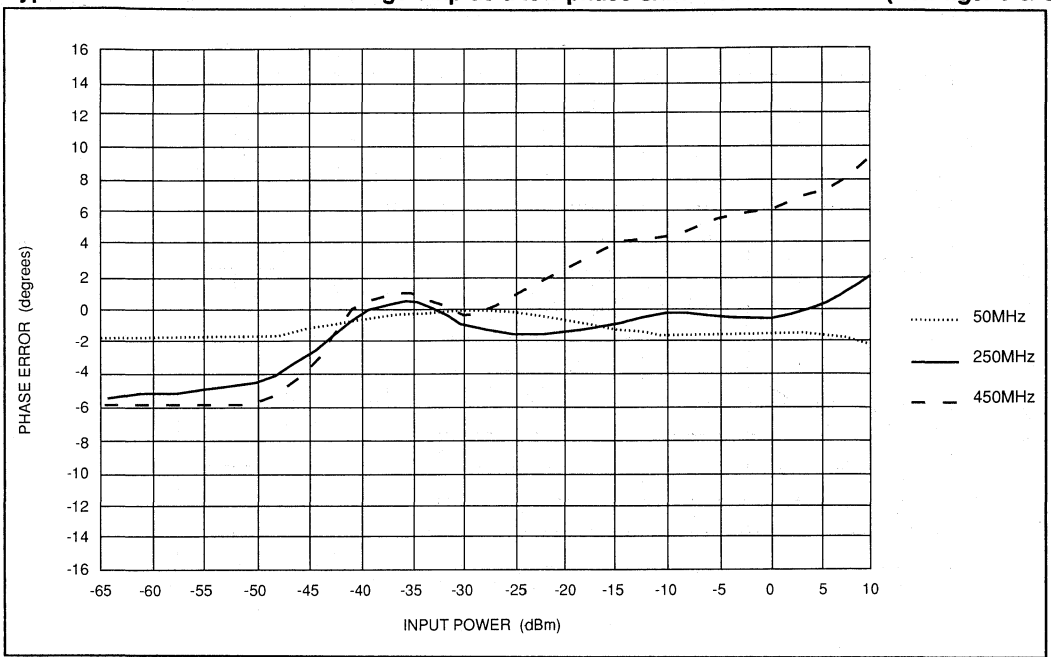


Fig. 20 Phase deviation vs CW input level (normalised at -30dBm) at 25°C across input frequency

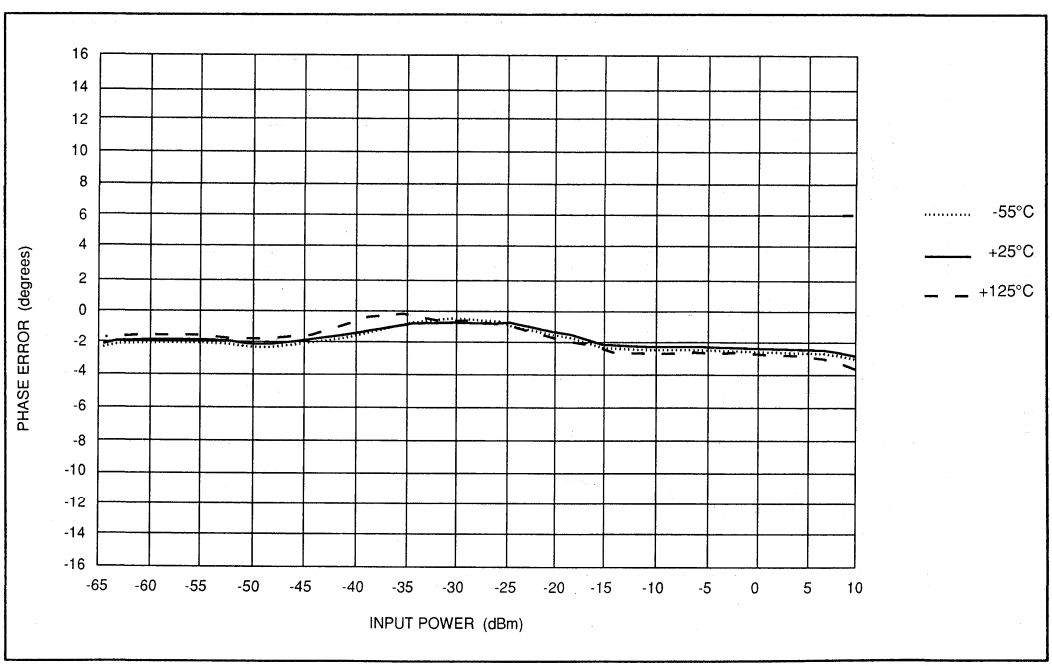


Fig. 21 Phase deviation vs CW input level (normalised at -30dBm) at 50MHz across temperature

Typical characteristics of a six-stage strip as a low phase shift wideband limiter (Ref. figs. 5 & 6)

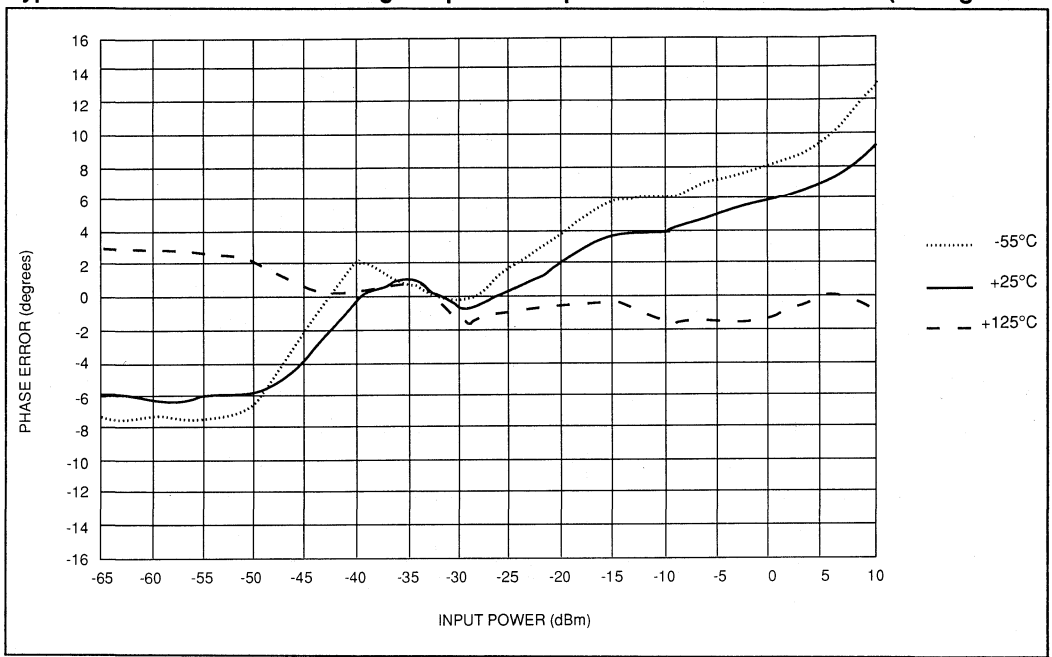


Fig. 22 Phase deviation vs CW input level (normalised at -30dBm) at 450MHz across temperature

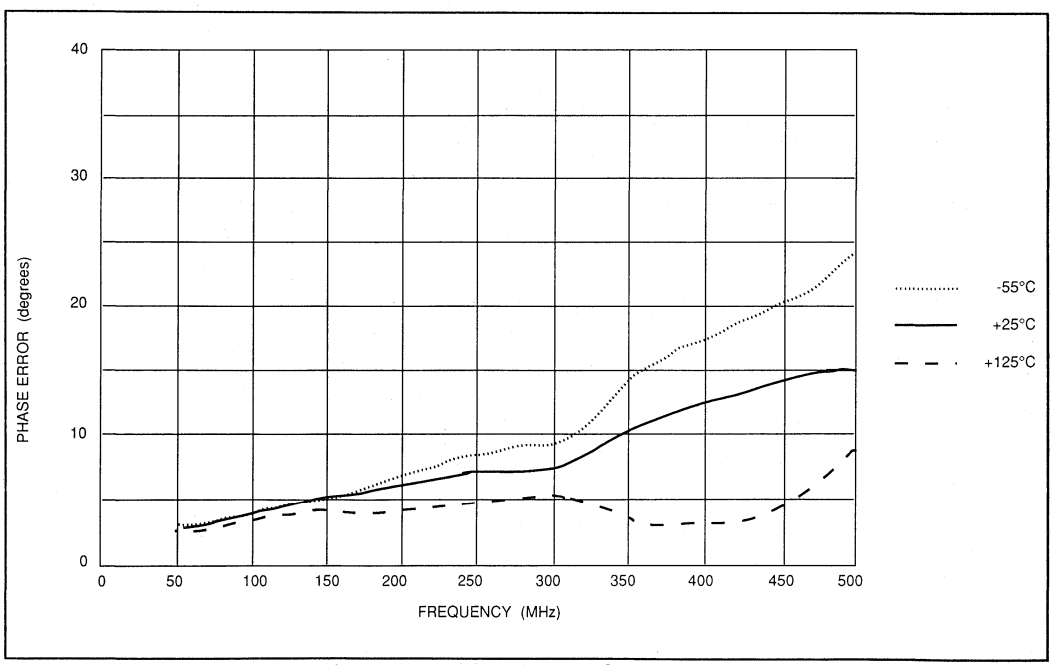


Fig. 23 Peak phase deviation over -65dBm → +10dBm CW input level vs CW input frequency. Across temperature

SL3145

1.6GHz NPN TRANSISTOR ARRAYS

The SL3145 is a monolithic array of five high frequency low current NPN transistors. The SL3145 consists of 3 isolated transistors and a differential pair in a 14 lead SO package The transistors exhibit typical frs of 1.6GHz and wideband noise figures of 3.0dB The device is pin compatible with the CA3046.

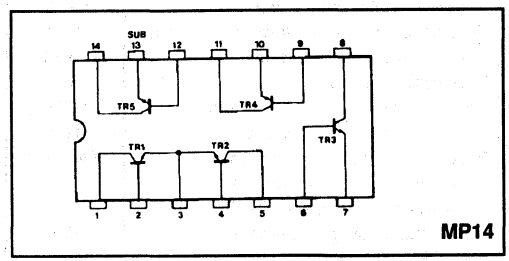


Fig.1 Pin connections SL3145

FEATURES

- f_T Typically 1.6GHz
- Wideband Noise Figure 3.0dB
- V_{BE} Matching Better Than 5mV

APPLICATIONS

- Wide Band Amplifiers
- PCM Regenerators
- High Speed Interface Circuits
- High Performance Instrumentation Amplifiers
- High Speed Modems

ORDERING INFORMATION

SL3145 C MP

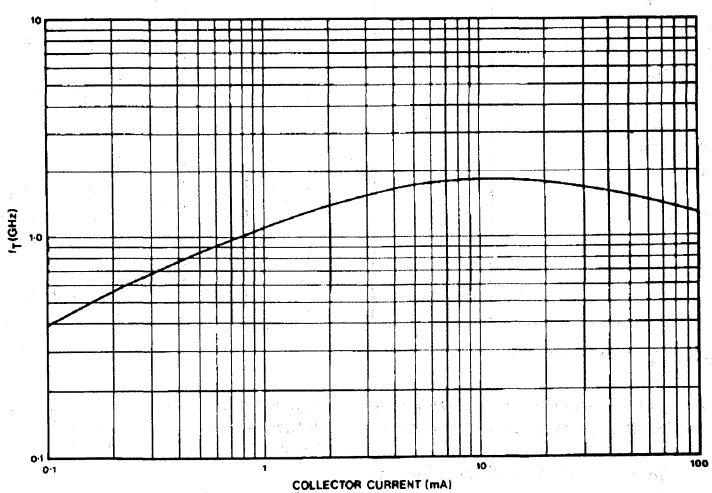


Fig.2 Transition frequency (f_T) v. collector current (V_{CB}= 2V, f=200MHz)

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following test conditions (unless otherwise stated)

T_{amb} = 22°C ± 2°C

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Static characteristic						
Collector base breakdown	BV_{CBO}	20	30		V	I_C = 10µA, I_E = 0
Collector emitter breakdown	LV_{CEO}	15	18		V	I_C = 1mA, I_B = 0
Collector substrate breakdown (isolation)	BV_{CIO}	20	55		V	I_C = 10µA, I_R = I_E = 0
Base to isolation breakdown	BV_{BIO}	10	20		V	I_B = 10µA, I_C = I_E = 0
Base emitter voltage	V_{BE}	0.64	0.74	0.84	V	V_{CE} = 6V, I_C = 1mA
Collector emitter saturation voltage	$V_{CE}(SAT)$		0.26	0.5	V	I_C = 10mA, I_B = 1mA
Emitter base leakage current	I_{EBO}		0.1	1	µA	V_{EB} = 4V
Base emitter saturation voltage	$V_{BE}(SAT)$		0.95		V	I_C = 10mA, I_B = 1mA
Base emitter voltage difference, all transistors expect TR1, TR2	ΔV_{BE}		0.45	5	mV	V_{CE} = 6V, I_C = 1mA
Base emitter voltage difference TR1, TR2	ΔV_{BE}		0.35	5	mV	V_{CE} = 6V, I_C = 1mA
Input offset current (except for TR1, TR2)	ΔI_B		0.2	3	µA	V_{CE} = 6V, I_C = 1mA
Input offset current TR1, TR2	ΔI_B		0.2	2	µA	V_{CE} = 6V, I_C = 1mA
Temperature coefficient of ΔV_{BE}	$\frac{\partial \Delta V_{BE}}{\partial T}$		2.0		µV/°C	
Temperature coefficiient of V_{BE}	$\frac{\partial V_{BE}}{\partial T}$		-1.6		mV/°C	V_{CE} = 6V, I_C = 1mA
Static forward current ratio	H_{FE}	40	100			V_{CE} = 6V, I_C = 1mA
Collector base leakage	I_{CBO}		0.3		nA	V_{CB} = 16V
Collector isolation leakage	I_{CIO}		0.6		nA	V_{CI} = 20V
Base isolation leakage	I_{BIO}		100		nA	V_{BI} = 5V
Emitter base capacitance	C_{EB}		0.4		pF	V_{EB} = 0V
Collector base capacitance SL3145	C_{CB}		0.4		pF	V_{CB} = 0V
Collector isolation capacitance	C_{CI}		0.8		pF	V_{CI} = 0V
Dynamic characteristics						
Transition frequency SL3145	f_T		1.6		GHz	V_{CE} = 6V, I_C = 5mA
Wideband noise figure	NF		3.0		dB	V_{CE} = 2V, R_S = 1kΩ I_C = 100µA, f = 60MHz
Knee of 1/f noise curve			1		KHz	V_{CE} = 6V, R_S = 200Ω I_C = 2mA

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

All electrical ratings apply to individual transistors. Thermal ratings apply to the total package.

The isolation pin (substrate) must be connected to the most negative voltage applied to the package to maintain electrical isolation.

V_{CB} = 20 volt
V_{EB} = 4.0 volt
V_{CE} = 15 volt
V_{CI} = 20 volt
I_C = 20 mA

Maximum individual transistor dissipation 200 mWatt
Storage temperature -55°C to 150°C
Max junction temperature 150°C

Package thermal resistance (°C/watt):-

Package Type	**MP14**
Chip to case	45°C/W
Chip to ambient	123°C/W

NOTE:
If all the power is being dissipated in one transistor, these thermal resistance figures should be increased by 100°C/watt

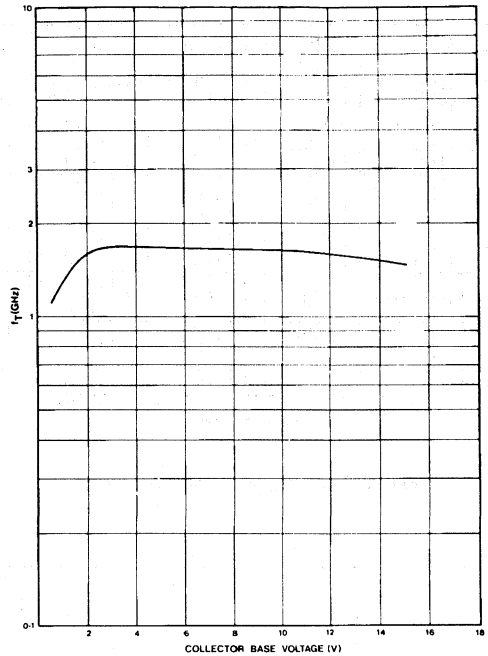


Fig.3 Transition frequency (f_T) v. collector base voltage (I_C = 5mA, Frequency = 200MHz)

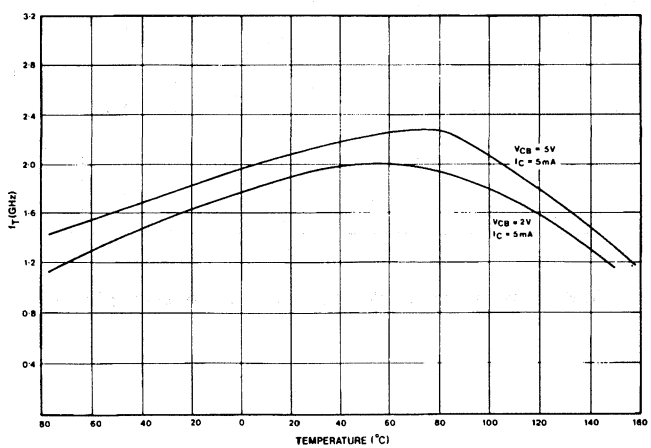


Fig.4 Variation of transition frequency (f_T) with temperature

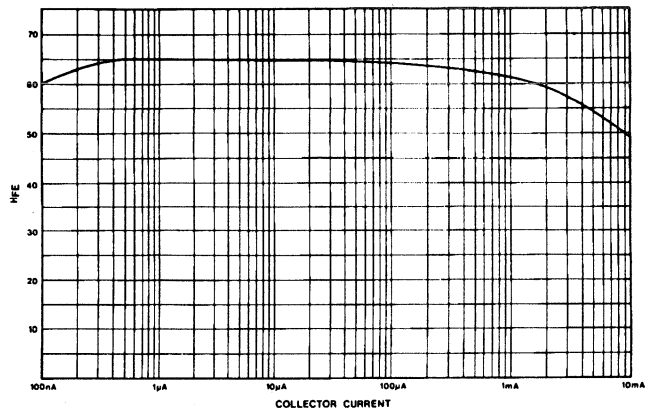


Fig.5 DC current gain v. collector current

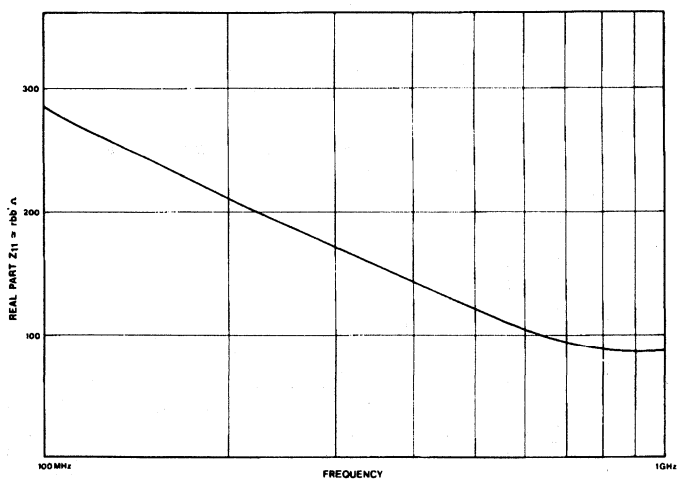


Fig.6 Z_{11} (derived from scattering parameters) v. frequency ($Z_{11} \backsim r_{bb}$)

SL3227

3GHz NPN TRANSISTOR ARRAYS

The SL3227 is a monolithic array of the five high frequency low current NPN transistors in a 16 lead DIL package. The transistors exhibit typical fT of 3GHz and wideband noise figures of 2dB. The SL3227 is pin compatible with the CA3127 and SL3127.

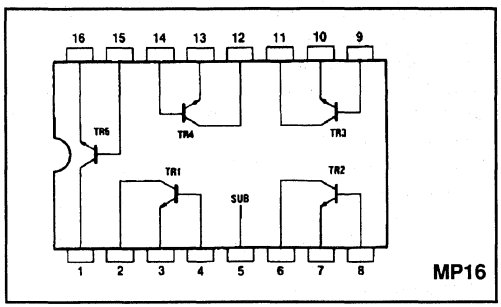


Fig.1 Pin connections - SL3227

FEATURES

- f_T Typically 3GHz
- Wideband Noise Figure 2.0dB
- V_{BE} Matching Better Than 5mV

APPLICATIONS

- Wide Band Amplifiers
- PCM Regenerators
- High Speed Interface Circuits
- High Performance Instrumentation Amplifiers
- High Speed Modems

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

All electrical ratings apply to individual transistors. Thermal ratings apply to the total package.

The isolation pin (substrate) must be connected to the most negative voltage applied to the package to maintain electrical isolation.

V_{CB} = 10 volt
V_{EB} = 2.5 volt
V_{CE} = 6 volt
V_{CI} = 15volt
I_C = 20 mA
Maximum individual transistor dissipation 200 mWatt
Storage temperature -55°C to +150°C
Max junction temperature +150°C

Package thermal resistance (°C/watt)

Package Type	MP16
Chip to case	111
Chip to ambient	41

NOTE:If all the power is being dissipated in one transistor, these thermal resistance figures should be increased by 100°C/watt

ORDERING INFORMATION

SL3227 NA MP

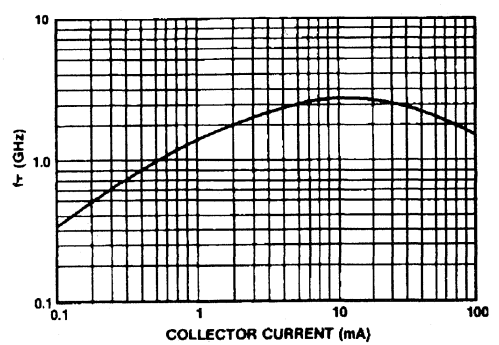


Fig.2 Transition frequency (f_T) v. collector current (V_{CB}= 2V, f=200MHz)

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following test conditions (unless otherwise stated)

T_{amb} = 22°C ± 2°C

Static Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Collector base breakdown	BV_{CBO}	10	20		V	I_C = 10µA
Collector isolation breakdown	BV_{CIO}	16	40		V	I_C = 10µA
Base emitter breakdown	BV_{EBO}	2.5	5.0		V	I_E = 10µA
Collector emitter breakdown	LV_{CEO}	6	9		V	I_C = 5mA
Collector emitter saturation voltage	$V_{CE(SAT)}$		0.22	0.5	V	I_C = 10mA, I_B = 1mA
Base emitter voltage	V_{BE}	0.73	0.78	0.81	V	V_{CE} = 2V, I_C = 1mA
Base emitter voltage difference, all transistors	ΔV_{BE}		0.45	5.0	mV	V_{CE} = 2V, I_C = 1mA
Input offset current	ΔI_B		0.2	3	µA	V_{CE} = 2V, I_C = 1mA
Temperature coefficient of V_{BE}	$\frac{\Delta V_{BE}}{T}$		-1.69		mV/°C	V_{CE} = 2V, I_C = 1mA
Static forward current ratio	H_{fe}	35	80			V_{CE} = 2V, I_C = 5mA
		35	95			V_{CE} = 2V, I_C = 0.1mA
		40	85			V_{CE} = 2V, I_C = 1mA
Emitter base leakage	I_{EBO}		15		nA	V_{EB} = 2V
Collector base leakage	I_{CBO}		5		pA	V_{CB} = 10V
Collector isolation leakage	I_{CIO}		5		pA	V_{CI} = 16V
Emitter base capacitance	C_{EB}		0.7		pF	V_{EB} = 0V
Collector base capacitance	C_{CB}		0.4		pF	V_{CI} = 0V
Collector isolation capacitance	C_{CI}		1.5	2.0	pF	V_{CI} = 0V

Dynamic Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Transition frequency	f_T		3		GHz	V_{CE} = 2V, I_C = 5mA
Wideband noise figure	NF		2.0		dB	f = 60MHz V_{CC} = 6V
Knee of NF noise curve			1		KHz	I_C = 1mA
						R_S = 1kΩ

SL3245

3GHz NPN TRANSISTOR ARRAY

The SL3245 is a monolithic array of five high frequency low current NPN transistors. The SL3245 consists of 3 isolated transistors and a differential pair in a 14 lead SO package. The transistors exhibit typical f_T of 3GHz and wideband noise figures of 2dB. The device is pin compatible with the SL3045 and SL3145.

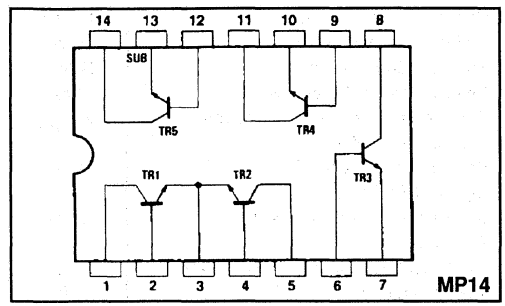


Fig.1 Pin connections - SL3245

FEATURES

- f_T Typically 3GHz
- Wideband Noise Figure 2.0dB
- V_{BE} Matching Better Than 5mV

APPLICATIONS

- Wide Band Amplifiers
- PCM Regenerators
- High Speed Interface Circuits
- High Performance Instrumentation Amplifiers
- High Speed Modems

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

All electrical ratings apply to individual transistors. Thermal ratings apply to the total package.

The isolation pin (substrate) must be connected to the most negative voltage applied to the package to maintain electrical isolation.

V_{CB} = 10 volt
V_{EB} = 2.5 volt
V_{CE} = 6 volt
V_{CI} = 15 volt
I_C = 20 mA
Maximum individual transistor dissipation 200 mWatt
Storage temperature -55°C to +150°C
Max junction temperature +150°C

Package thermal resistance (°C/watt)

Package Type	MP14
Chip to case	45
Chip to ambient	123

NOTE:If all the power is being dissipated in one transistor, these thermal resistance figures should be increased by 100°C/watt

ORDERING INFORMATION

SL3245 NA MP

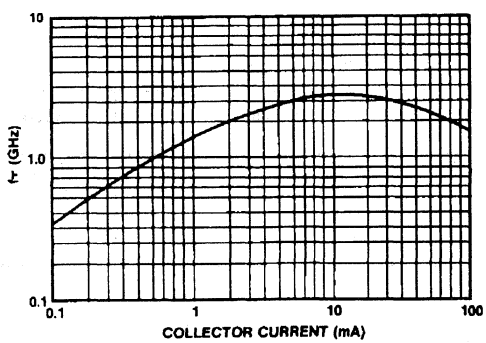


Fig.2 Transition frequency (f_T) v. collector current (V_{CB}= 2V, f=200MHz)

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following test conditions (unless otherwise stated)

T_{amb} = 22°C ± 2°C

Static Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Collector base breakdown	BV_{CBO}	10	20		V	I_C = 10µA
Collector isolation breakdown	BV_{CIO}	16	40		V	I_C = 10µA
Base emitter breakown	BV_{EBO}	2.5	5.0		V	I_E = 10µA
Collector emitter breakdown	LV_{CEO}	6	9		V	I_C = 5mA
Collector emitter saturation voltage	$V_{CE(SAT)}$		0.22	0.5	V	I_C = 10mA, I_B = 1mA
Base emitter voltage	V_{BE}	0.73	0.78	0.81	V	V_{CE} = 2V, I_C = 1mA
Base emitter voltage difference (except TR1, TR2)	ΔV_{BE}		0.45	5.0	mV	V_{CE} = 2V, I_C = 1mA
Base emitter voltage diference TR1, TR2	ΔV_{BE}		0.33	5.0	mV	V_{CE} = 2V, I_C = 1mA
Input offset current (except TR1, TR2)	ΔI_B		0.2	3	µA	V_{CE} = 2V, I_C = 1mA
Input offset current TR1, TR2	ΔI_B		0.2	2	µA	V_{CE} = 2V, I_C = 1mA
Temperature coefficient of V_{BE}	$\frac{\Delta V_{BE}}{T}$		-1.69		µV/°C	V_{CE} = 2V, I_C = 1mA
Static forward current ratio	H_{fe}	35	80			V_{CE} = 2V, I_C = 5mA
		35	95			V_{CE} = 2V, I_C = 0.1mA
		40	85			V_{CE} = 2V, I_C = 1mA
Emitter base leakage	I_{EBO}		10		nA	V_{EB} = 2V
Collector base leakage	I_{CBO}		5		pA	V_{CB} = 10V
Collector isolation leakage (TR1-TR4)	I_{CIO}		10		pA	V_{CI} = 16V
Collector isolation leakage (TR5)	I_{CIO}		10		pA	V_{CI} = 5V
Emitter base capacitance	C_{EB}		0.4		pF	V_{EB} = 0V
Collector base capacitance	C_{CB}		0.4		pF	V_{CI} = 0V
Collector isolation capacitance	C_{CI}		1.4	2.0	pF	V_{CI} = 0V

Dynamic Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Transition frequency	f_T		3		GHz	V_{CE} = 2V, I_C = 5mA
Wideband noise figure	NF		2.0		dB	f = 60MHz V_{CC} = 6V
						I_C = 1mA
Knee of NF noise curve			1		kHz	R_S = 1kΩ

SL3522

500MHz 75dB LOGARITHMIC / LIMITING AMPLIFIER

(Supersedes Edition in Professional Products IC Handbook May 1991)

The SL3522 is a monolithic seven stage successive detection logarithmic amplifier integrated circuit for use in the 100MHz to 500MHz frequency range. It features an on–chip video amplifier with provision for external adjustment of log slope and offset. It also features a balanced RF output. The SL3522 operates from supplies of ±5V.

FEATURES

- 75dB Dynamic Range
- Surface Mount SO Package
- Adjustable Log Slope and Offset
- 0dBm RF Limiting Output
- 60dB Limiting Range
- 2V Video Output Range
- Low Power (Typ. 1W)
- Temperature Range (T_{CASE}): –55°C to +125°C

APPLICATIONS

- Ultra Wideband Log Receivers
- Channelised and Monopulse Radar
- Instrumentation

ABSOLUTE MAXIMUM RATINGS

Supply voltages	±6.0V
Storage temperature	–65°C to +175°C
Junction temperature	+175°C
Thermal resistance	
Die–to–case	15.5°C/W
Die–to–ambient	76.5°C/W
Applied DC voltage to RF input	±400mV
Applied RF power to RF input	+15dBm

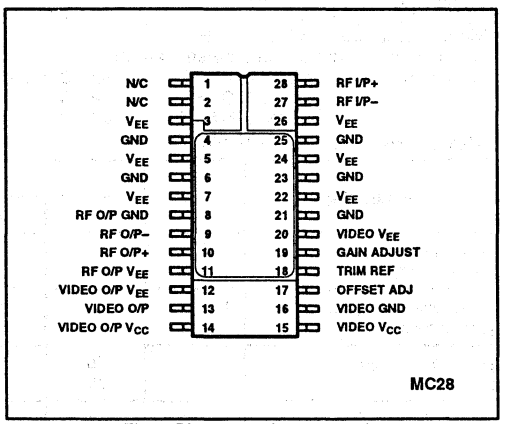


Fig. 1 Pin connections – top view

ORDERING INFORMATION

SL3522 A MC (Miniature Ceramic package)
SL3522 C MC (Miniature Ceramic package)
SL3522 NA 1C (Probe–tested bare die)
(Also available: SL3522 AA MC screened to GPS HI–REL level A. Contact GPS sales outlet for a separate data sheet.)

ESD PROTECTION

To achieve the high frequency performance there are no ESD protection structures on the RF input pins (27, 28). These pins are **highly static sensitive**, typically measured as 250V using MIL–STD–883 method 3015. Therefore, ESD handling precautions are **essential** to avoid degradation of performance or permanent damage to this device.

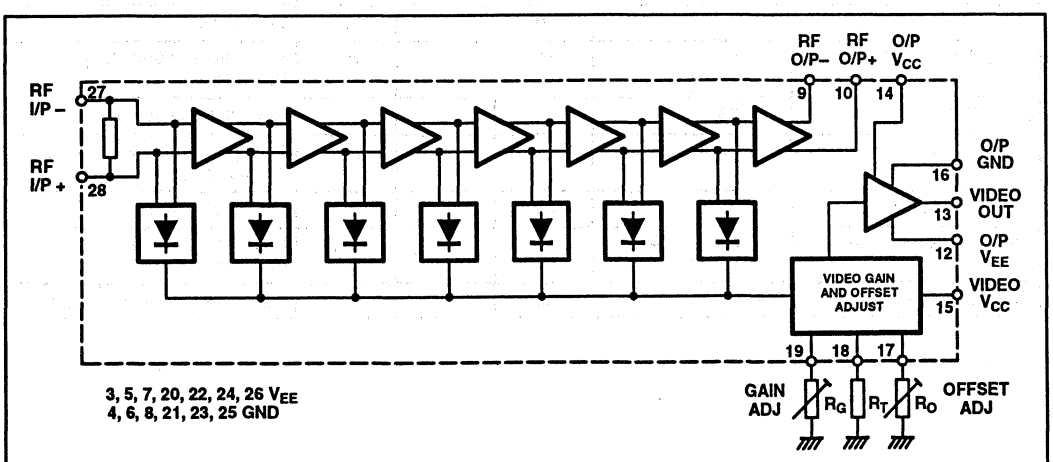


Fig. 2 Functional block diagram

ELECTRICAL CHARACTERISTICS

The electrical characteristics are guaranteed over the following range of operating conditions, using test circuit in Fig. 3 (unless otherwise stated):

Temperature range: Military: SL3522 A MC, SL3522 NA 1C 55°C to +125°C (T_{CASE})
Commercial: SL3522 C MC 0°C to +70°C (T_{CASE})
Supply voltage: V_{CC}: +4.50V to +5.50V (all grades)
V_{EE}: −4.5V to −5.50V (all grades)
Frequency =100MHz to 500MHz
Rg, Ro, Rt =1.5KΩ
Video output load =200Ω//20pF

Test conditions (unless otherwise stated):

Temperature: SL3522 A MC: +25°C, +125°C & −55°C (T_{CASE})
SL3522 C MC: +25°C
SL3522 NA 1C +25°C
Supply voltage: V_{CC} = +5.0V, V_{EE} = −5.0V

Parameter	Pin	Value			Units	Conditions
		Min	Typ	Max		
Positive supply current (quiescent)	14, 15		28	35	mA	V_{CC}= +5.0V
Negative supply current (quiescent)	ALL V_{EE} Pins		150 180	175 210	mA mA	V_{EE}= −5.0V See note 1 V_{EE}= −5.0V See note 2
Dynamic range		75 70			dB dB	100 to 400MHz See note 1, 3 See note 1, 4
Linearity		−1 −1 −1.25		+1 +1 +1.25	dB dB dB	T_{CASE} = −55°C T_{CASE} = +25°C T_{CASE} =+125°C
Video output range	13	1.30	1.75	2.00	V	
Video slope	13	18	21	24	mV/dB	
Video slope variation	13	−5		+5	%	See note 5
Video slope adjust range	13	±20	±30		%	R_G=1kΩ to 2.2kΩ
Video offset	13	−0.1	+0.25	+0.5	V	
Video offset variation	13		−0.5		mV/°C	T_{CASE}=+25°C
Video offset adjust range	13	±0.5			V	R_O=1kΩ to 2.2kΩ
Video trim reference voltage	17, 18, 19	−0.59	−0.54	−0.49	V	
Video output impedance	13		10		Ω	See note 8
Video rise time	13		16		ns	10% − 90% (60dB step) See note 7
Input VSWR	27, 28		1.5:1			Zs = 50Ω See note 7
RF bandwidth	9, 10		450		Mhz	T_{CASE} = +25°C RF_{IN} = −70dBm See notes 2, 7
RF limiting range	9, 10		60		dB	See notes 2, 6, 7
RF limited output level	9, 10	−3.0	−1.0	+1.0	dBm	R1 = 50Ω single ended See note 2
RF output impedance	9, 10		50		Ω	Single ended See notes 2, 8

ELECTRICAL CHARACTERISTICS(cont.)

Parameter	Pin	Value			Units	Conditions
		Min	Typ	Max		
Phase variation with RF input level			15		Degrees	Freq = 300MHz RF_{IN} = –60 to +10dBm See notes 2, 7
Phase tracking between units			3		Degrees	T_{CASE} = +25°C FREQ=300MHz See notes 2, 7

Notes
1. RF output buffer OFF (pin 8 disconnected from 0V)
2. RF output buffer ON (pin 8 connected to 0V)
3. Minimum dynamic range under any single set of operating conditions
4. Log linearity guaranteed for pin = –64dBm to +6dBm for ALL supply, temperature and frequency conditions
5. Full range of supply, temperature and frequency conditions
6. Input limiting range typically –50dBm to +10dBm
7. Not tested, but guaranteed by characterisation
8. Not tested, but guaranteed by design

The SL3522 CANNOT be GUARANTEED to operate below 100MHz and meet the electrical characteristics shown above. However, characterisation has shown that the device can still function adequately down to frequencies of 50MHz, with the following reservations:–

1) The video bandwidth is fixed to approx 40MHz a certain amount of carrier breakthrough on the video O/P (pin 13) will occur, with input signal frequencies below 100MHz.

2) There are 2 RF coupling capacitors (20pF) on–chip, which couple the output signal from stage 3 to the input of stage 4 (ref Fig. 24). These can introduce undesirable limiting phase performance for input signal frequencies below 100MHz.

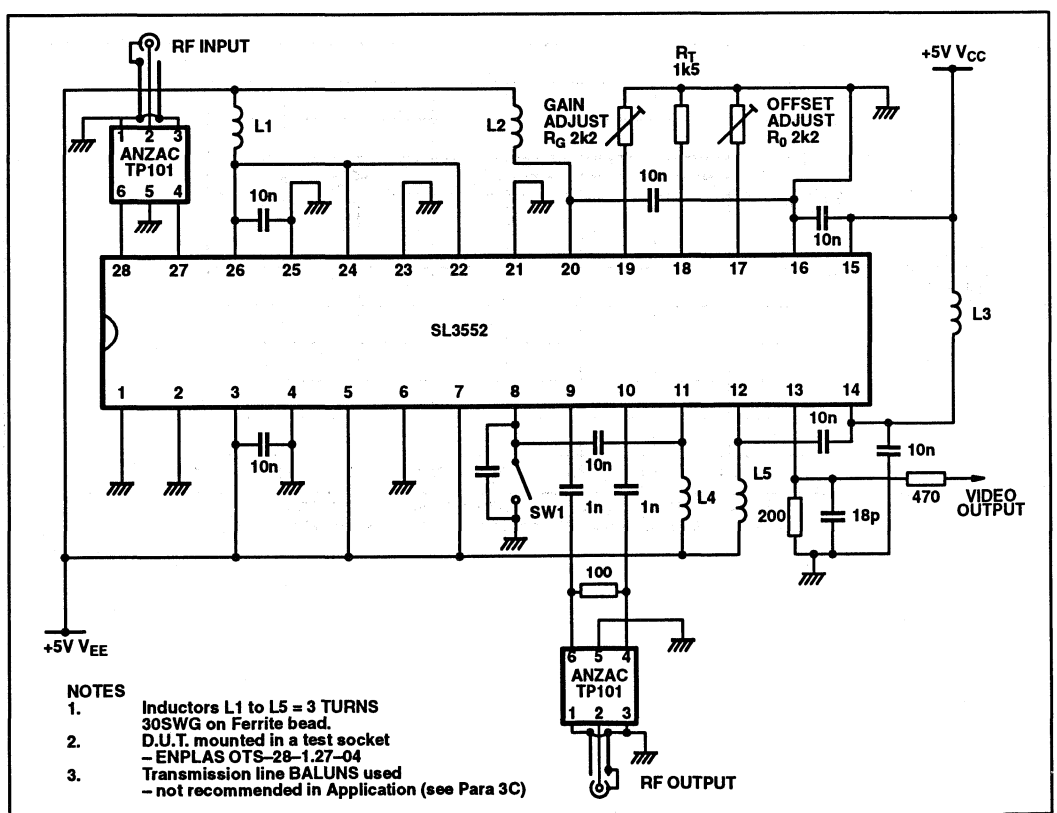


Fig. 3 Test circuit

PRODUCT DESCRIPTION

The SL3522 is a complete monolithic successive detection Log/limiting amplifier which can operate over an input frequency range of 100MHz to 500MHz. Producing a log/lin characteristic for input signals between –64dBm and +6dBm, the log amplifier can provide an accuracy of better than ±1.00dB at case temperatures of –55°C and +25°C and an accuracy of better than ±1.25dB at +125°C. The dynamic range is better than 75dB over a frequency range of 100MHz to 400MHz. The graph in fig 4 shows how the dynamic range is guaranteed over frequency.

The SL3522 consists of 6 Gain stages, 7 Detector stages, a limiting RF Output buffer and a Video Output amplifier. The power supply connections to each section are isolated from each other to aid stability.

The SL3522 consumes 1.1W of power when ALL parts of the circuit are powered up from a ± 5.0V power supply. As the circuit uses a differential architecture, the power consumption of the RF gain/detector stages and RF Output Buffer will be independent of RF input signal level. However, the Video Output (pin 13) is driven by a single ended emitter follower and so the power consumption of the Video amplifier will vary with RF input signal level between pins 27 and 28.(upto 10mA over 2V video output range with max video load of 200Ω//20pF)

The SL3522 has a high RF gain (>50dB) across a wide bandwidth (>450MHz) when the limiting RF Output Buffer is enabled. The limiting RF Output Buffer provides a balanced Limited Output level of nominally –1.0dBm on each RF Output connection (pin 9 and 10), for RF input signal levels on pins 27 and 28 in excess of –50dBm.

The limiting RF Output Buffer can be isolated from the other sections of the SL3522, by disconnecting the RF Output Buffer GND (pin 8) from 0V, and leave the pin floating. This feature aids stability in applications NOT requiring a Limited RF Output signal, and lowers the power consumption of the SL3522 to 0.95Watts, when the other sections are powered up from a± 5.0V power supply.

Each of the Gain and Detector stages has approximately 12dB of gain, and a significant amount of on–chip RF decoupling (200pF per stage), also to aid stability.

The Video amplifier provides a positive going output signal proportional to the log of the amplitude of an RF input applied between pins 27 and 28. The gain and the offset of the Video amplifier can be adjusted by 3 resistors; R_G, R_T, and R_O which are connected to Gain adjust (pin 19), Trim reference (pin 18) and Offset adjust (pin 17). With R_T set to 1.5kΩ, Rg can be set to any value between 1kΩ and 2k2Ω and achieve a range in Video Slope of ± 20%, centred on 21mV/dB. Similarly, R_O can be set to any value between 1kΩ and 2.2KΩ and achieve an offset range of ± 0.5V, which should allow the Video Offset to be trimmed to 0V if required.

The RF input pins (27 and 28) have a 50Ω terminating resistor connected between them on–chip. These are capacitively coupled to the I/P gain stage with 20pF on–chip capacitors. (Refer to APPLICATION NOTES section for information on how to connect an RF input signal to the device).

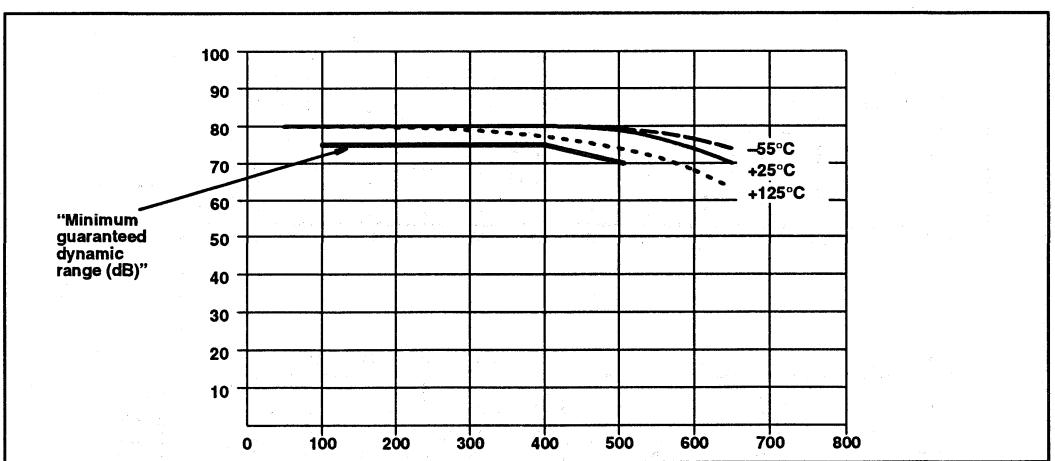


Fig. 4 Plot showing guaranteed dynamic range v. frequency (typical achievable dynamic range lines indicated across temperature)

APPLICATION NOTES

1) VIDEO–AMPLIFIER

The SL3522 uses a single ended Video amplifier to produce a trimmable Video transfer characteristic. Both the gain (Slope) and Offset of the amplifier can be externally adjusted.

a) Gain and Offset trimming (ref Applications circuits in figs 5 and 6)

The Gain and Offset control is achieved by adjusting R_G and R_O respectively. The control is dependent upon their difference from the Trim reference resistor, R_T.

Adjustment of Gain has an effect on Offset, but adjustment of Offset does NOT affect the Gain. Therefore the Gain should be optimised first. The Offset should only be adjusted once the Gain has been set.

Fig 7 shows the variation of Video Offset with value of R_O, for a fixed value of R_T and R_G = 1k5Ω.

Fig 8 shows the variation of Video Slope with value of R_g, for a fixed value of R_T and R_O = 1k5Ω.

The Video amplifier incorporates temperature compensation for Video gain (Slope). To ensure temperature stability for Video gain (Slope) over the operating temperature range, it is recommended that the resistors with identical temperature coefficients of resistance are used for R_T and R_G.

The Video amplifier does NOT incorporate temperature compensation for Video Offset. Although it is recommended that a resistor with identical temperature coefficient of resistance to R_T be used for R_O, it may be necessary to use an additional external temperature compensating network.

b) Video performance

The Video–amplifier has a critically damped rise time of 16ns (10% – 90%).In order to achieve this transient performance, it is important to ensure that:–

i) the resistor connected to Trim reference (pin 18), has a nominal resistance of 1.5kΩ, with a parasitic capacitance LESS than 5pF.

ii) the load applied to the Video Output (pin 13) does NOT exceed 200Ω resistance in parallel with 20pF.

Also, the following decoupling should be incorporated:–

i) The Video Output V_{CC} (pin 14) should be decoupled with a 10nF capacitor to the RETURN line from the video load, connected to Video GND (pin 16), avoiding any common impedance path.

ii) The Video Output Vee (pin 12) should be decoupled with a 10nF capacitor DIRECTLY to Video–Output Vcc (pin 14).

2) SL3522 AS A LOG AMPLIFIER with RF output buffer disabled (pin 8 floating)

If the SL3522 is to be used as a Logarithmic successive detection amplifier only, with no requirement for a limited RF Output, the RF input (pins 27 and 28) can be driven EITHER differentially or single ended from a 50Ω source. If being used with a single ended input, the SIGNAL should be applied to pin 27 and the RETURN should be connected to pin 28, as shown in the Application circuit diagram in Fig 5.

The SL3522 is VERY stable when used in this way. Although not a crucial requirement, it is recommended that the device should be mounted using a ground plane.

3) SL3522 AS A LOG/LIMITING AMPLIFIER – with RF Output–Buffer ENABLED (pin 8 connected to GND)

If the SL3522 is to be used as a Limiting or Log/limiting amplifier with a requirement for a Limited RF Output signal, care is required in the layout of components and connections around the device to ensure stability. The following precautions should be observed (refer to Application circuit diagram in Fig. 6):–

a) The device should be mounted on a ground plane, ensuring that the impedance between the ground plane and ALL the GND pins is kept as low as possible. If a multilayer PCB is used where the ground plane is connected to the GND pins using through–plated holes (vias), it is essential to ensure that the vias have a very low impedance. ALL supply decoupling capacitors should be RF chip capacitors whose leads should be kept as short as possible.

b) The RF V_{EE} connections (pins 3,5,7,11,20,22,24,26) should be connected to a low impedance copper plane. A two layer PCB should help to achieve this.

c) The RF input (pins 27 and 28) should be driven with a balanced source impedance. One way of achieving this is to use an **isolating** BALUN transformer (50Ω UNBALANCED → 50Ω BALANCED) connected between the signal source and the RF input pins. (e.g. Mini circuits TT1–6, TO –75). The device stability is VERY sensitive to an imbalance of the differential source impedance at pins 27 and 28. Use of a transmission line BALUN though, is NOT recommended.

d) The RF Output connections (pins 9 and 10) should each be loaded with matched impedances ideally 50Ω transmission lines. The RF Output lines leading away from the device should be balanced. Driving highly reactive SWR loads is NOT recommended as these can encourage device instability, as can an imbalance of the differential load impedance at pins 9 and 10.

e) The RF Output connections (pins 9 and 10) are DC coupled, and ideally the output pins should be capacitively coupled to their loads using 1nF capacitors. However the RF Outputs can drive a DC load to GND and a DC offset of approx. 400mV will exist on each RF Output pin. IT WILL NOT BE POSSIBLE TO DISABLE THE RF OUTPUT BUFFER UNDER THESE CONDITIONS.

f) The RF output (pins 9 and 10) has a tendancy to limit on self noise, particularly at low ambient temperatures (–55°C), when the RF output buffer is enabled.

NOTE that this will effect the liminting range as the gain of the RF output buffer will reduce as the amount of noise limiting increases.

If required the limited RF Output can be attenuated using an attenuation network as shown in fig. 9. Under these conditions the effective RF Output currents will be reduced, allowing the device to operate with a greater margin of stability.It may be possible to run the device without a BALUN transformer on the RF input if the total output impedance on the RF Output $\gg$ 50Ω, and the attenuation components are mounted as close as possible to the RF Output connections (pins 9 and 10). The RF input connection could then be configured as in Fig 5.

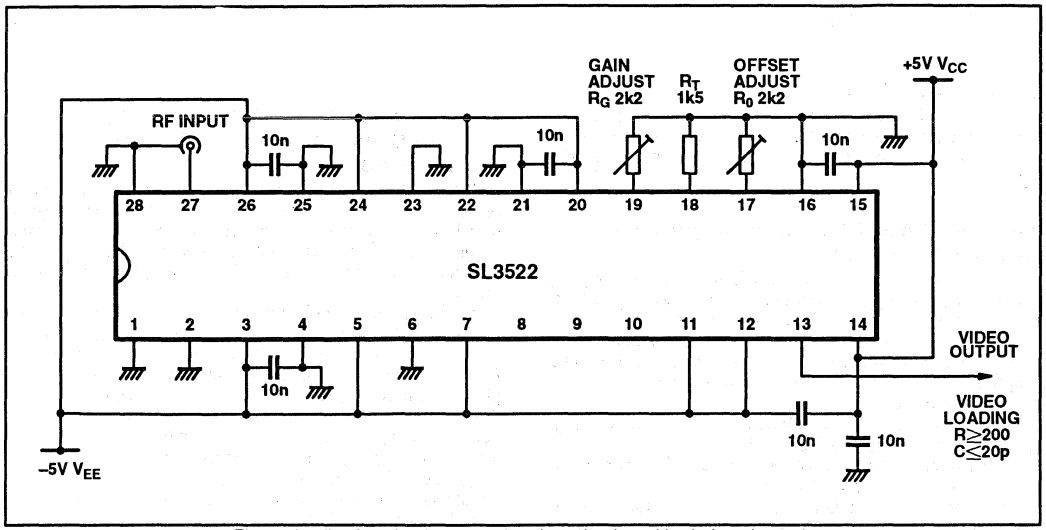


Fig. 5 Application circuit successive detection logarithmic function only

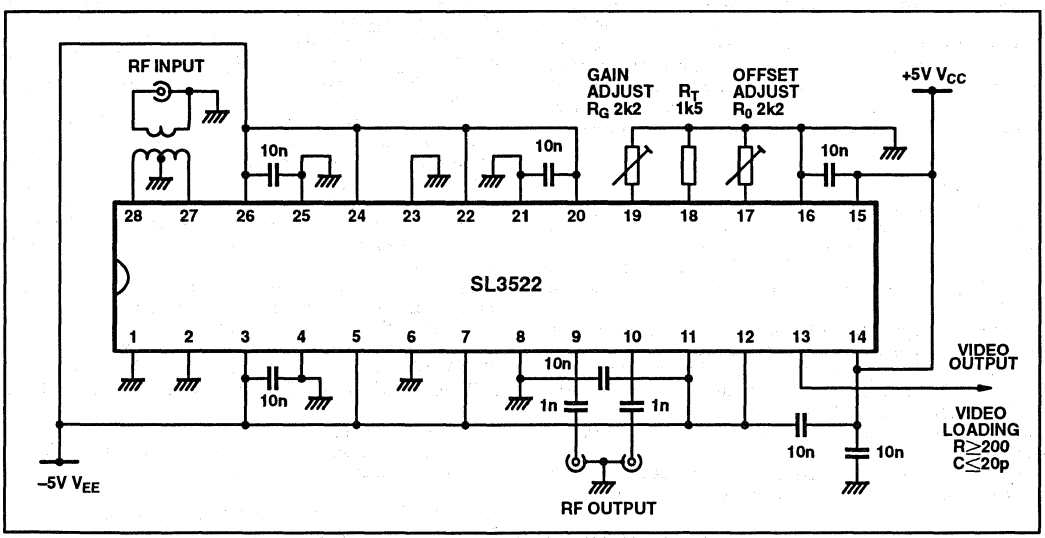


Fig. 6 Applications circuit – Log / Limiting function

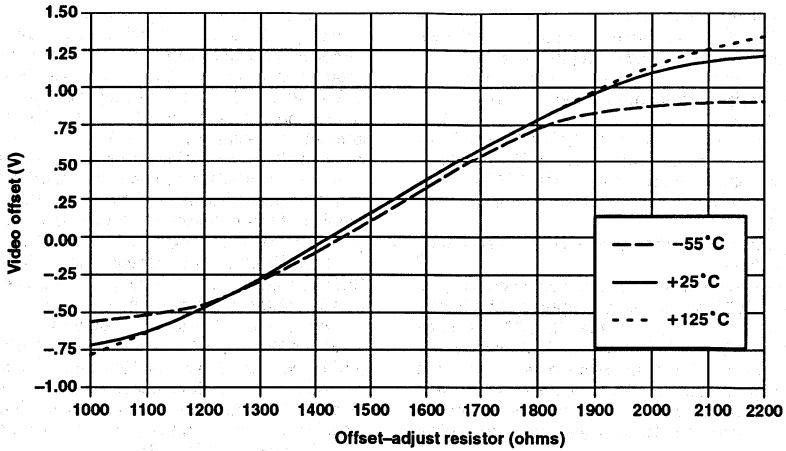


Fig. 7 Video offset v. offset–adjust resistor (pin17 to GND) across temperature

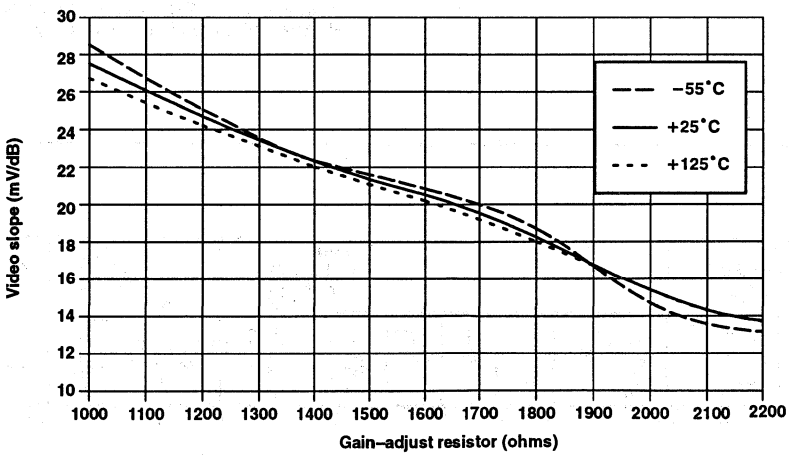


Fig. 8 Video slope v. gain–adjust resistor (pin19 to GND) across temperature

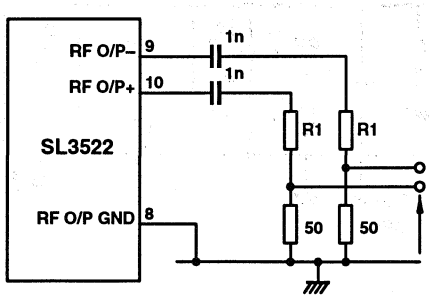


Fig. 9 Network for attenuating limited RF output

A PRACTICAL APPLICATION FOR THE SL3522 AS A LOG/LIMITING AMPLIFIER

The SL3522, with the RF Output–Buffer ENABLED, has a large limited RF Output level (0dBm on each of two RF Output pins (9 and10)) and a wide RF bandwidth (450MHz) in a small 28 pin Miniature Ceramic S.O package. As a result, there is a tendency for the device to become unstable unless care is used in the application.

The PCB layout for a "SL3522 DEMONSTRATION BOARD" in Fig. 11 has proved reliably stable. The PCB is a double layer Fibre epoxy board which uses SMDs where possible. A circuit diagram for the Demonstration PCB appears in Fig. 10.

The following points should be noted when this application is realised practically:–

1) A wire needs to connect the two pads connected to pins 14 and 15 of the SL3522, to allow +5V to appear at both pins.

2) ALL the GND connections to the SL3522 are made through the PCB to a Ground plane on the bottom side. It is important to ensure that the impedance of each of these connections is kept to an absolute minimum to prevent instability. If these connections are achieved using through plated holes, it is recommended that they are filled with solder to lower their impedance.

3) The PCB is configured to accept SMA, SMB or SMC connectors for the RF input, RF Output and Video Output connections. These can be changed if necessary to an alternative type, but it is vital to ensure that the ground plane is solidly connected to the Guard Ring which surrounds the RF Output tracks.

4) The PCB is configured to accept a small surface mounting DC isolating BALUN transformer (e.g VANGUARD VE43666, available from Vanguard Electronics Company Inc, 1480 West 178th St. GARDENA, C.A. 90248, U.S.A. Tel:– U.S.A. (213) 323 – 4100) to couple a signal into the RF input connections (pins 27 and 28). It is NOT recommended to attempt operating the SL3522 with the RF Output Buffer enabled, WITHOUT using an input BALUN, although it may be possible, provided the input source impedance to both pins 27 and 28 remains balanced. The centre tap of the secondary winding of the transformer should be soldered to the small ground plane on the upper side of the PCB.

5) The RF Output connection to the PCB is from pin 9 of the SL3522 only, with pin 10 being terminated on the PCB using a 51Ω resistor. It is important to ensure that both pin 9 and10 are terminated with equal impedances.

6) The RF Output Buffer can be enabled by soldering a link (LK) between pin 8 of the SL3522 and the adjacent guard track around the RF Output lines. Similarly, the buffer can be disabled by removing the same link. When the buffer is disabled, the following components can be omitted:–

1nF capacitors (C1, C2)

10nF capacitor (C8)

51Ω resistor (R_{FO})

7) The Slope (gain) and Offset of the Video Output can be adjusted using two 1kΩ trimmers, provision for which is included in the PCB layout.

The plots in Fig. 12 to fig. 23 are typical of the performance of SL3522 devices used with the PCB layout detailed in Fig.11.

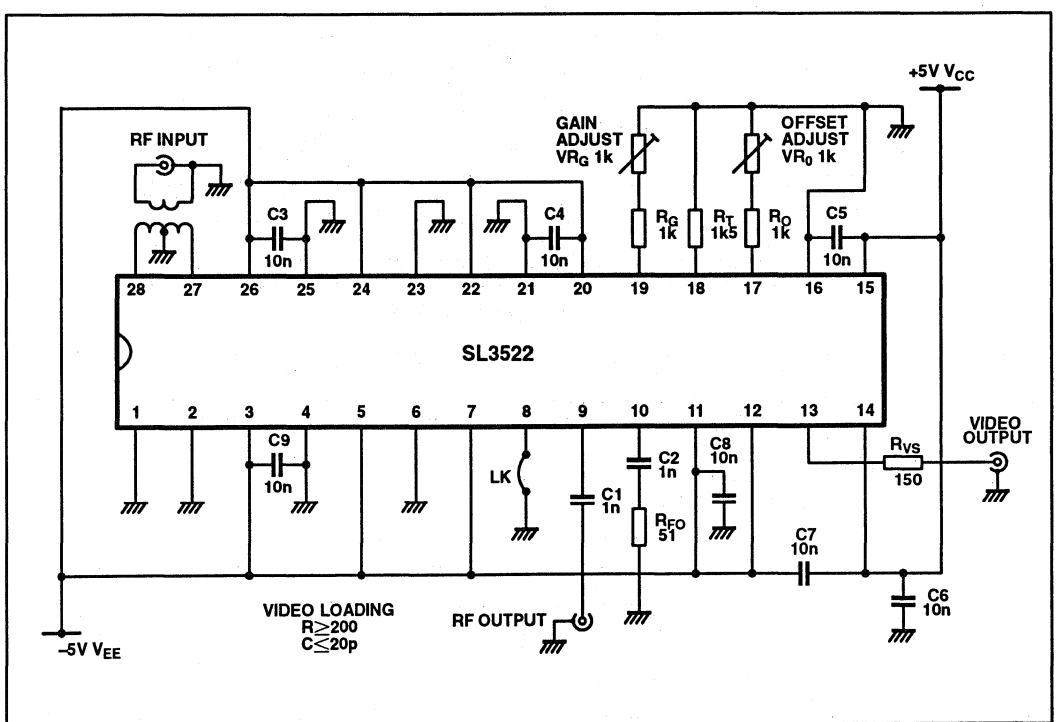
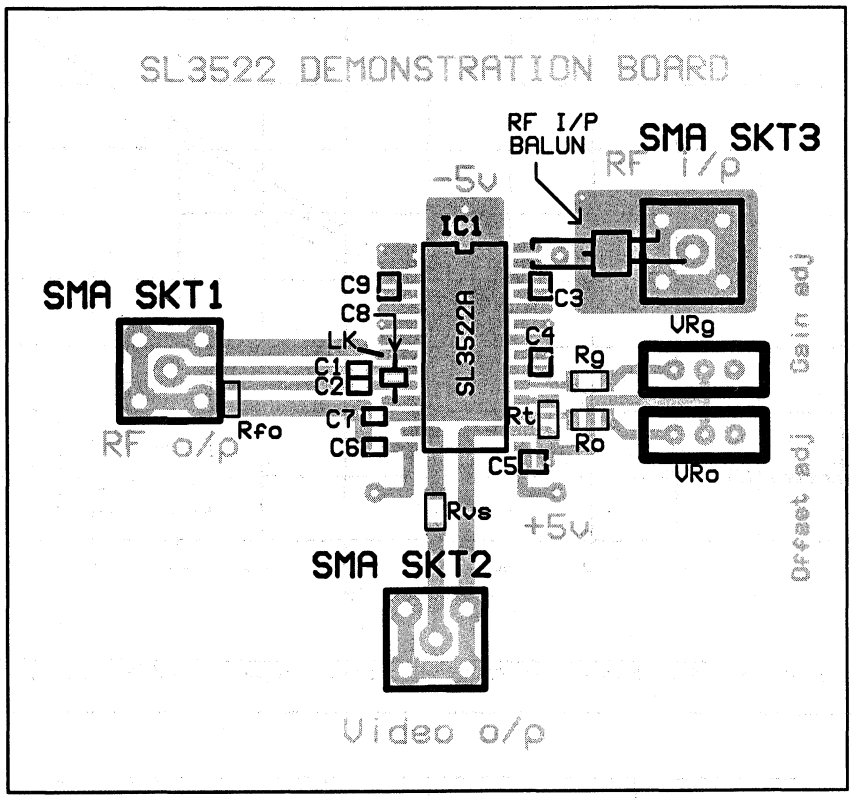


Fig. 10 SL3522 demonstration board circuit diagram



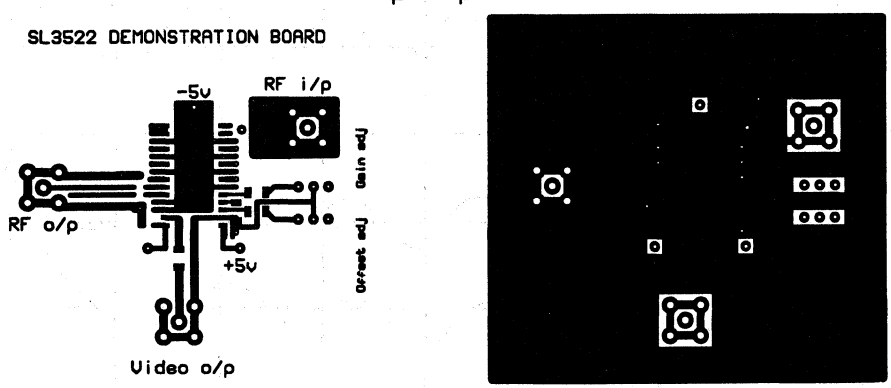


Fig. 11 Demonstration Circuit PCB showing component positions (2x full size) with top and bottom copper masks (full size)

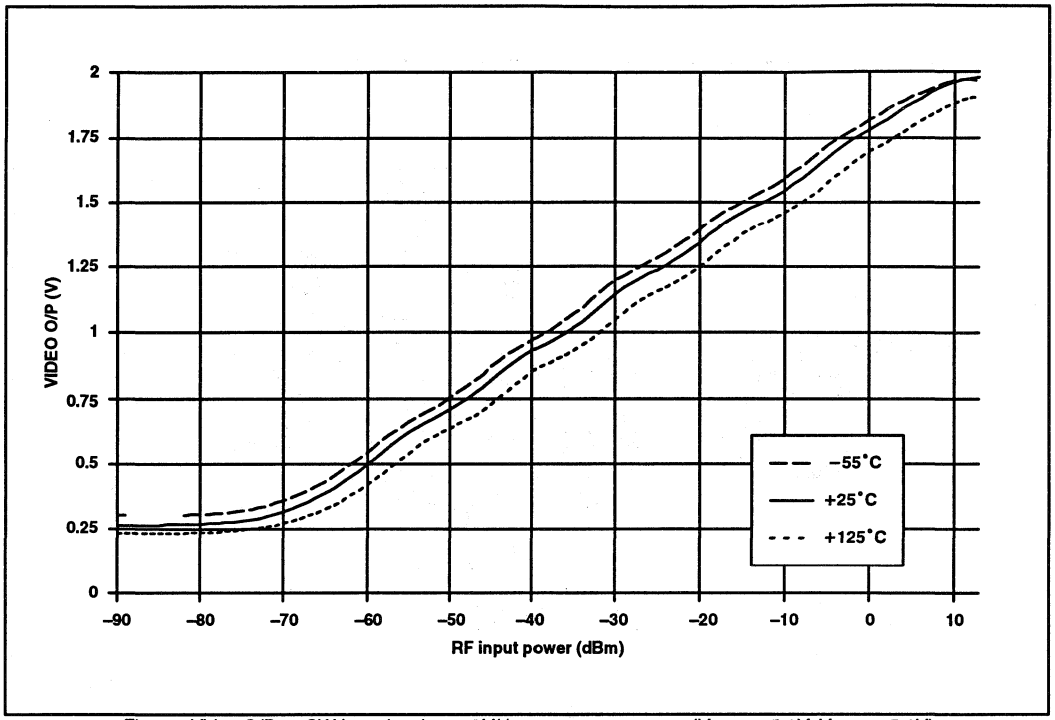


Fig. 12 Video O/P vs CW input level at 325MHz across temperature (V_{CC} = + 5.0V, V_{EE} = – 5.0V)

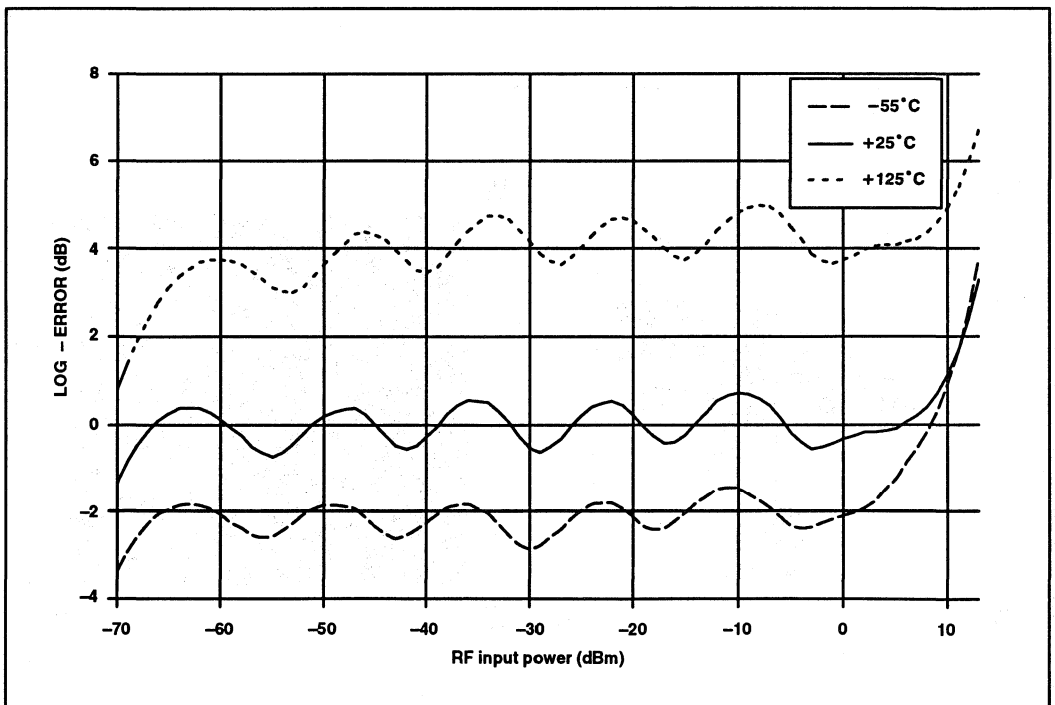


Fig. 13 Video O/P log–error, (referenced to single straight line measured at 325MHz, +25°C, 5.0V PSUs) across temperature

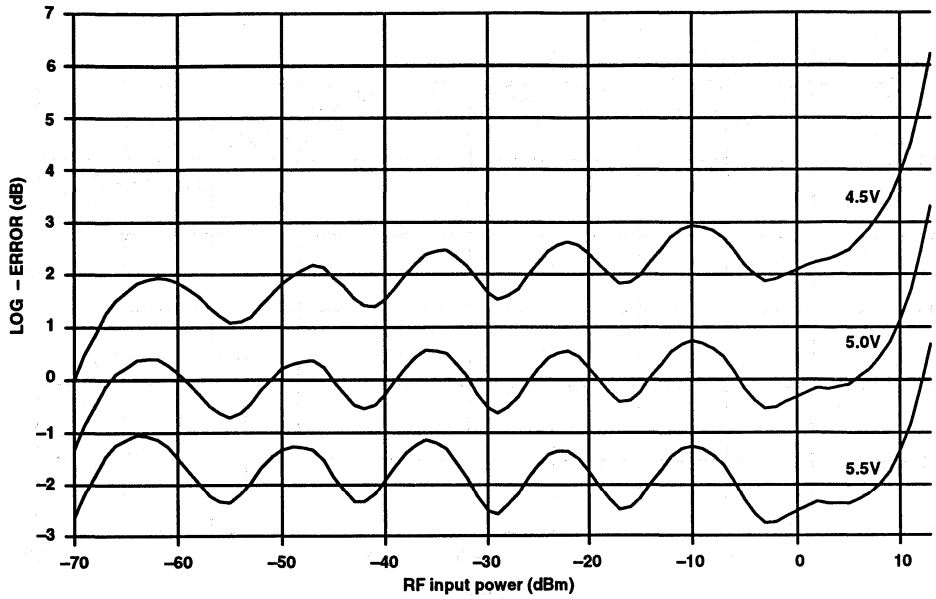


Fig. 14 Video log error, (referenced to single straight line measured at 325MHz, 25°C, 5.0V PSUs), across supply voltage

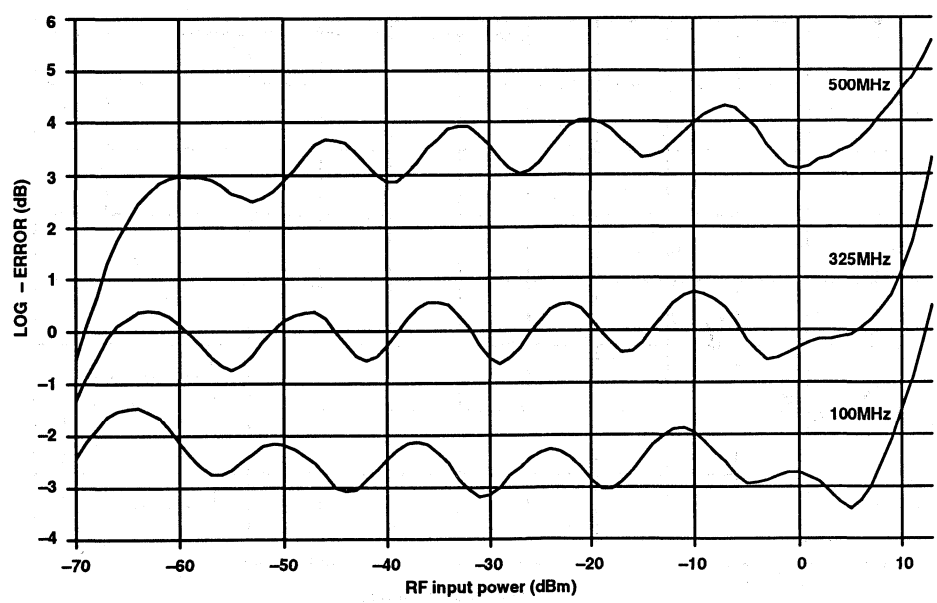


Fig. 15 Video log error, (referenced to single straight line measured at 325MHz, 25°C, 5.0V PSUs), across frequency

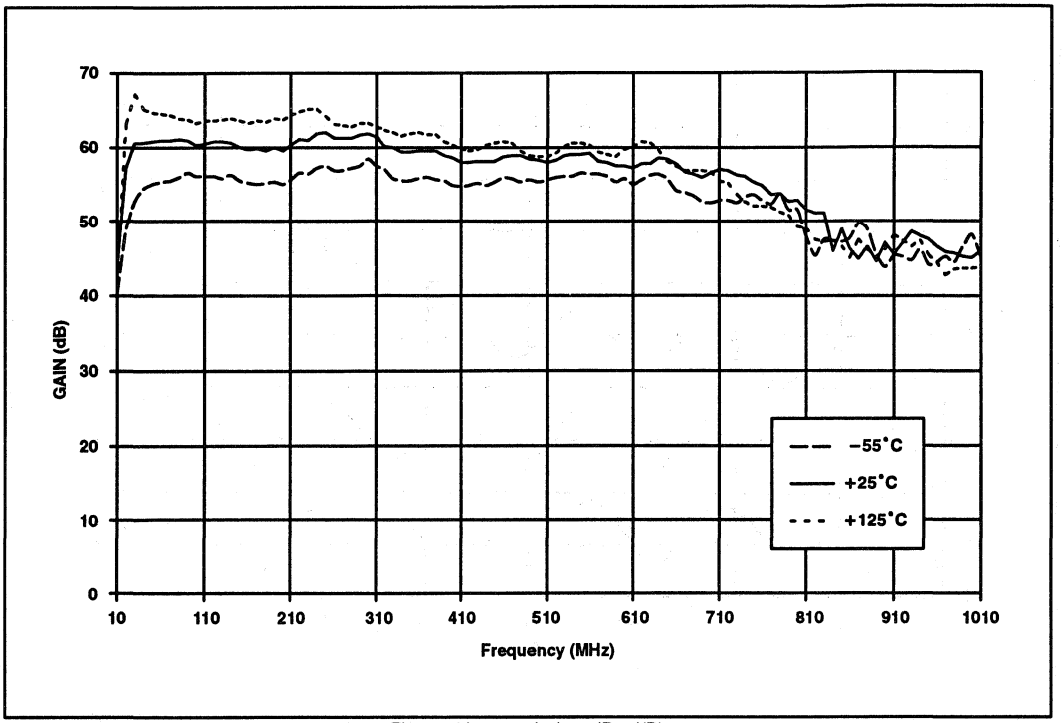


Fig. 16 Linear gain (–70dBm I/P)

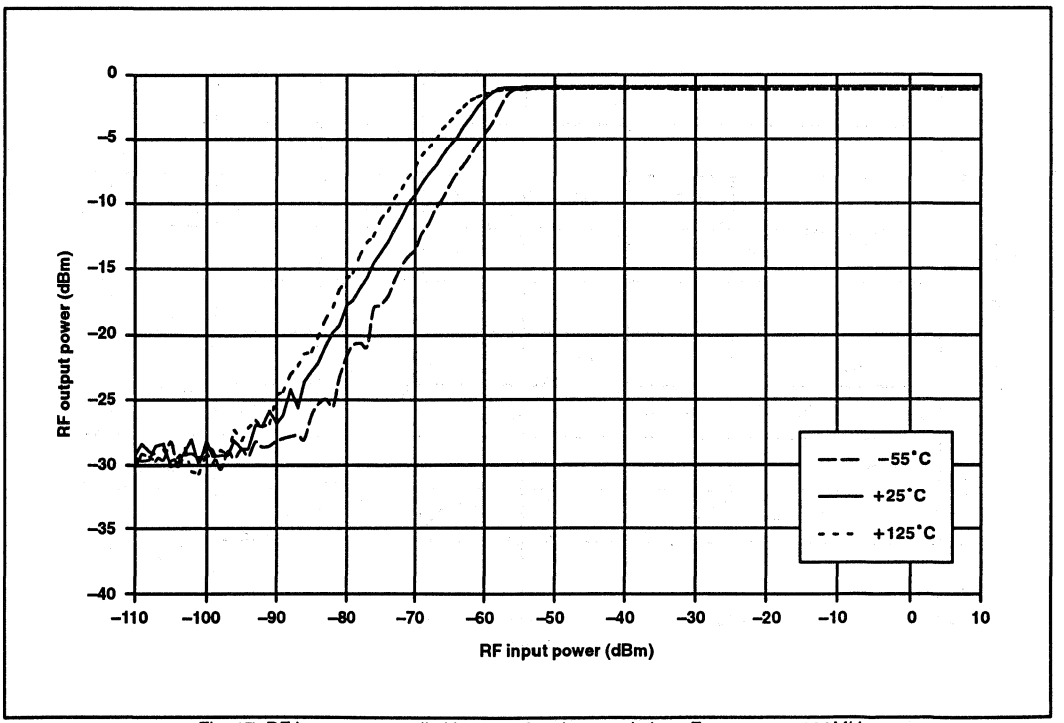


Fig. 17 RF input → output limiting transfer characteristic at Frequency = 100MHz

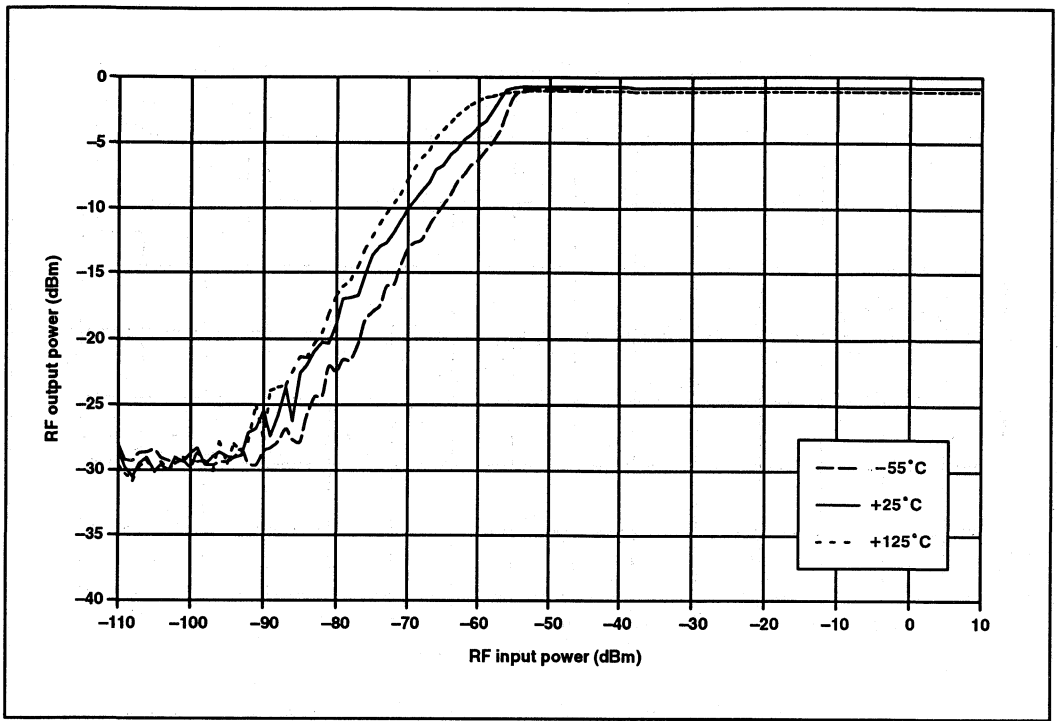


Fig. 18 RF input → output limiting transfer characteristic at Frequency = 325MHz

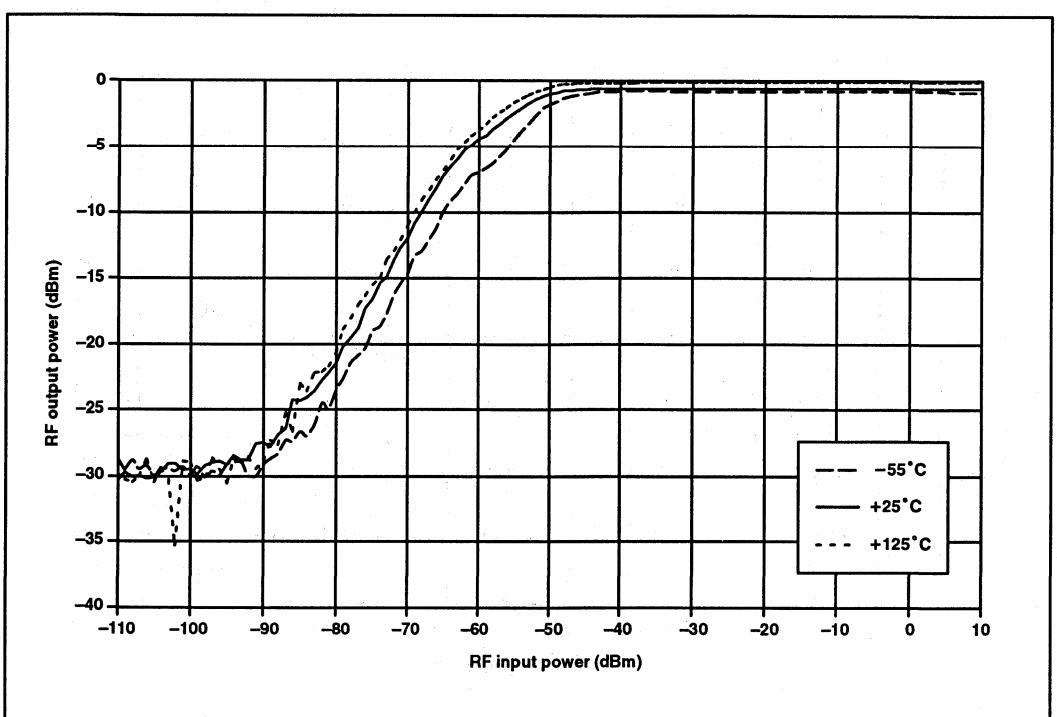


Fig. 19 RF input → output limiting transfer characteristic at Frequency = 500MHz

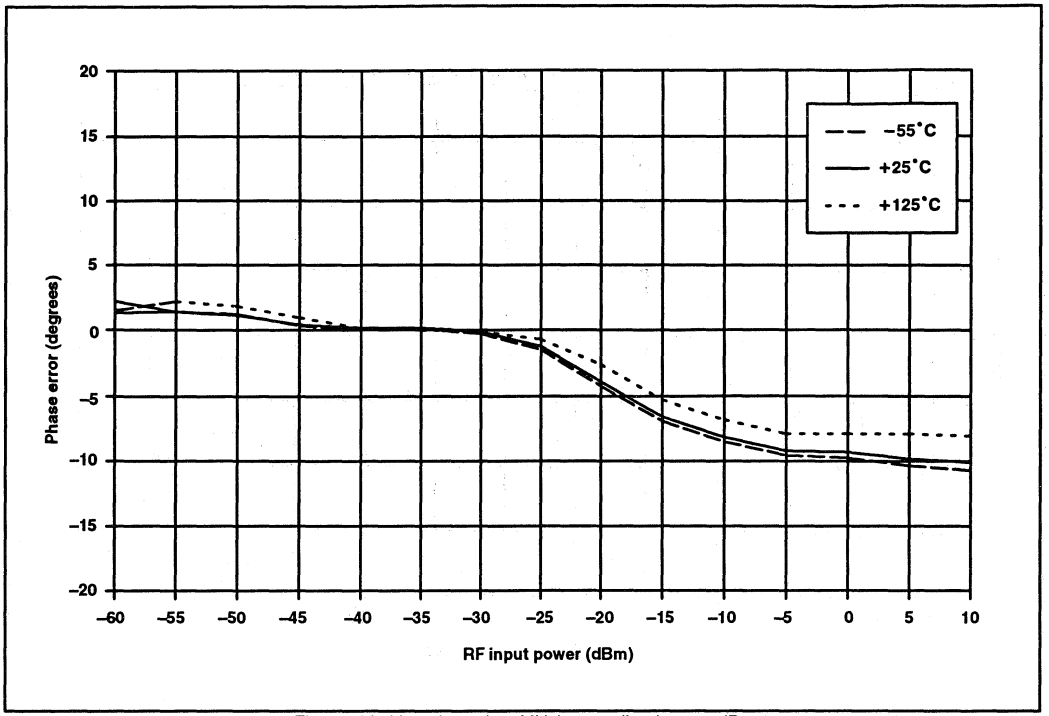


Fig. 20 Limiting phase (100MHz) normalised at –30dBm

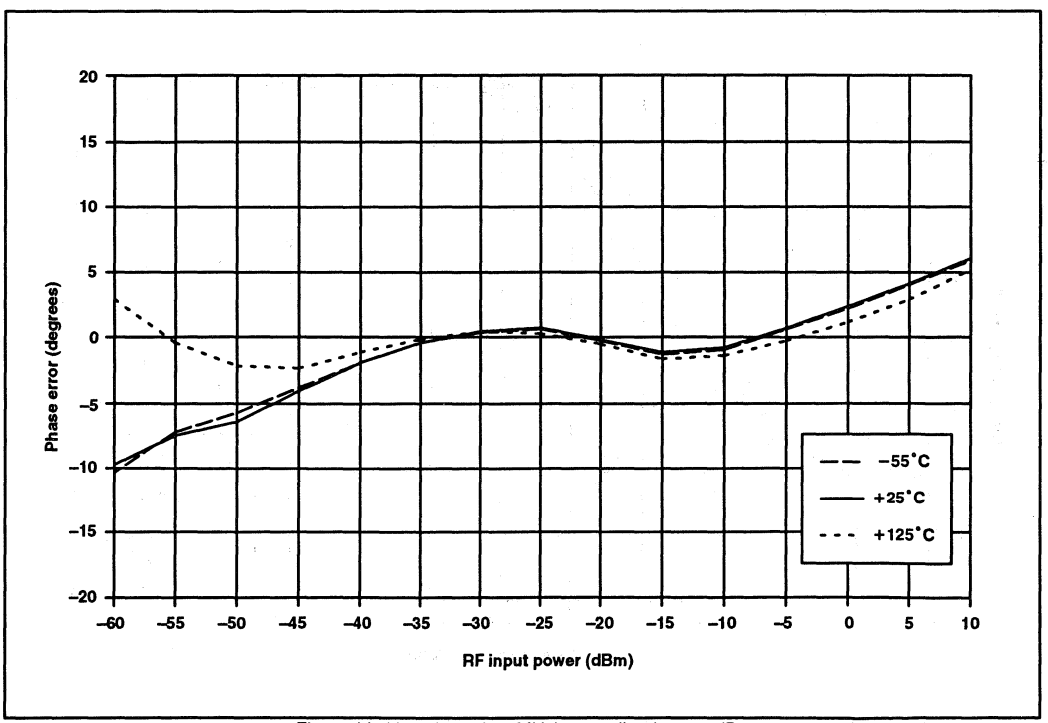


Fig. 21 Limiting phase (300MHz) normalised at –30dBm

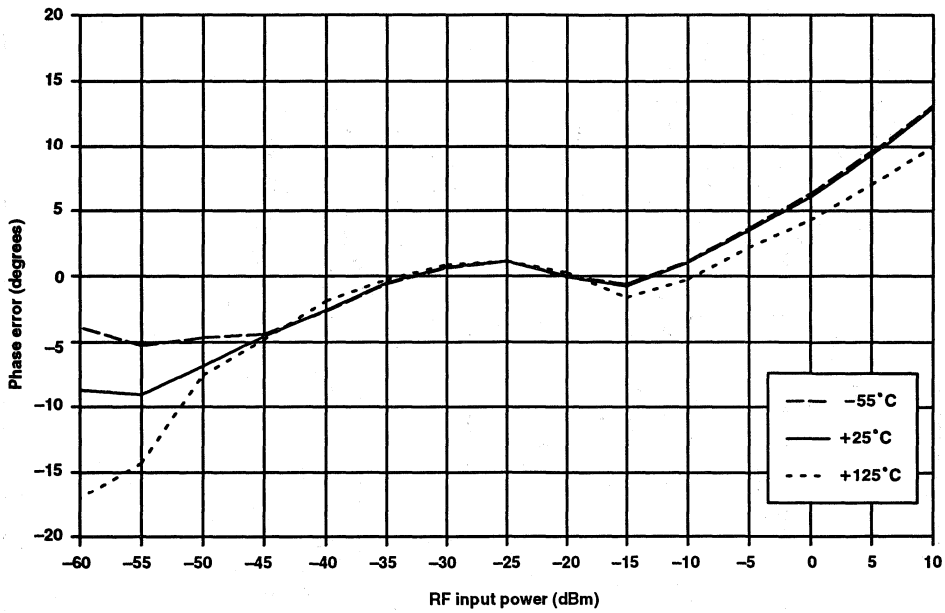


Fig. 22 Limiting phase (500MHz) normalised at –30dBm

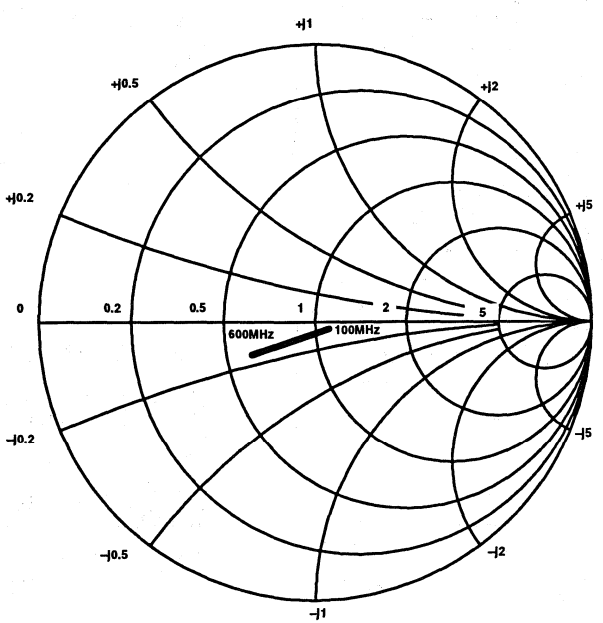


Fig. 23 Typical input impedance normalised to 50Ω – 20dBm I/P level

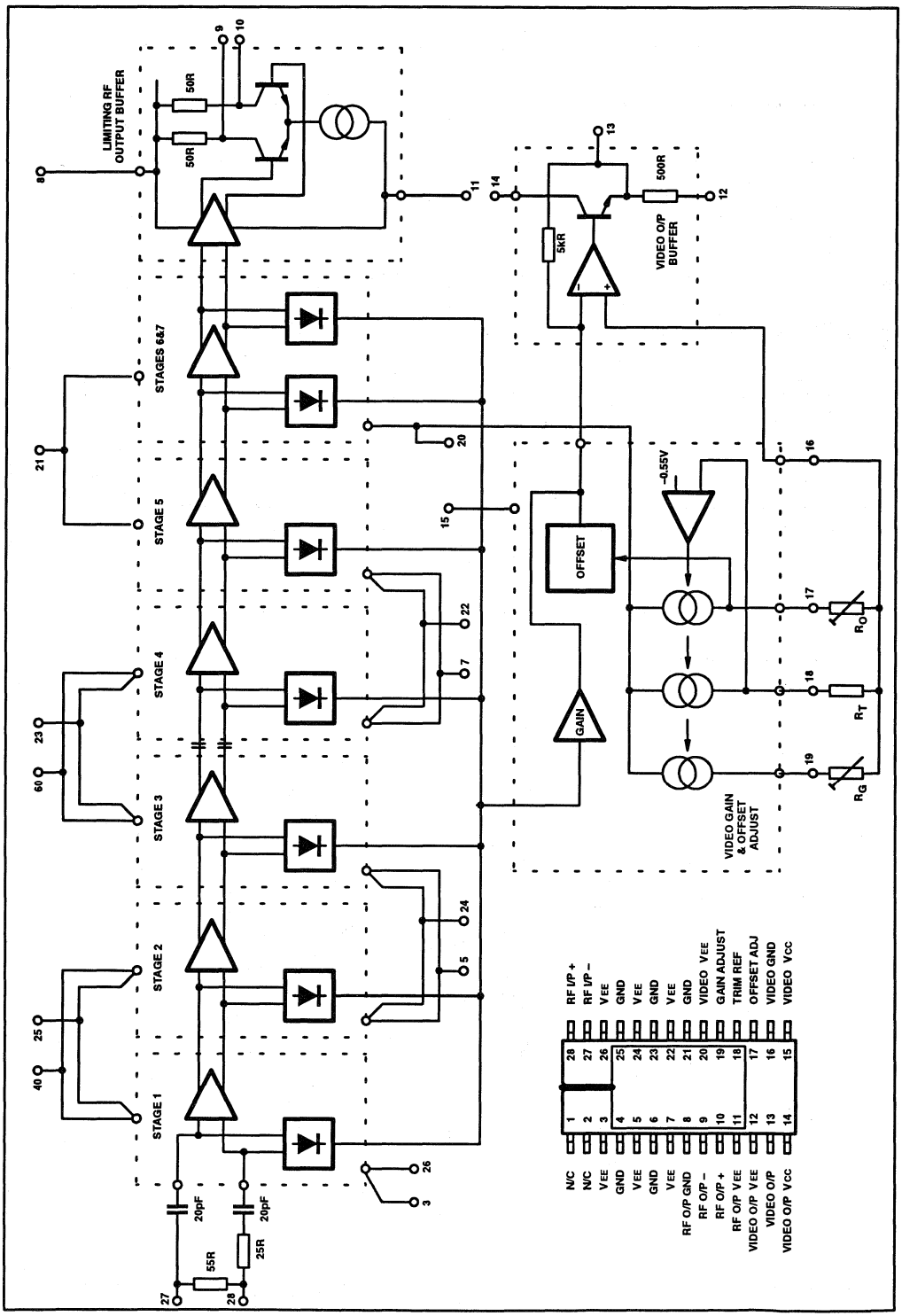
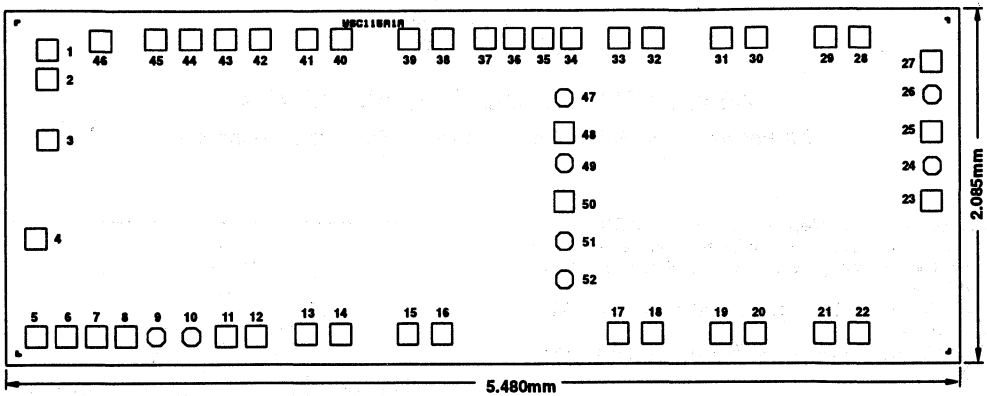


Fig. 24 SL3522 Schematic diagram



TO SCALE

TERMINALS ((X) DENOTES MC PACKAGE PIN NUMBER)							
1	Video O/P (13)	14	V_{EE} 5A (22)	27	Test point	40	V_{EE} 5B (7)
2	Video O/P V_{CC} (14)	15	V_{EE} 4A (22)	28	V_{EE} 1B (3)	41	RF BUF O/P GND (8)
3	Gain V_{CC} (15)	16	GND 4B (23)	29	GND 1B (4)	42	RF BUF O/P GND (8)
4	Video GND (16)	17	GND 3A (23)	30	GND 2B (4)	43	RF O/P – (9)
5	Offset ADJ (17)	18	V_{EE} 3A (24)	31	V_{EE} 2A (5)	44	RF O/P + (10)
6	Trim REF (18)	19	V_{EE} 2A (24)	32	V_{EE} 3A (5)	45	RF BUF O/P V_{EE} (11)
7	Gain ADJ (19)	20	GND 2A (25)	33	GND 3B (6)	46	Video O/P V_{EE} (12)
8	Gain V_{EE} (20)	21	GND 1A (25)	34	Test point	47	Test point
9	Test point	22	V_{EE} 1A (26)	35	Test point	48	Test point
10	Test point	23	Test point	36	Test point	49	Test point
11	V_{EE} 6A (20)	24	RF I/P signal (27)	37	Test point	50	Test point
12	GND 6A (21)	25	Test point	38	GND 4B (6)	51	Test point
13	GND 5A (21)	26	RF I/P return (28)	39	V_{EE} 4B (7)	52	Test point

NOTES
1. All pads with square cross–section =120μm × 120μm
2. All pads with octagonal cross–section =100μm × 100μm
3. Chip is passivated with polyimide

Fig. 25 SL3522 pad map for bare IC dice

SL6140

400MHz WIDEBAND AGC AMPLIFIER

(Supersedes Edition in May 1991 Professional Products I.C. Handbook)

The SL6140 is an integrated broadband AGC amplifier, designed on an advanced 3–micron all implanted bipolar process. The amplifier provides over 15dB of linear gain into 50Ω at 400MHz.

Accurate gain control is also provided with over 70dB of dynamic range.

The SL6140 provides over 45dB of voltage gain with an R_L of 1kΩ.

FEATURES

- 400MHz Bandwidth (R_L=50Ω)
- High voltage Gain 45dB (R_L=1kΩ)
- 70dB Gain Control Range
- High Output Level at Low Gain
- Accurate Gain Control
- Full Military Temperature Range (CM only)
- MC1590 Replacement with Improved Perforance in most applications

APPLICATIONS

- RF/IF Amplifier
- High Gain Mixers
- Video Amplifiers

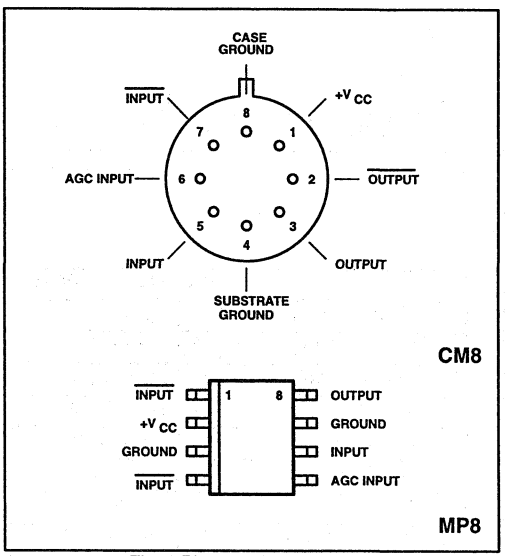


Fig. 1 Pin connections top view

ORDERING INFORMATION

SL6140/NA/MP Industrial temperature range miniature plastic package.
SL6140A/CM Military temperature range metal can package.
SL6140AC/CM MIL STD 883 "Class B" compliant metal can package.

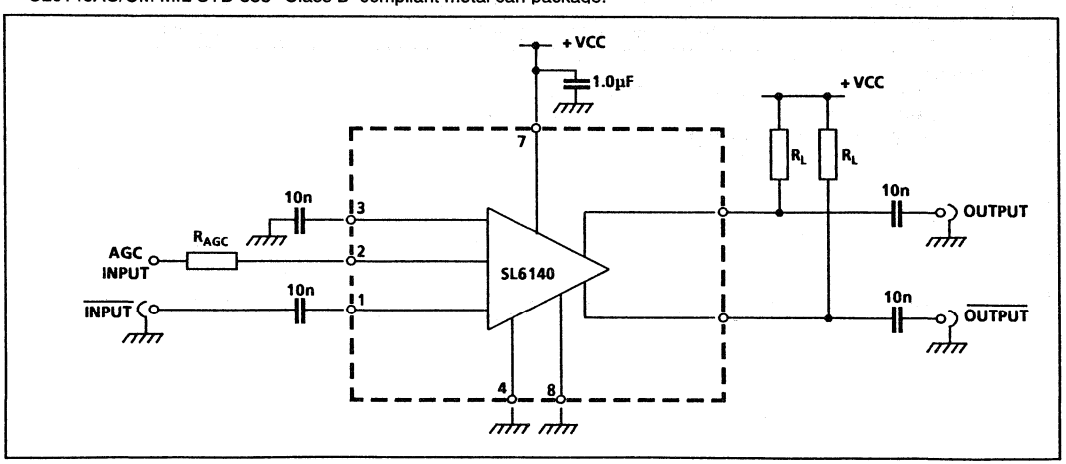


Fig.2 Typical application (CM pinout)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = 25°C, V_{CC} = 12V ±5%, V_{IN} = 1mV_{RMS}, Frequency = 6MHz, Load (R_L) = 1KOHms, R_{AGC} = 22KOHm

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	5,6,7		19	23	mA	No input signal
Output stage current	5,6 (sum)	5	7	9	mA	No input signal
Output current matching (magnitude of difference of output currents)	5,6		1.0		mA	See note 2
AGC range	2	60	75		dB	See Fig. 4 & Note 1 (VAGC = 0V to 10V)
Voltage gain (single ended)	5,6	40	45		dB	R_L = 1kΩ See Fig. 5 & Note 1
			55		dB	Tuned input and Output
	5,6		15		dB	R_L = 50Ω
Bandwidth (-3dB)	5,6		25		MHz	RL = 1kΩ See Fig. 5 See note 2
			400			RL = 50Ω
Maximum output level (single ended)						
0dB AGC	5,6	2.5	3.5		V p-p	Note 1
-30dB AGC	5,6	2.5	3.5		V p-p	R_L = 1kΩ. Note 1
Noise figure	5,6		5		dB	Test CCT Fig. 13
Gain change with temp.	5,6		+4.5		dB	At -55°C W.R.T R/T See note 2
V_{AGC} = 9V	5,6		-3		dB	At +125°C W.R.T R/T See note 2
Gain change with temp.	5,6		+2		dB	At -55°C W.R.T R/T See note 2
V_{AGC} = 10V	5,6		-3		dB	At +125°C W.R.T R/T See note 2

Note: 1 Guaranteed but not tested for MP package

Note: 2 Guaranteed but not tested

DESCRIPTION

The SL6140 (Fig. 3) is a high gain amplifier with an AGC control capable of reducing the gain of the amplifier by over 70dB. The gain is adjustable by applying a voltage to the AGC input via an external resistor (R_{AGC}), the value of which adjusts the curve of gain reduction versus control voltage (see Fig. 4). As the output stage of the amplifier is an open collector the maximum voltage gain is determined by R_L. With load resistance of 1kΩ the single ended voltage gain is 45dB and with a load resistance of 50Ω the voltage gain is 15dB ($20\log_{10} V_{OUT}/V_{IN}$). Another parameter that depends on the load resistance is the bandwidth: 25MHz for R_L = 1kΩ, as compared with 400MHz for R_L = 50Ω. R_L is chosen to give either the required bandwidth or voltage gain for the circuit.

Figs. 7 through to 10 show the typical S parameters for the device. Figs 11 and 12 show the typical variation in 3rd order intercept performance with AGC.

In any application, the substrate (pin 4 in CM 8, pin 7 in MP 8) should be connected to the most negative point in the circuit, usually to the same point as pin 8 (pin 3 in MP 8).

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	+18V
Input voltage (differential)	+5V
AGC supply	V_{CC}
Storage temperature	-55°C to +150°C
Operating temperature range	
SL6140 MP	-40°C to +85°C
SL6140 A CM	-55°C to +125°C
	at 200mW
Chip operating temperature	
SL6140 MP	+150°C
SL6140 (CM variants)	+175°C

THERMAL RESISTANCE

Chip-to-ambient	
SL6140 MP	163°c/w
SL6140 (CM variants)	225°C/W
Chip-to-case	
SL6140 MP	57°C/W
SL6140 (CM variants)	65°C/W

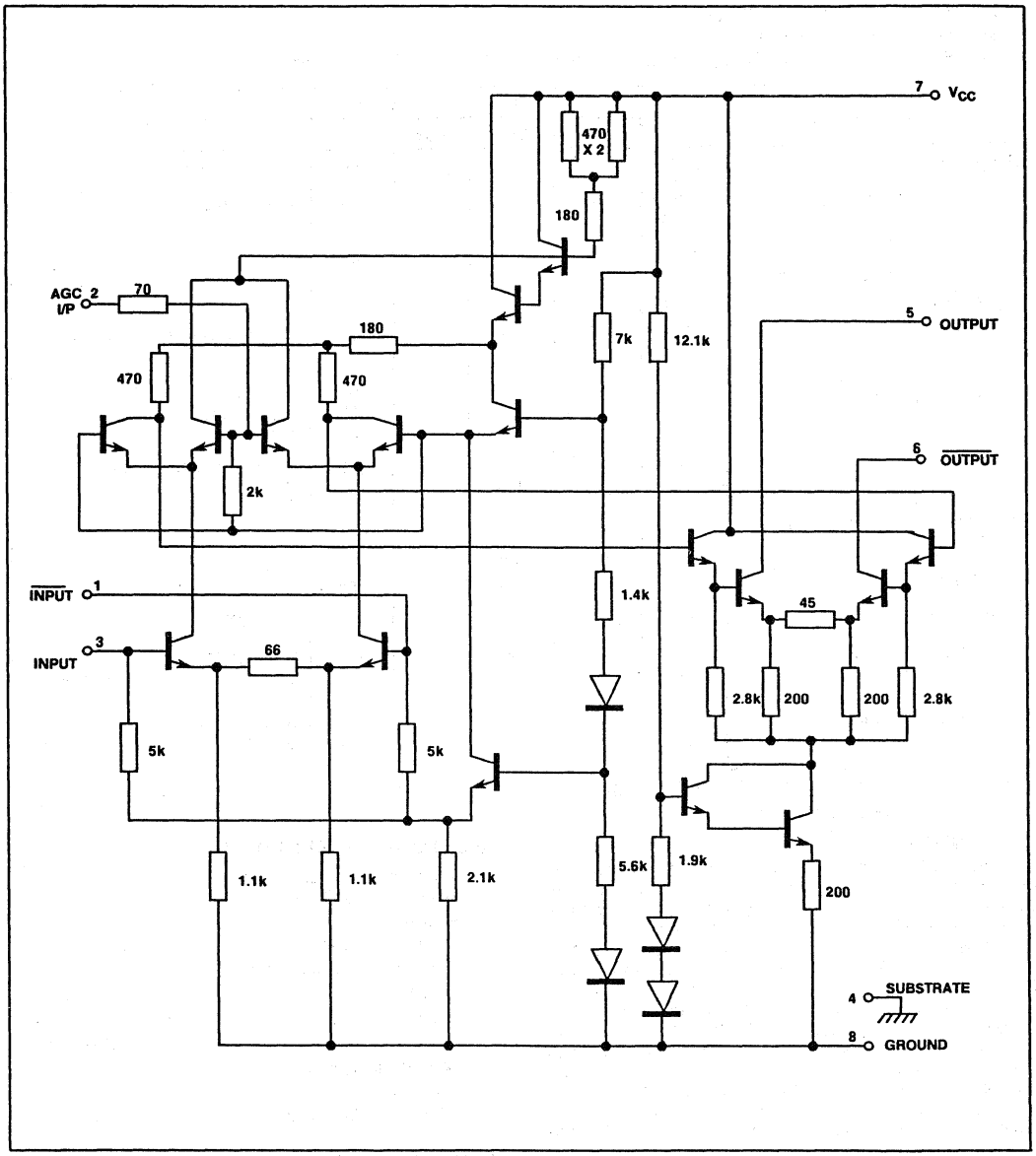


Fig. 3 Full circuit diagram of SL6140 (CM pinout)

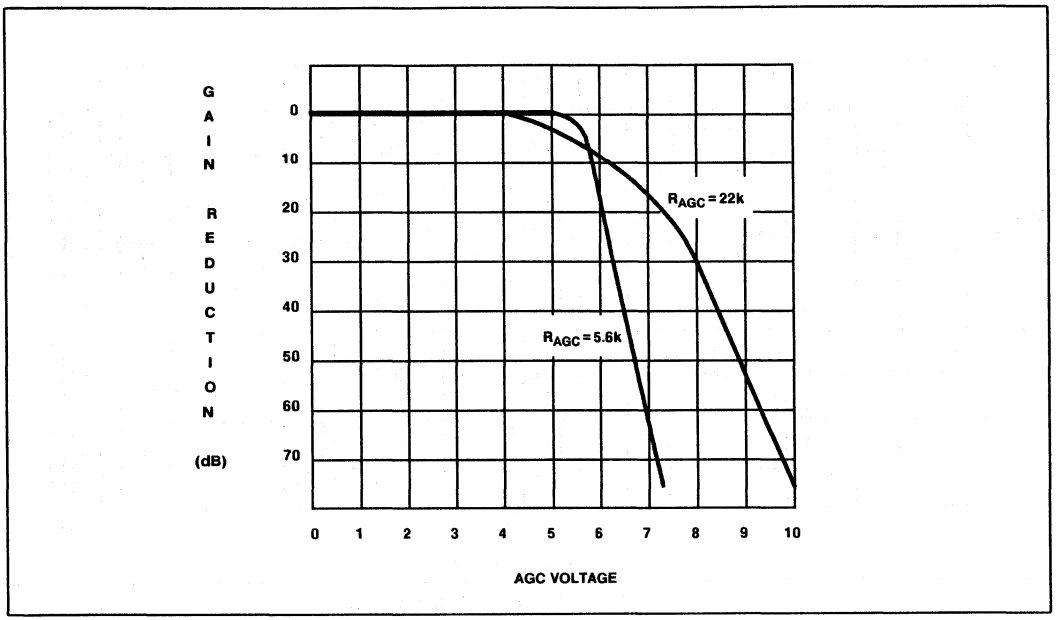


Fig. 4 Gain reduction v. AGC voltage

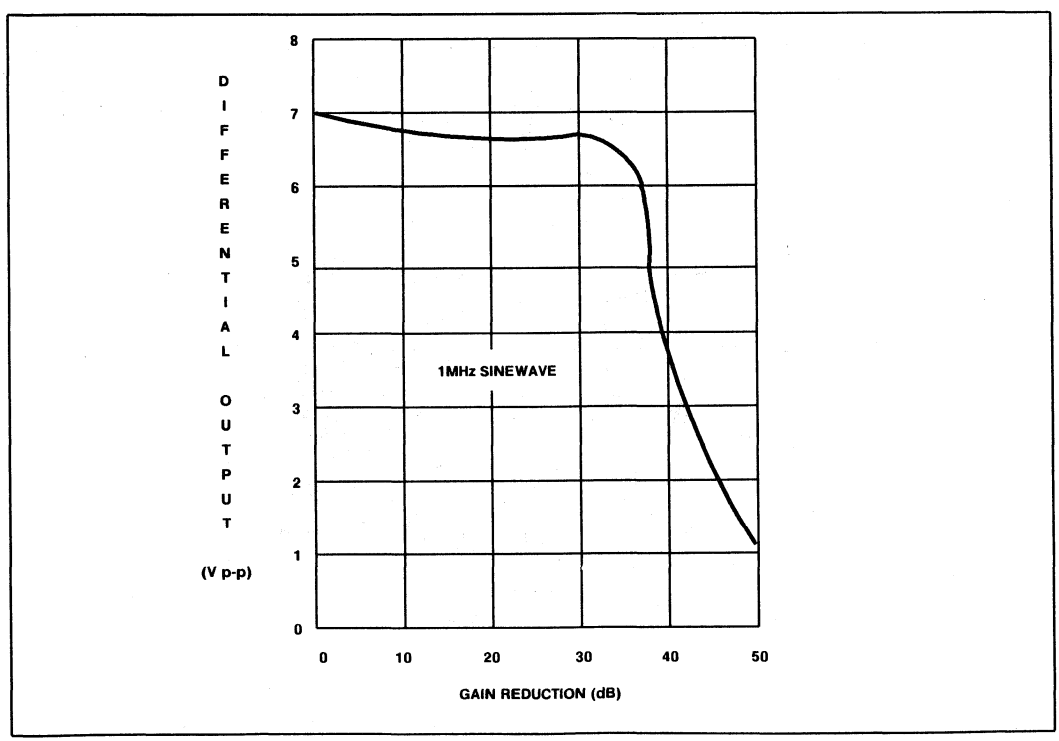


Fig. 5 Max differential O/P voltage v gain reduction

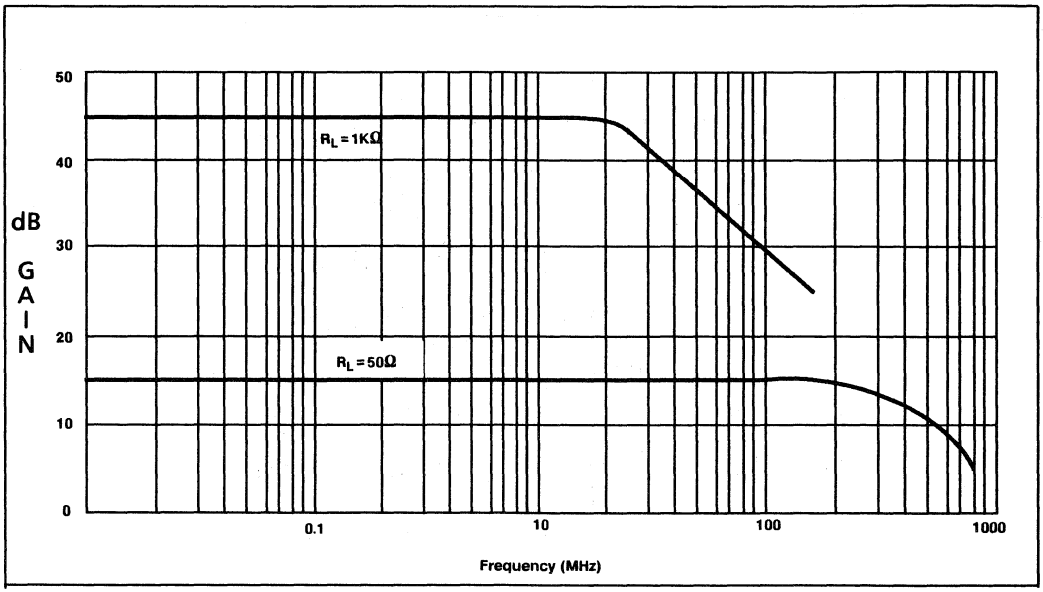


Fig. 6 Voltage Gain V. Frequency

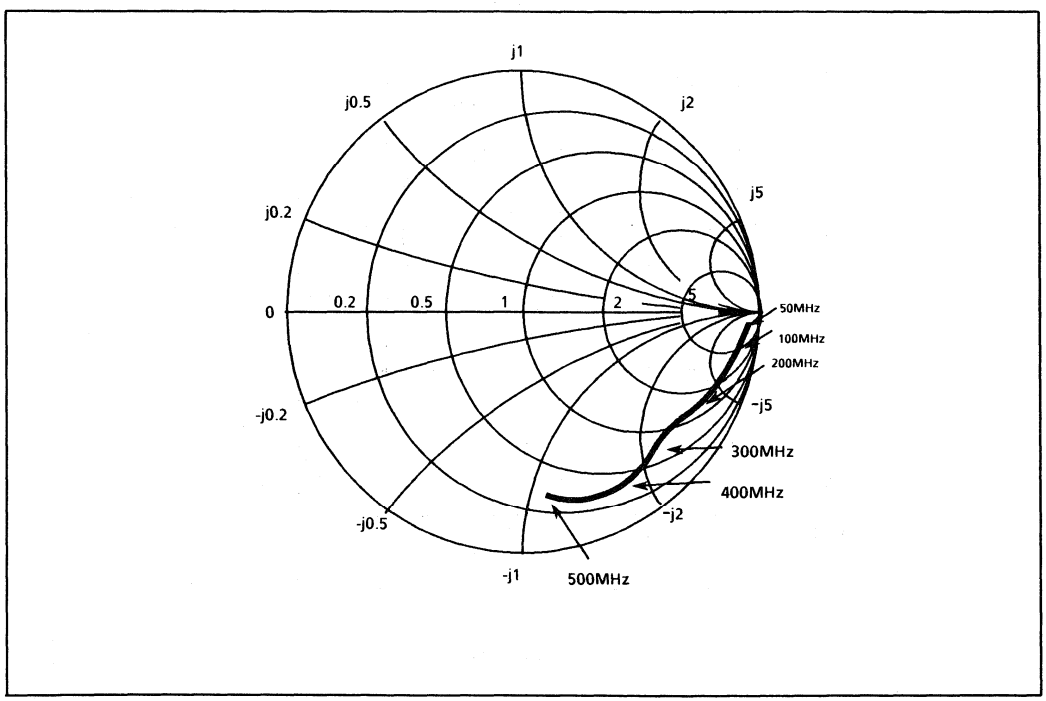


Fig. 7 Input impedance 50Ω system

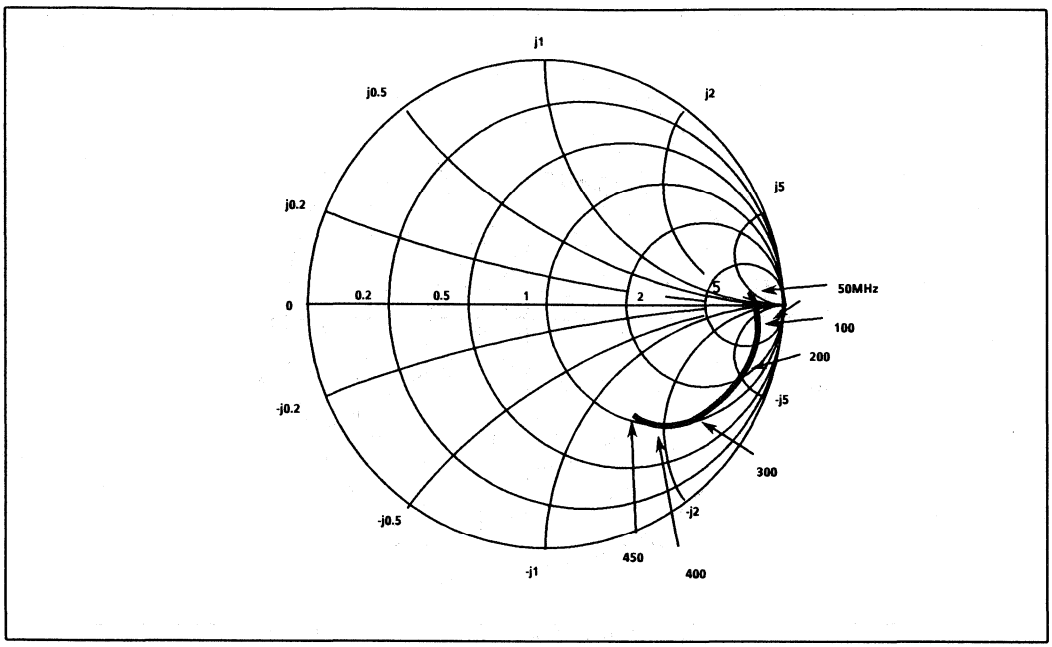


Fig. 8 Output impedance 50Ω system

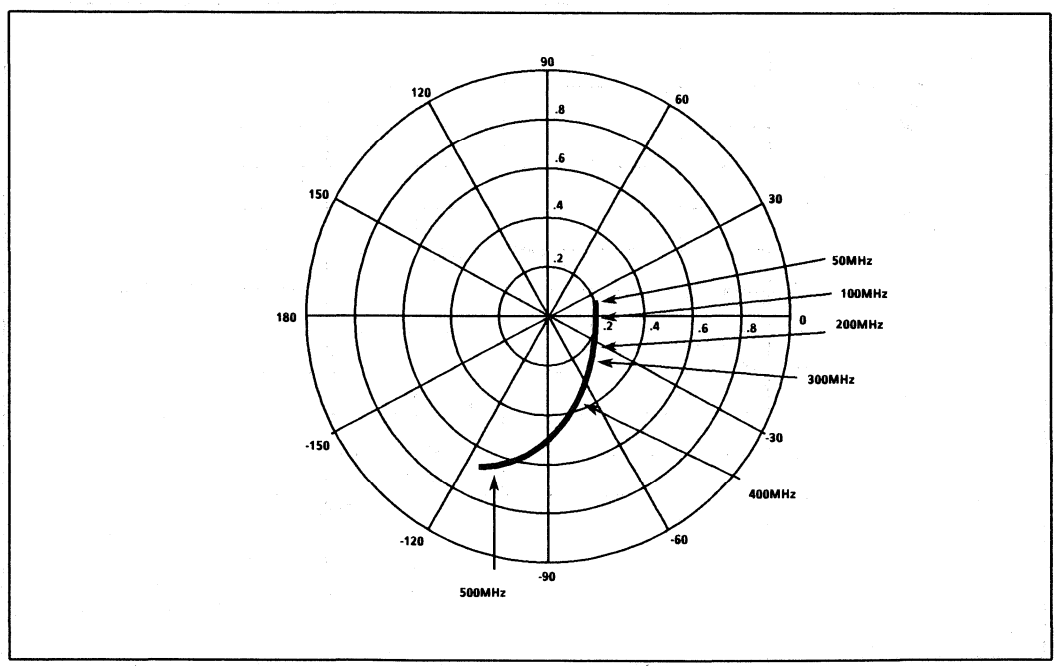


Fig. 9 Reverse transmission coefficient S_{12} SL6140

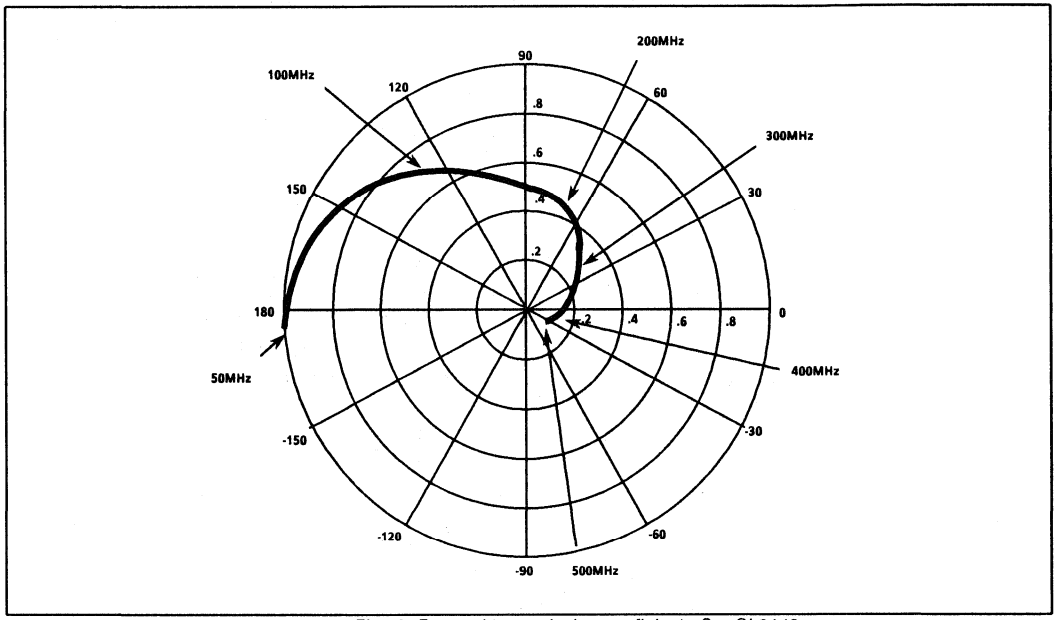


Fig.10 Forward transmission coeficients S_{21} SL6140

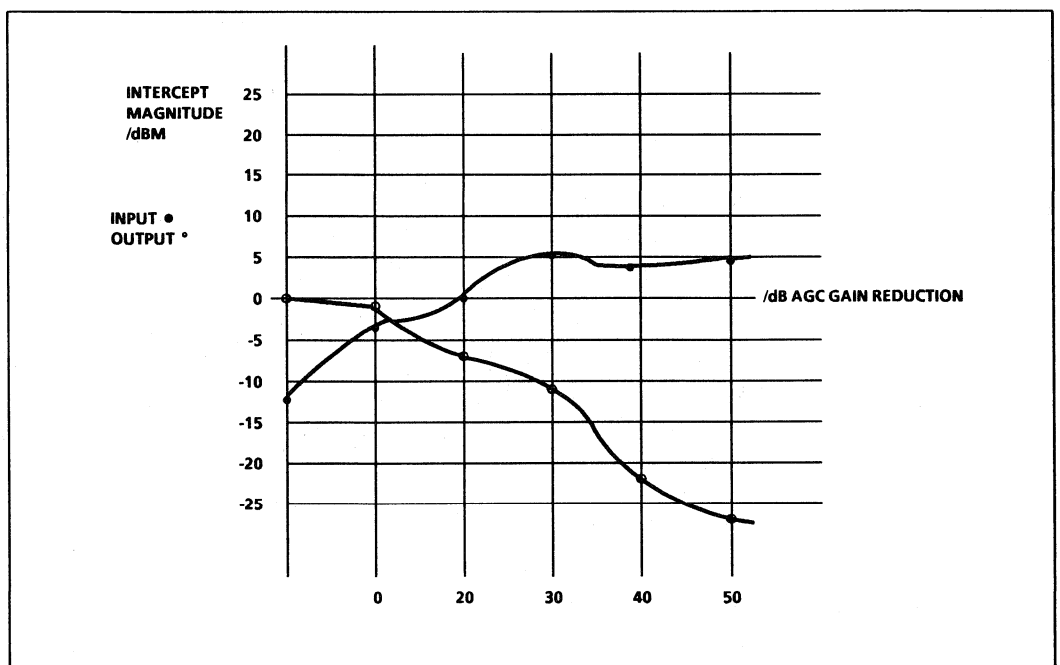


Fig.11 3rd Order intercept point against gain reduction at 250.0Mhz and 254.0MHz

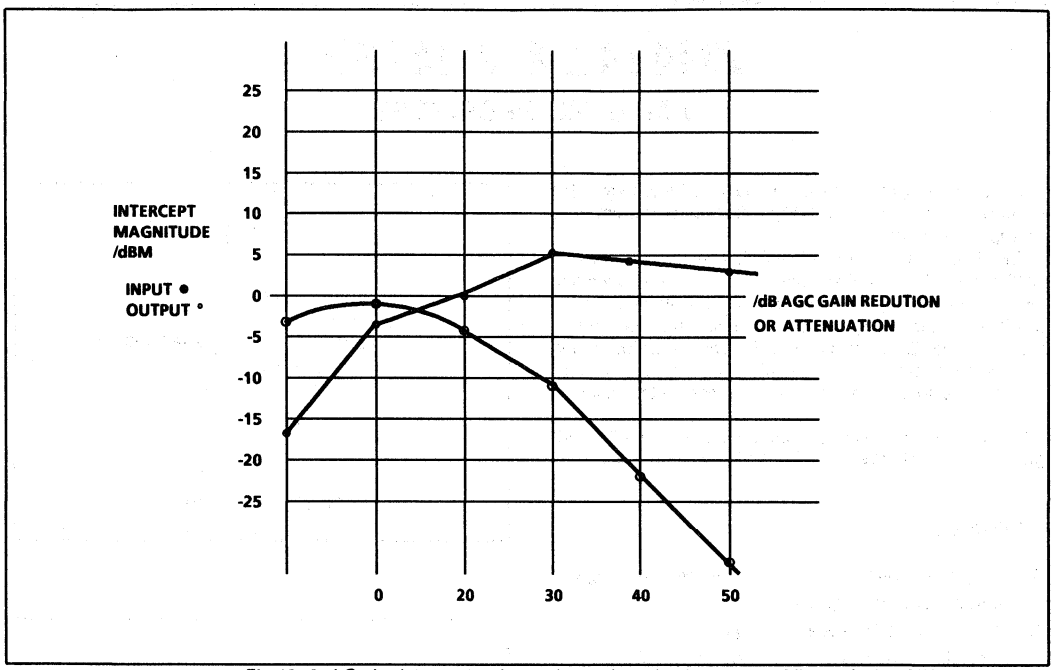


Fig.12 3rd Order intercept point against gain reduction at 100.0Mhz and 104.0MHz

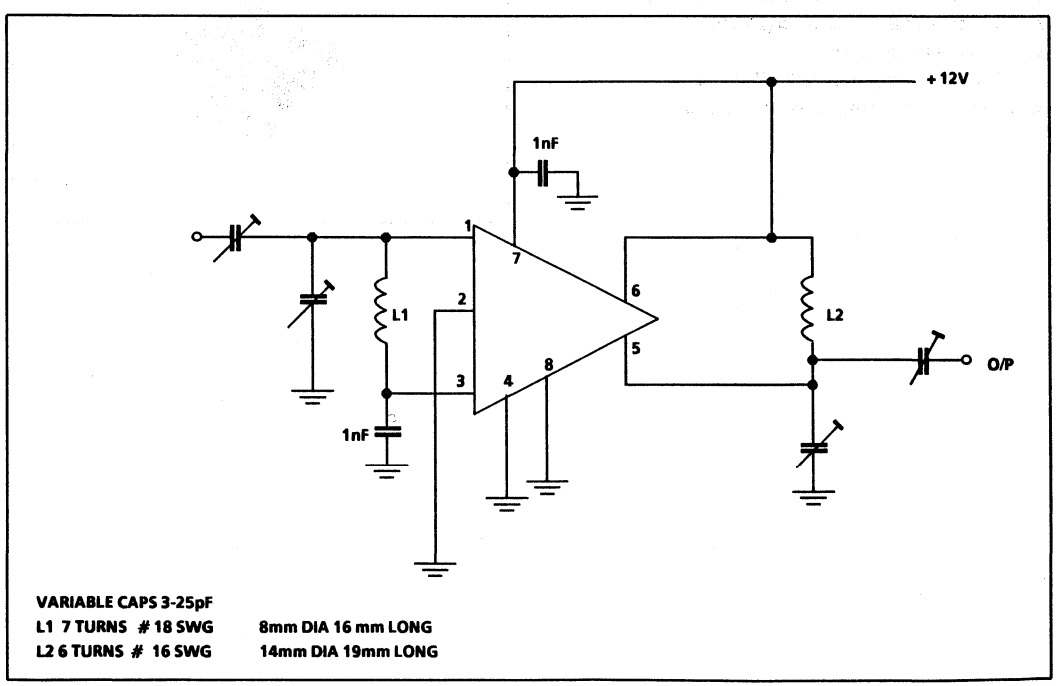


Fig.13 50MHz Noise figure test circuit CM package)

ZN414Z & ZN416E

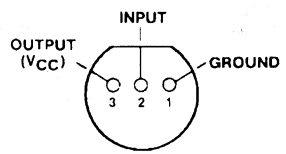
AM RADIO RECEIVERS

The ZN414Z is a 10 transistor tuned radio frequency (TRF) circuit packaged in a 3-pin TO-92 plastic package for simplicity and space economy .

The circuit provides a complete R.F. amplifier, detector and AGC circuit which requires only six external components to give a high quality A.M. tuner. Effective AGC action is available and is simply adjusted by selecting one external resistor value. Excellent audio quality can be achieved, and current consumption is extremely low. No setting-up or alignment is required and the circuit is completely stable in use.

The ZN416E is a buffered output version of the ZN414Z giving typically 120mV (r.m.s.) output into a 64Ω load.

ZN414Z



PLASTIC (TO-92)

ZN416E

DP8

FEATURES

- Single cell operation (1.1 to 1.6 volt operating range)
- Low current consumption
- 150kHz to 3MHz frequency range
  (i.e. full coverage of medium and long wavebands)
- Easy to assemble, no alignment necessary
- Simple and effective AGC action
- Will drive crystal earphone direct (ZN414Z)
- Will drive headphone direct (ZN416E)
- Excellent audio quality
- Typical power gain of 72dB (ZN414Z)
- Minimum of external components required

DEVICE SPECIFICATIONS

(T_{amb} = 25°C, V_{CC} = 1.4V. Parameters apply to all types unless otherwise specified)

Parameter		Min.	Typ.	Max.	Units
Supply voltage, V_{CC}		1.1	1.3	1.6	Volts
Supply current, I_S	ZN414Z		0.3	0.5	mA
with 64Ω headphones	ZN416E		4	5	mA
Input frequency range		0.15		3.0	MHz
Input resistance			4.0		MΩ
Threshold sensitivity (Dependant on Q of coil)			50		µV
Selectivity			4.0		kHz
Total harmonic distortion			3.0		%
AGC range			20		dB
Power gain (ZN414Z)			72		dB
Voltage gain of output stage	ZN416E		18		dB
Output voltage into 64Ω load	ZN414Z		60		mVpp
before clipping	ZN416E		340		mVpp
Upper cut-off frequency of output stage, No capacitor, (ZN416E)			20		kHz
With 0.01µF between pin 7 and 0V (ZN416E)			10		kHz
Lower cut-off frequency of output stage 0.47µF between pins 2 and 3 for ZN416E			50		kHz
Quiescent output voltage	ZN414Z		40		mV
	ZN416E		200		mV
Operating temperature range		0		70	°C
Maximum storage temperature		-65		125	°C

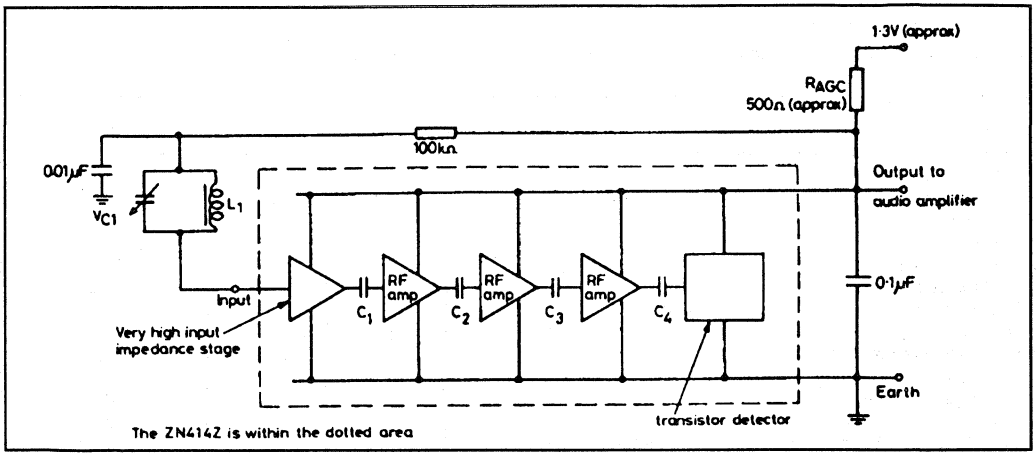


Fig.1 ZN414Z System Diagram

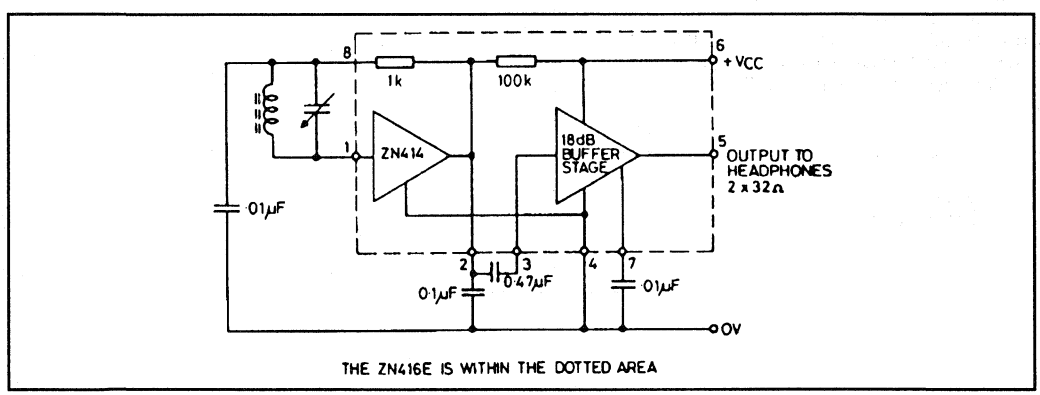


Fig.2 ZN416E System Diagram

ZN414Z CHARACTERISTICS - **All measurements performed with 30% modualtion, FM = 400Hz**

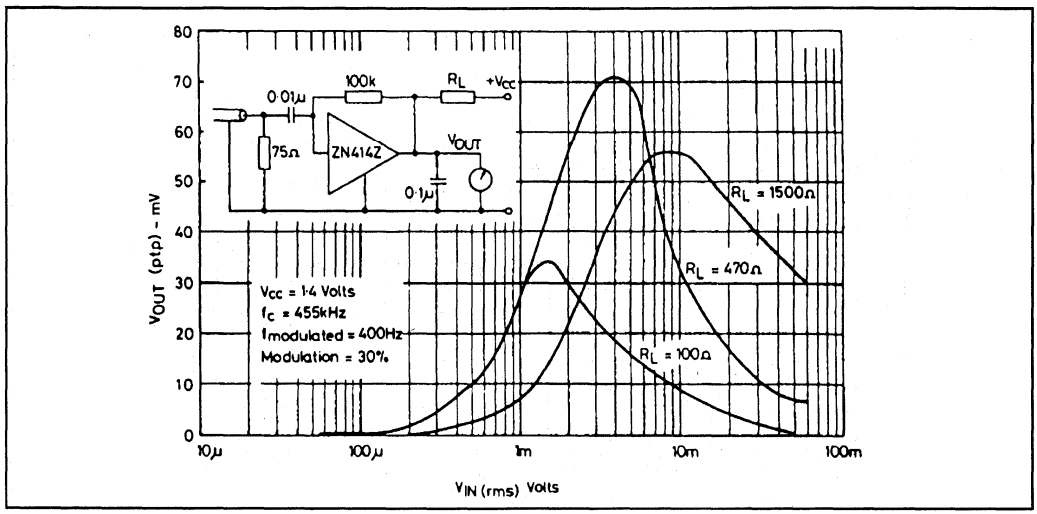


Fig.3 Gain and AGC characteristics

See operating notes for explanation of AGC action.

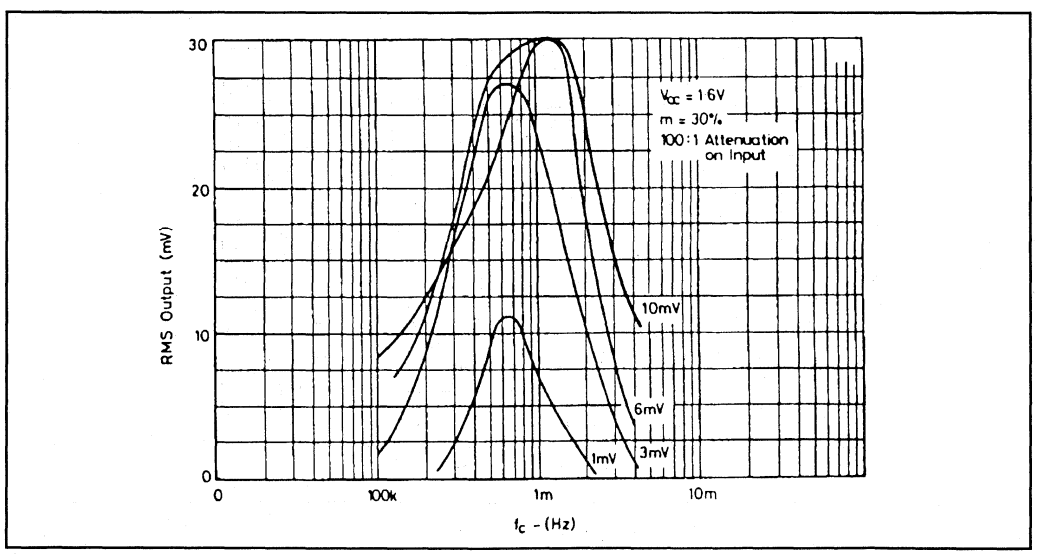


Fig.4 Frequency response of the ZN414Z

Note that this graph represents the chip response, and not the receiver bandwidth.

ZN414Z CHARACTERISTICS - *(Continued)*

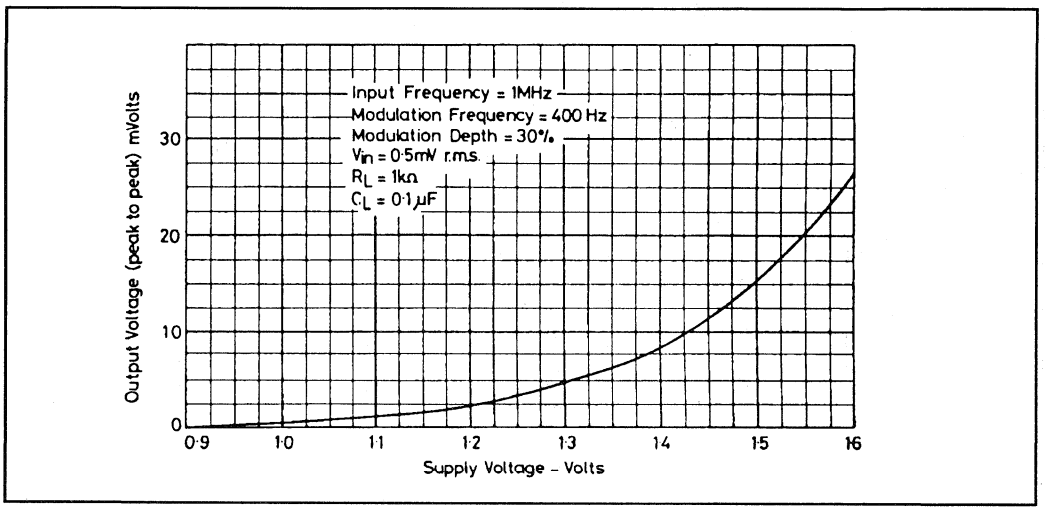


Fig.5 Gain variation with supply volts.

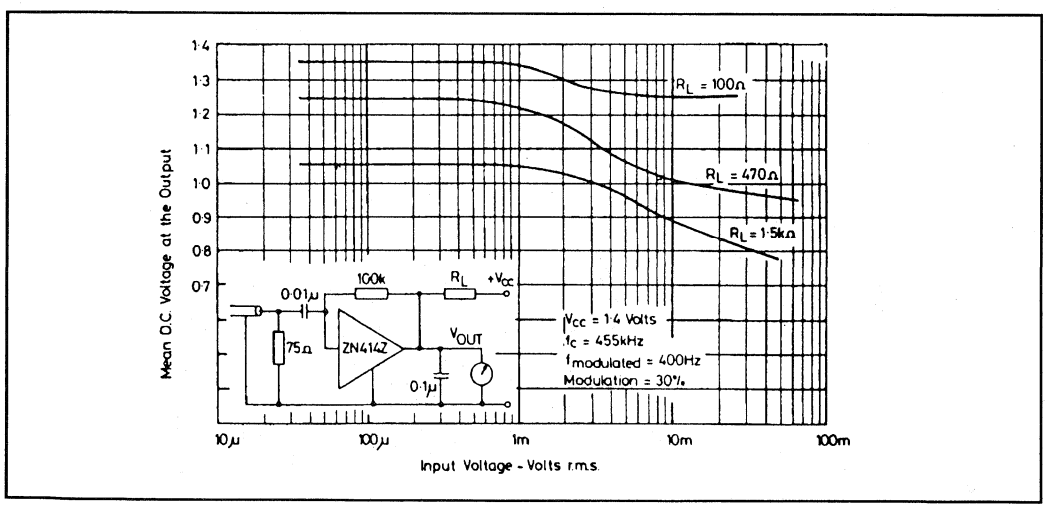


Fig.6 D.C. level at output

LAYOUT REQUIREMENTS

As with any high gain R.F. device, certain basic layout rules must be adhered to if stable and reliable operation is to be obtained. These are listed below:

1. The output decoupling capacitor should be soldered as near as possible to the output and earth leads of the ZN414Z. Furthermore, its value together with the AGC resistor (R_{AGC}) should be calculated at =4kHz, i.e.:

$$C \text{ (farads)} = \frac{1}{2\pi \cdot R_{AGC} \cdot 4 \cdot 10^3}$$

2. All leads should be kept as short as possible, especially those in close proximity to the ZN414Z.

3. The tuning assembly should be some distance from the battery, loudspeaker and their associated leads .

4. The 'earthy' side of the tuning capacitor should be connected to the junction of the 100kΩ resistor and the 0.01μF capacitor.

OPERATING NOTES

(a) Selectivity
To obtain good selectivity, essential with any T.R.F. device, the ZN414Z must be fed from an efficient, high 'Q' coil and capacitor tuning network. With suitable components the selectivity is comparable to superhet designs, except that a very strong signal in proximity to the receiver may swamp the device unless the ferrite rod aerial is rotated to "null-out" the strong signal.

Two other factors affect the apparent selectivity of the device. Firstly, the gain of the ZN414Z is voltage sensitive (see previous page) so that, in strong signal areas, less supply voltage will be needed to obtain correct AGC action. Incorrect adjustment of the AGC causes a strong station to occupy a much wider bandwidth than necessary and in extreme cases can cause the RF stages to saturate before the AGC can limit RF gain. This gives the effect of swamping together with reduced AF output. All the above factors have to be considered if optimum performance is to be obtained.

(b) Ferrite aerial size
Because of the gain variation available by altering supply voltage, the size of the ferrite rod is relatively unimportant. However, the ratio of aerial rod length to diameter should ideally be large to give the receiver better directional properties. Successful receivers have been constructed with ferrite rod aerials of 4cm (1.5") and up to 20cm (8").

DRIVE CIRCUITS

Three types of drive circuit are shown. each has been used successfully. The choice is largely an economic one, but circuit 3 is recommended wherever possible, having several advantages over the other circuits. Values for 9V supplies are shown, simple calculations will give values for other supplies.

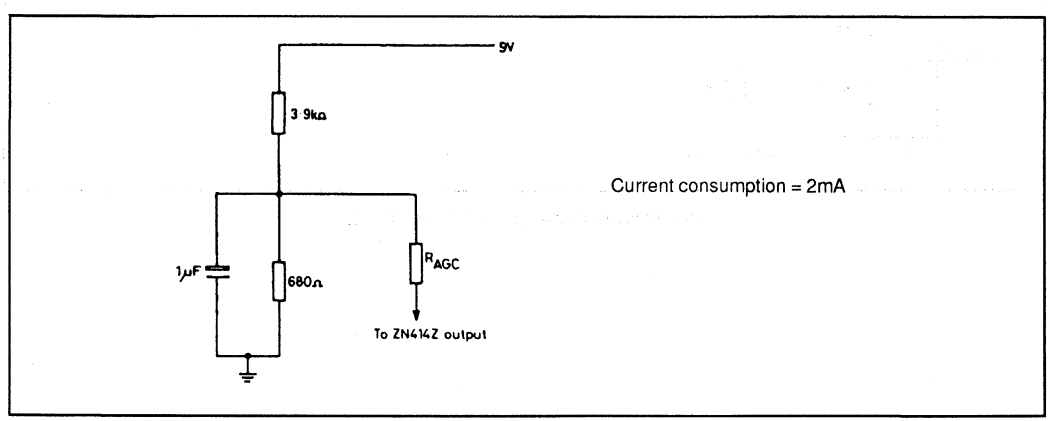


Fig.7 Resistive Divider (ZN414Z)

Note: Replacing the 680Ω resistor with a 500Ω resistor and a 250Ω preset, sensitivity may be adjusted and will enable optimum reception to be realised under most conditions.

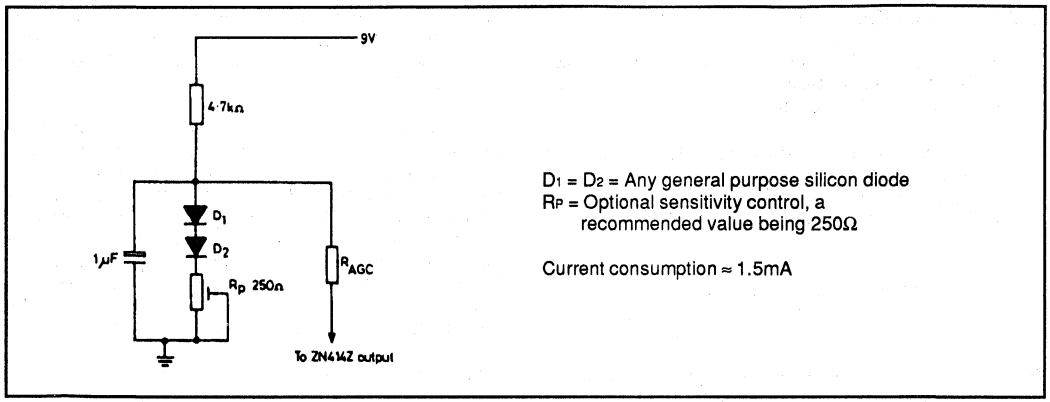


Fig.8 Diode Drive (ZN414Z)

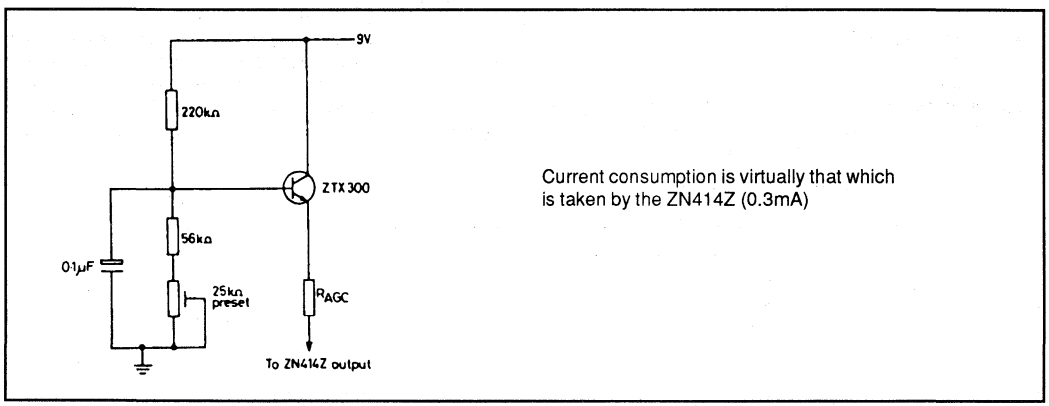


Fig.9 Transistor Drive (ZN414Z and ZN415E)

RECOMMENDED CIRCUITS

(a) Earphone radio

The ZN414Z will drive a sensitive earpiece directly. In this case, an earpiece of equivalent impedance to R_{AGC} is substituted for R_{AGC} in the basic tuner circuit. Unfortunately, the cost of a sensitive earpiece is high, and unless an ultra-miniature radio is wanted, it is considerably cheaper to use a low cost crystal earpiece and add a single gain stage. One further advantage of this technique is that provision for a volume control can be made. A suitable circuit is shown below.

L_1 = 80 turns of 0.3mm dia. enamelled copper wire on a 5cm or 7.5cm long ferrite rod. Do not expect to adhere rigidly to the coil-capacitor details given. Any value of L_1 and C_1 which will give a high 'Q' at the desired frequency may be used.
Volume Control: a 250Ω potentiometer in series with a 100Ω fixed resistor substituted for the 270Ω emitter resistor provides an effective volume control.

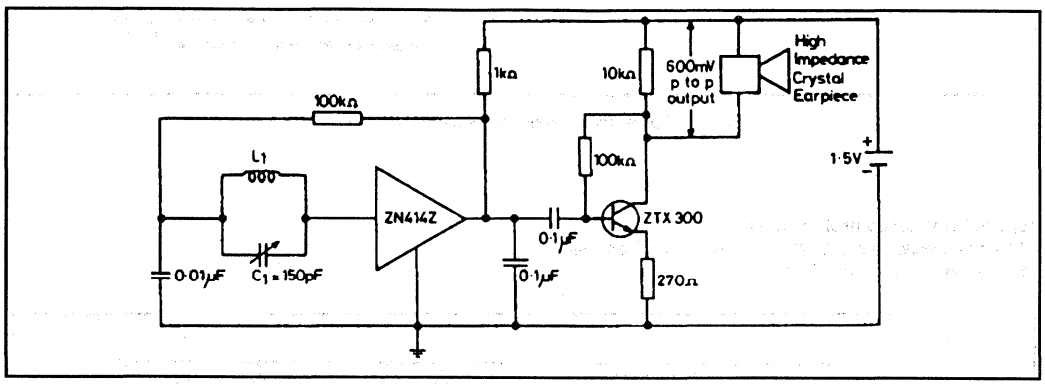


Fig.10 Earphone Radio

(b) Domestic portable receiver

The circuit shown is capable of excellent quality, and its cost relative to conventional designs is much lower

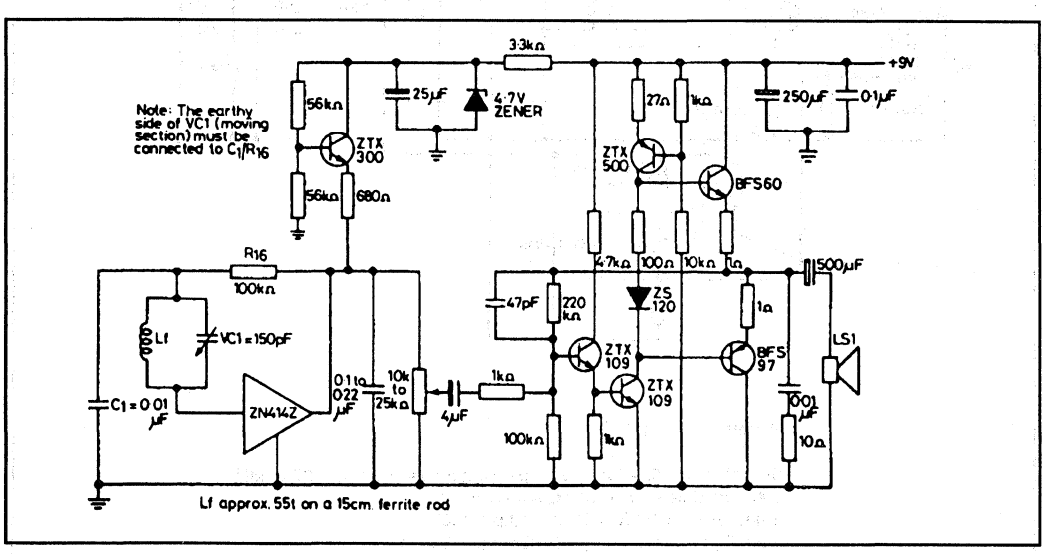


Fig.11 The complete circuit diagram of the Triffid receiver

(b) i

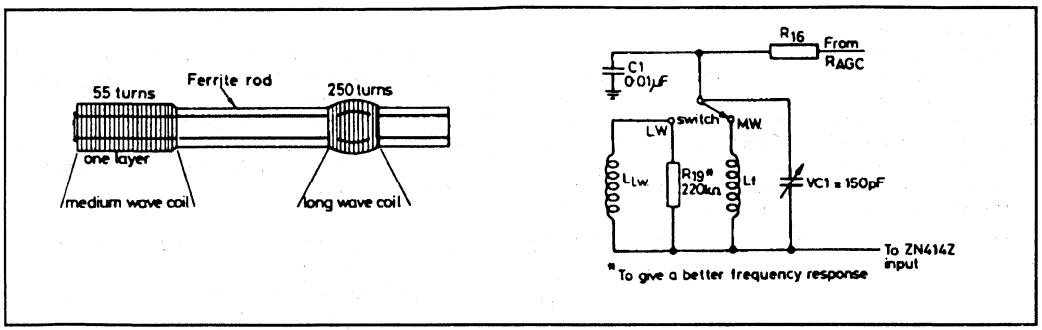
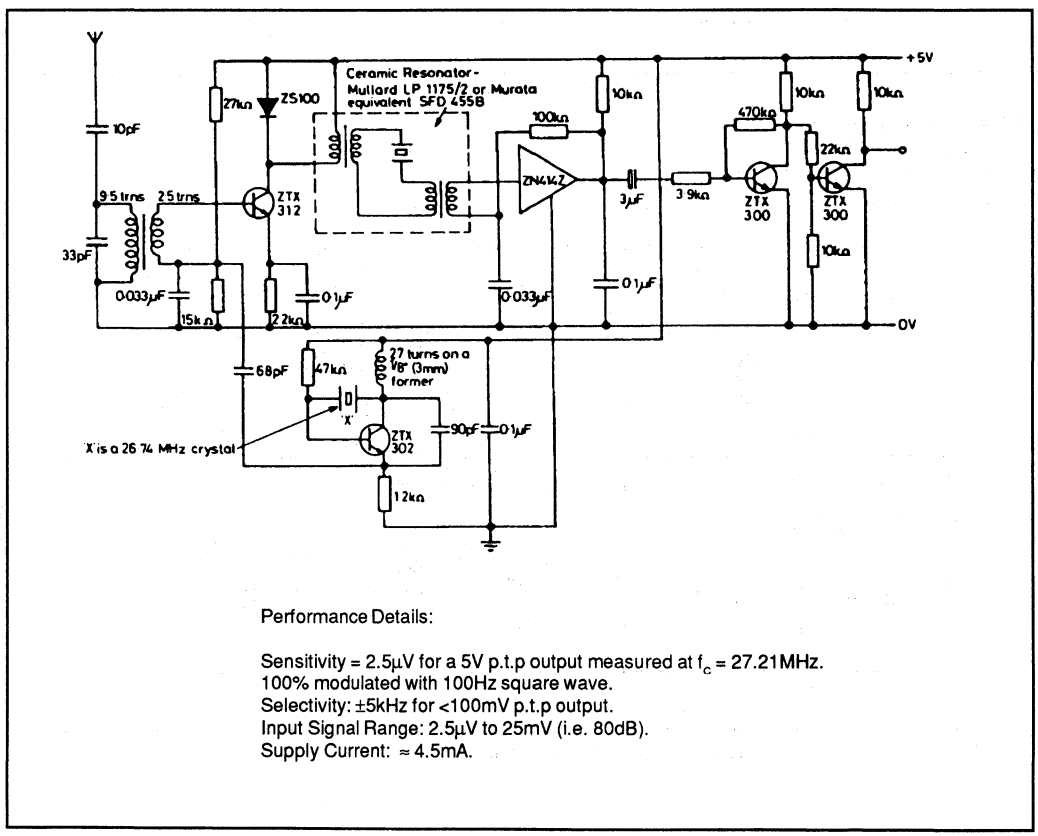


Fig.12 Coil winding details and waveband selection

(c) Use in model control receiver

The circuit below shows a ZN414Z used as an IF amplifier for a 27MHz superhet receiver.



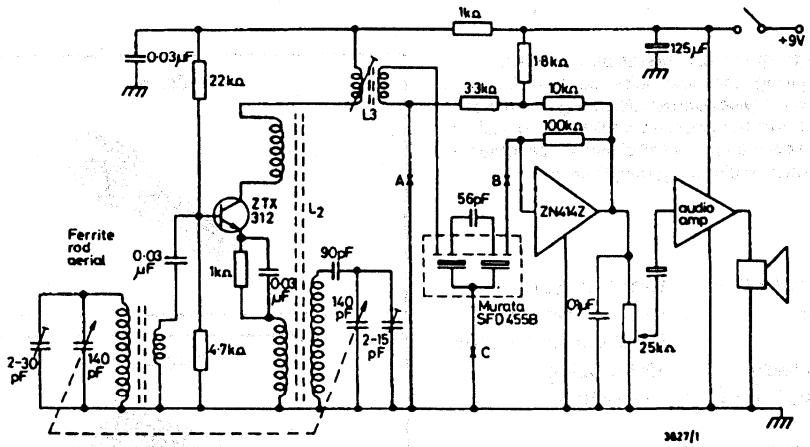
Performance Details:

Sensitivity = 2.5µV for a 5V p.t.p output measured at f_c = 27.21MHz.
100% modulated with 100Hz square wave.
Selectivity: ±5kHz for <100mV p.t.p output.
Input Signal Range: 2.5µV to 25mV (i.e. 80dB).
Supply Current: ≈ 4.5mA.

Fig.13

(d) Broadcast band superhet using ZN414Z

The ZN414Z coupled with the modern ceramic resonators offers a very good I.F. amplifier at modest cost, whilst maintaining simplicity and minimal alignment requirements. A typical circuit is shown below:



-6dB Bandwidth = 6kHz
-30dB Bandwidth = 8kHz
AGC Range = 40dB
(For 10dB change in A.F. output).

Fig.14

FURTHER APPLICATIONS

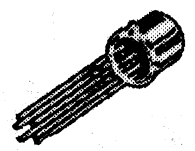
The ZN414Z is an extremely versatile device and, in a data sheet, it is not possible to show all its varied applications. A comprehensive applications note on the device is available which gives full details of various radio receivers, I.F. amplifiers and frequency standards together with comprehensive technical information.

ZN459, ZN459CP

ULTRA LOW NOISE WIDEBAND PREAMPLIFIER

A versatile high grade a.c. pre-amplifier designed for applications requiring ultra low noise such as infra-red imaging and low noise wide band amplifiers e.g. microphone, acoustic emission, transducer bridge amplifier. The matching of open loop gain coupled with small physical size make the ZN459 series ideal for multichannel amplification.

ZN459



CM6

ZN459CP

DP8

FEATURES

- High Controlled Gain : 60dB ±1dB typical
- Low Noise : 40Ω Equivalent Noise Resistance, or 800pV/√Hz
- Wide bandwidth : 15MHz typical
- Low Supply Current : <3mA from 5V

ABSOLUTE MAXIMUM RATINGS

Supply voltage	6 Volts
Operating Temperature Range:	
for ZN459	-55 to +125°C
for ZN459CP	0 to +70°C
Storage Temperature Range	-55 to +125°C

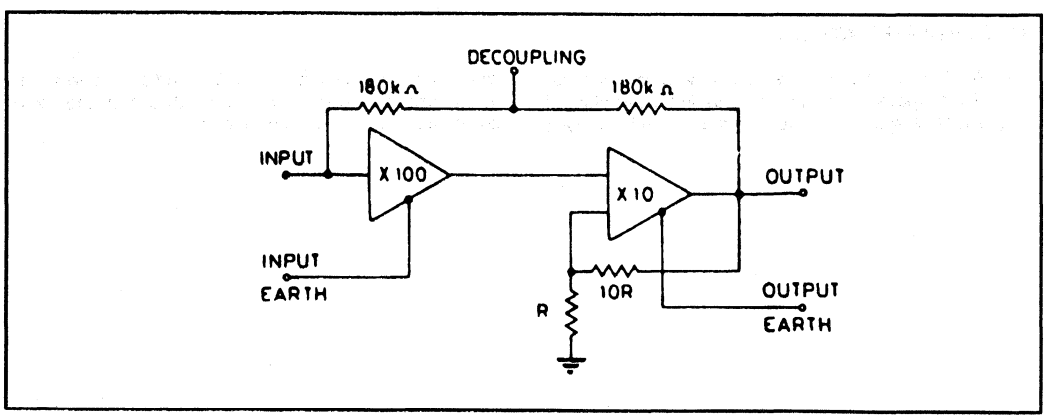


Fig.1 ZN459 Outline circuit

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
(V_{CC} = 5V, T_{amb} = 25°C)

Parameter	Min.	Typ.	Max.	Units	Conditions
Supply Current	2.0	2.5	3.0	mA	
Voltage Gain	59	60	61	dB	10KHz
TC of Voltage Gain		-0.2		%/°C	
V_{CC} Coefficient of Voltage Gain		25		%/V	
Cut-off Frequency		15		MHz	3dB down
Input Resistance	3.5	7		kΩ	10KHz
Input Capacitance		80		pF	Note 1
Noise Resistance		40		Ω	R_s = 0
White Noise Voltage		800	1100	pV/√HZ	R_s = 0
L.F. Spot Noise		3		nV/√HZ	R_s = 0, f = 25Hz
White Noise Current		1		pA/√HZ	
Output Level	1.5	2.0	2.5	V	
Supply Voltage Coefficient of Output Level		0.34		V/V	
Output Current Limit	0.6	0.8	1.1	mA	Sink current
Total Harmonic Distortion		0.15		%	1 Vpp at 10KHz
Output Resistance		75		Ω	10KHz
Supply Rejection Ratio		42.5		dB	
Delay Time		20		ns	Small signal
Delay Time		40		ns	100mV rms input
Positive Input Overdrive		10		mA	
Negative Input Overdrive		-5		V	

Note 1: In P.C.B. The input capacitance may be reduced to 25pF by screening between output and input.

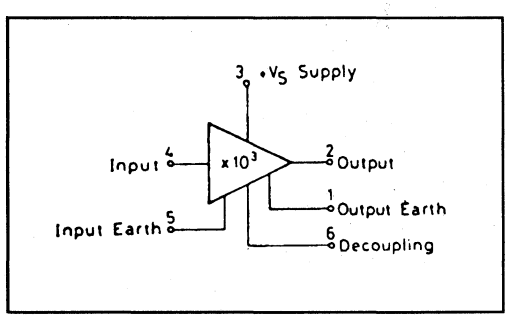


Fig.2 Pinning configuration - ZN459

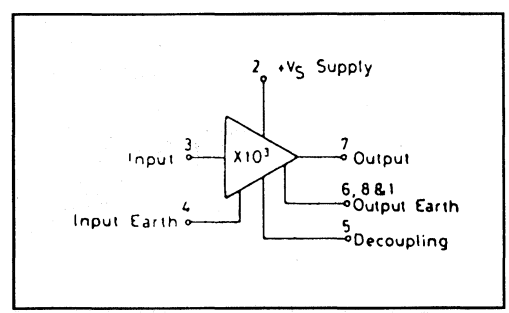


Fig.3 Pinning configuration - ZN459CP

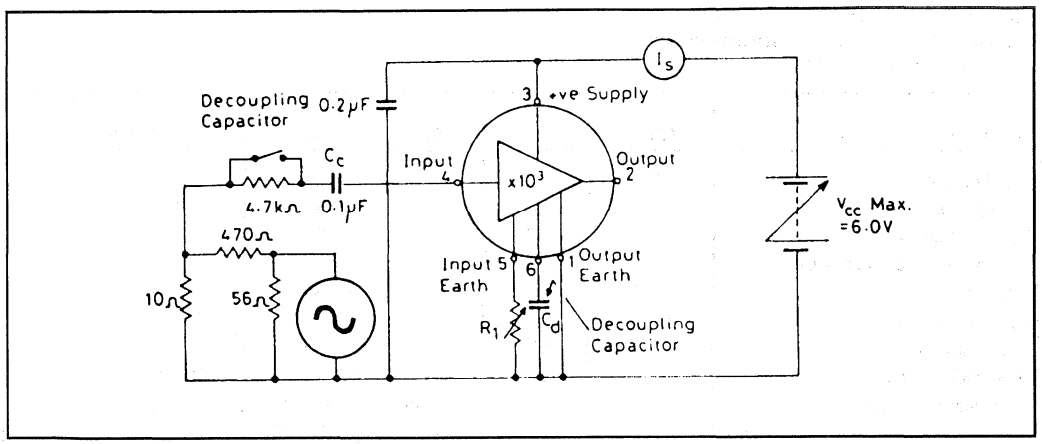


Fig.4 Gain Test Circuit (ZN459)

The input impedance may be increased at the expense of noise by including R_1 to vary the gain ($R_1 = 0$, gain = 10^3; R_1 = 470Ω, gain = 10^2).

C_d is required to decouple the internal feedback loop and in order to obtain a flat frequency response make $C_d \geq C_c$.

The earth lead of the supply decoupling capacitor should be as close as possible to that of R_1.

For optimum Common Mode Rejection connect a twisted pair between source and pins 4 and 5 of the device and complete the earth return from source ground.

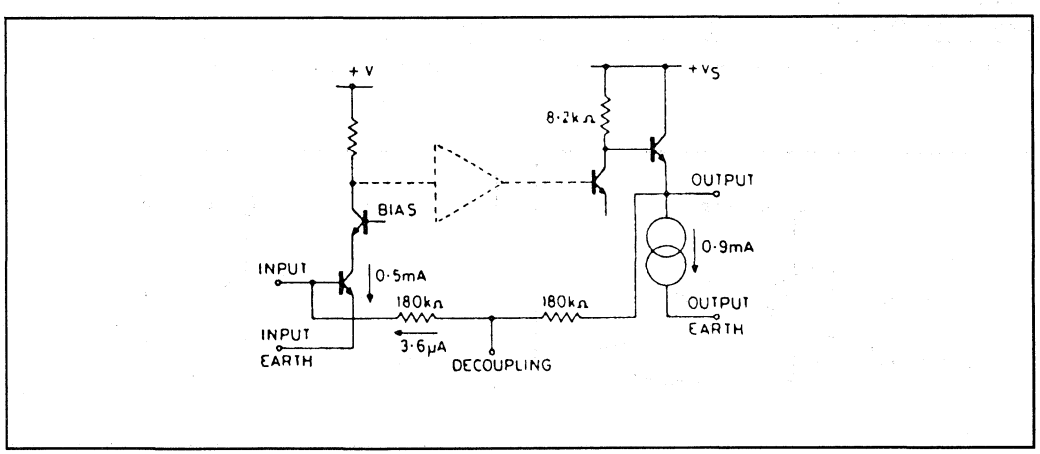


Fig.5 ZN459 Input and output circuit

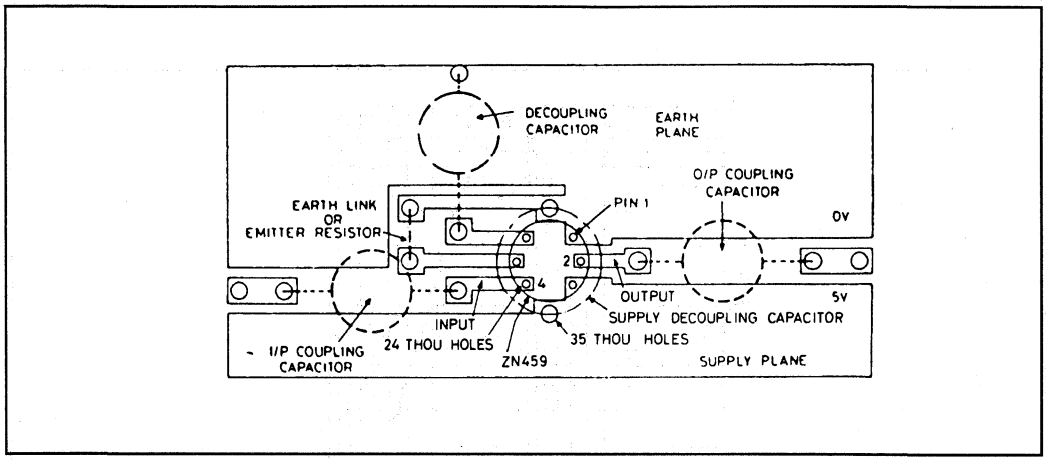


Fig.6 PCB layout (ZN459)

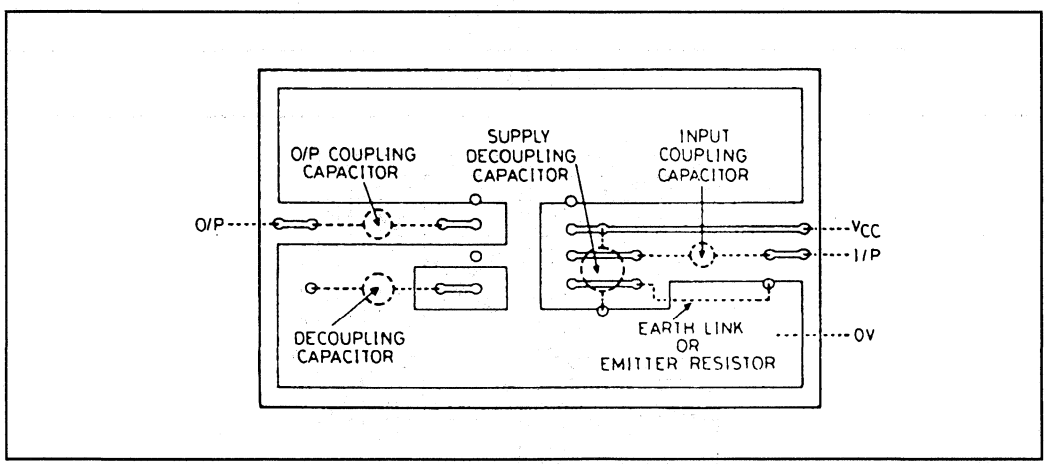


Fig.7 PCB layout (ZN459CP)

TYPICAL CHARACTERISTICS

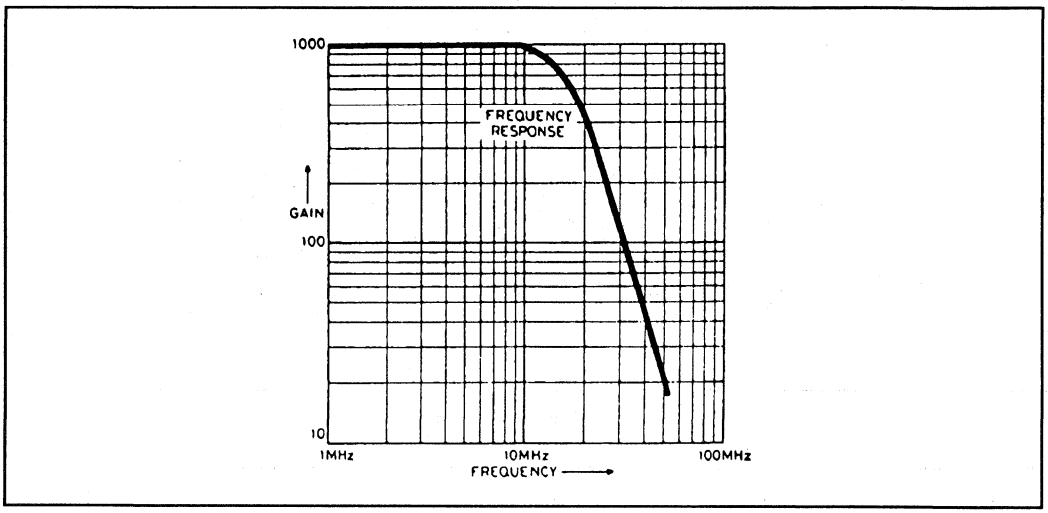


Fig.8 Gain V_s Frequency

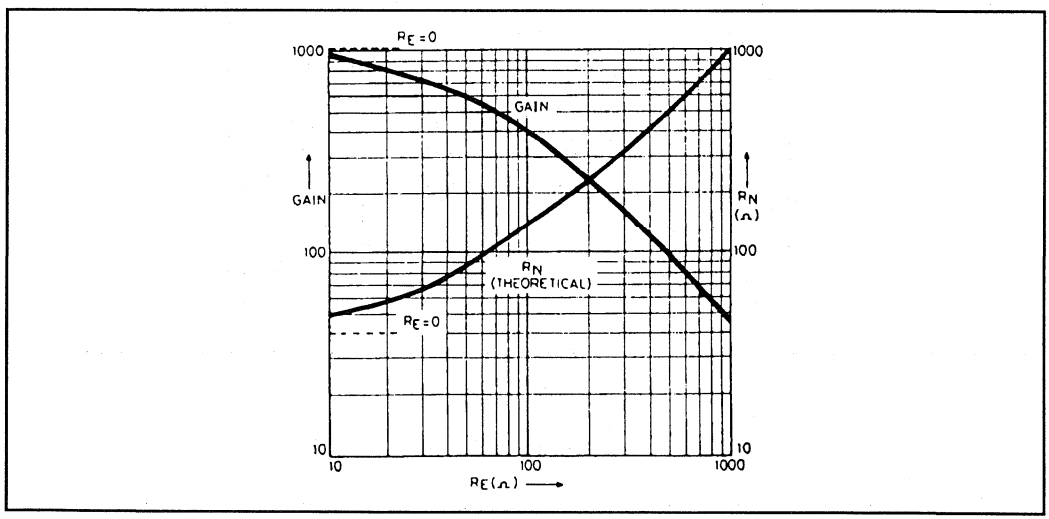


Fig.9 Gain and noise resistance V_s emitter resistance

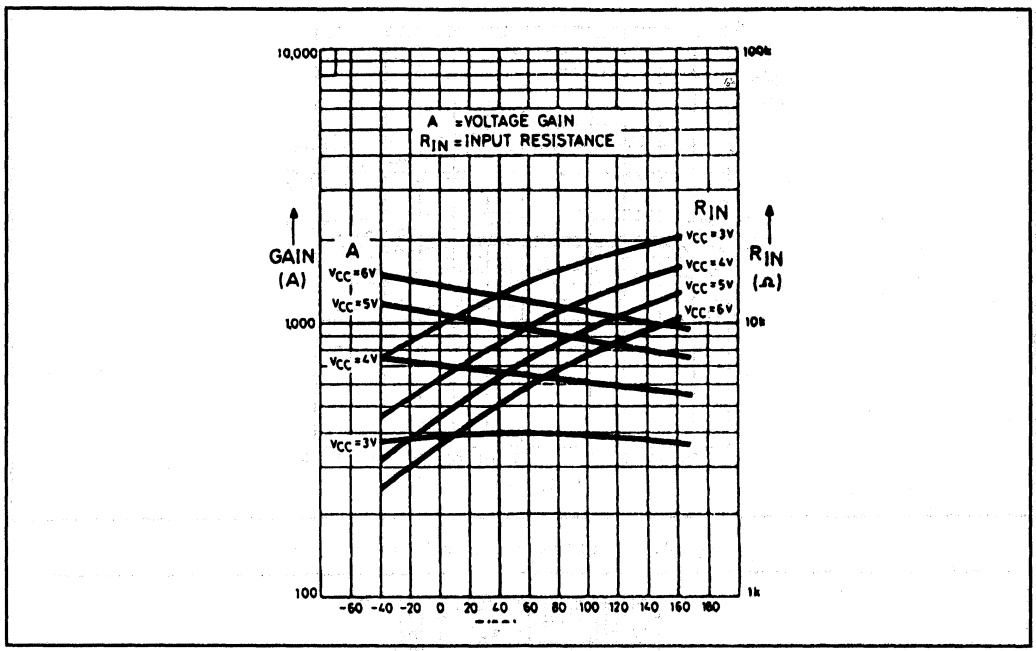


Fig.10 Gain and Input Impedance

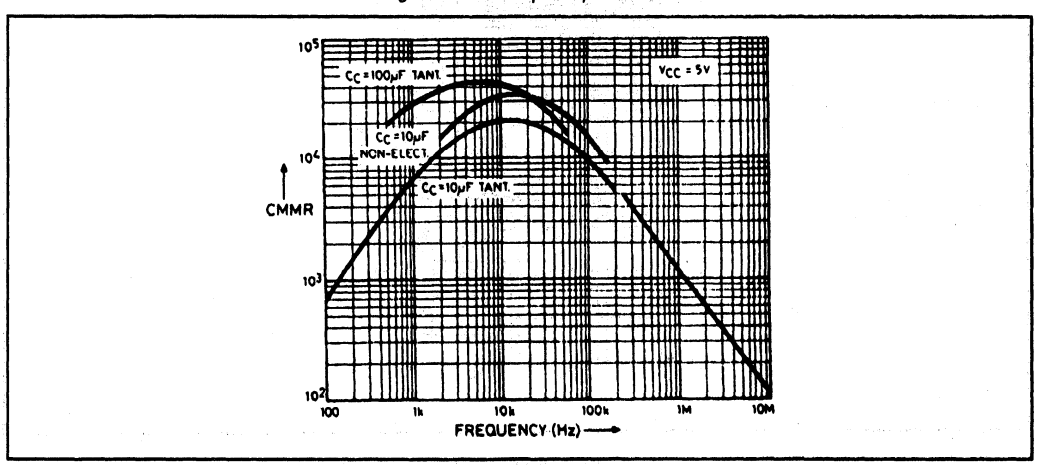


Fig.11 Common Mode Rejection Vs Frequency
(Measured between input earth and output earth)

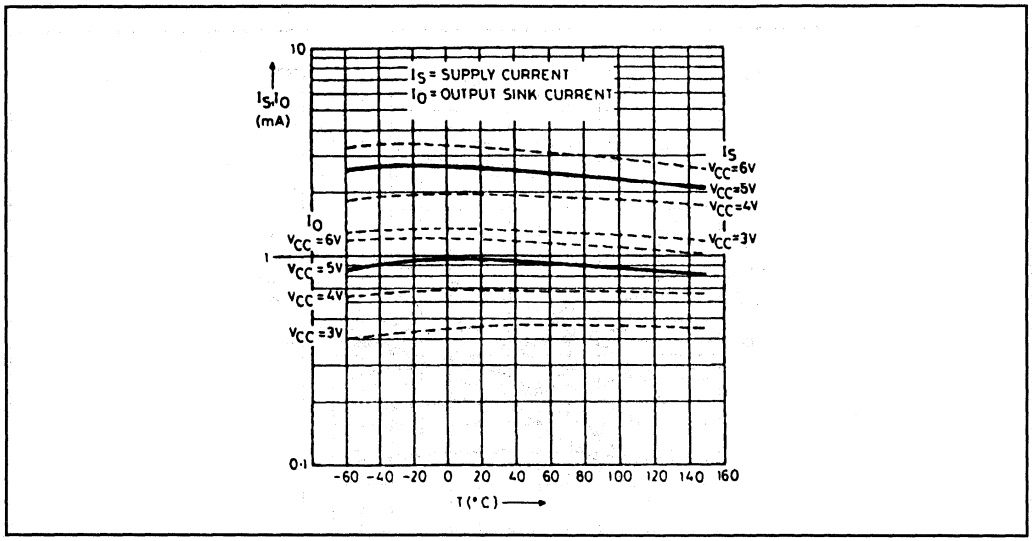


Fig.12 Supply Current and Output Sink Current

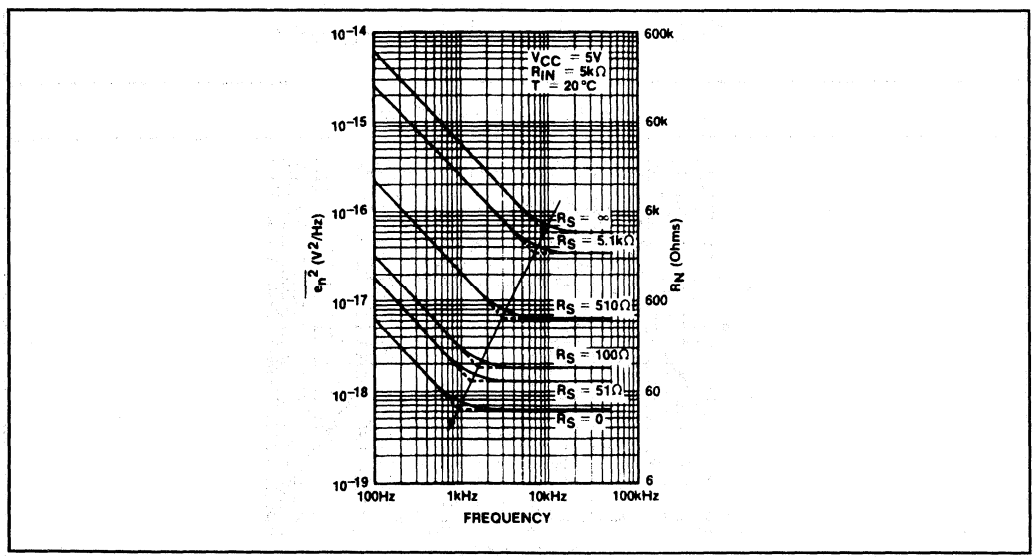


Fig.13 Noise Voltage

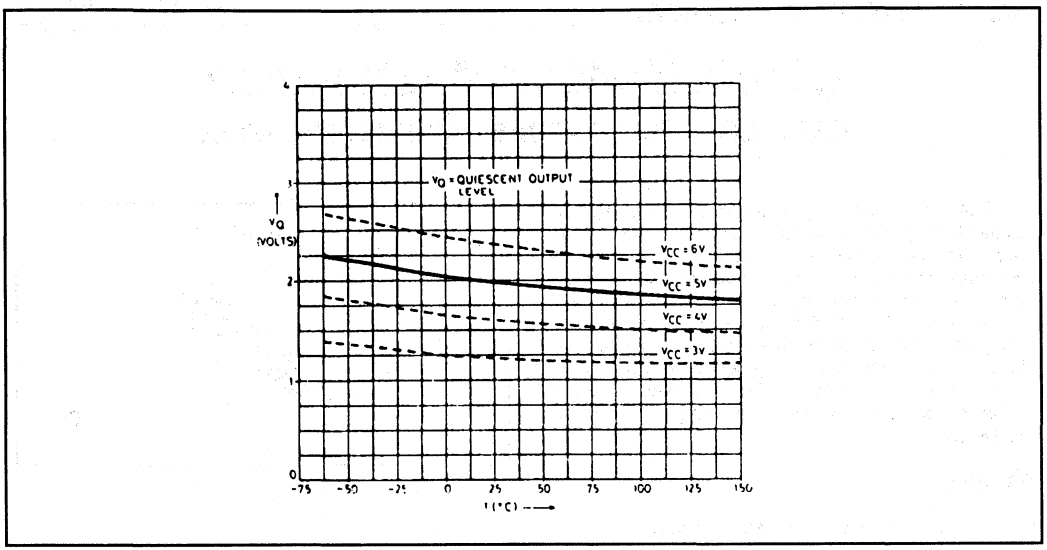


Fig.14 Quiescent Output Level

ZN460, ZN460AM, ZN460CP

ULTRA LOW NOISE WIDEBAND PREAMPLIFIER

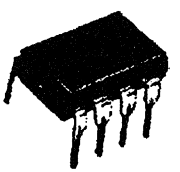
The ZN460 is a versatile high performance AC preamplifier, designed for applications requiring ultra low noise such as infra-red imaging and low noise wideband amplifiers e g microphone, acoustic emission, transducer bridge amplifier. The matching of open loop gain, coupled with small physical size. makes the ZN460 ideal for multichannel amplification.

The programmable gain feature allows variable detector gain factors to be trimmed out The programmable bandwidth feature allows the noise bandwidth to be reduced to the required signal bandwidth, thus minimising the wideband output noise

ZN460

CM8

ZN460CP



DP8

FEATURES

- High Controlled Gain : 60dB ±1dB typical
- Programmable Gain : 50-60dB typical
- Programmable Bandwidth : 6MHz downwards
- Low Noise : 40Ω Equivalent Noise Resistance, or 800pV/√Hz
- Low Supply Current : <3mA from 5V

ABSOLUTE MAXIMUM RATINGS

Supply voltage	6 Volts
Operating Temperature Range:	
for ZN460 and ZN460AM	-55 to +125°C
for ZN460CP	0 to +70°C
Storage Temperature Range	-55 to +125°C

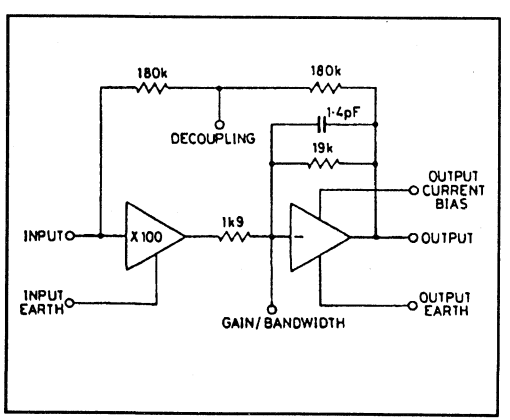
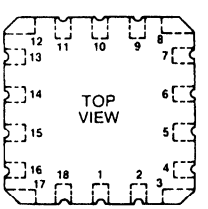


Fig.1 Circuit diagram

ZN460AM



LC18

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
(V_{CC} = 5V, T_{amb} = 25°C)

Parameter	Min.	Typ.	Max.	Units	Conditions
Supply Current	2.0	2.5	3.0	mA	
Voltage Gain	59	60	61	dB	10KHz (Note 1)
TC of Voltage Gain		-0.2		%/°C	
V_{CC} Coefficient of Voltage Gain		25		%/V	
Cut-off Frequency		6		MHz	3dB down (Note 1)
Input Resistance	3.5	7		kΩ	10KHz
Input Capacitance		80		pF	Note 2
Noise Resistance		40		Ω	R_S = 0
White Noise Voltage		800	1100	pV/√HZ	R_S = 0
L.F. Spot Noise		3		nV/√HZ	R_S = 0, f = 25Hz
White Noise Current		1		pA/√HZ	
Output Level	1.5	2.0	2.5	V	
Output Swing		4		Vpp	R_F = ∞
	2			Vpp	R_F = 6KΩ
Supply Voltage Coefficient of Output Level		0.34		V/V	
Output Current Limit	0.6	0.8	1.1	mA	Note 3
Total Harmonic Distortion		0.15		%	1 Vpp at 10KHz
Output Resistance		75		Ω	10KHz
Supply Rejection Ratio		42.5		dB	
Delay Time		20		ns	Small signal
Delay Time		40		ns	100mV rms input
Positive Input Overdrive			10	mA	
Negative Input Overdrive			-5	V	

Note 1: Without external components

Note 2: In P.C.B. The input capacitance may be reduced to 25pF by screening between output and input.

Note 3: Sink current without external bias resistor

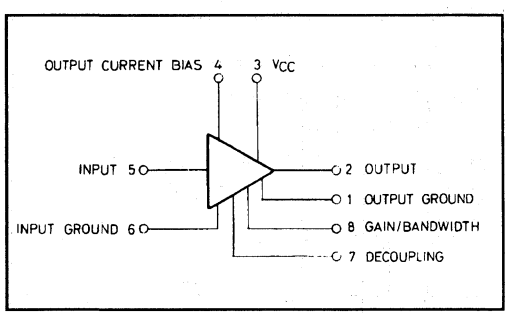


Fig.2 Pinning configuration - ZN460 and ZN460CP

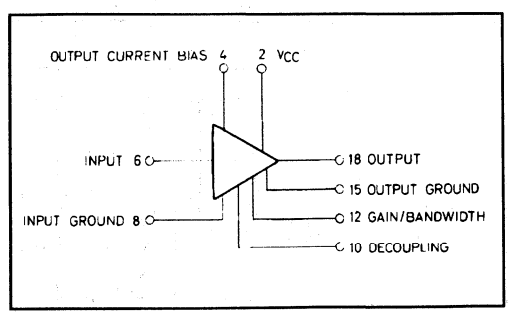


Fig.3 Pinning configuration - ZN460AM

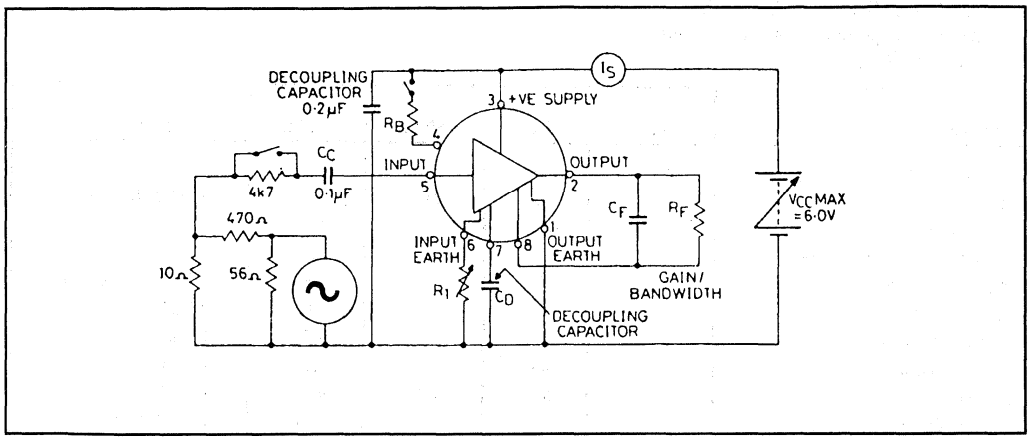


Fig.4 Gain Test Circuit (ZN460)

The input impedance may be increased at the expense of noise by including R_1 to vary the gain ($R_1 = 0$, gain = 10^3; $R_1 = 470\Omega$, gain = 10^2).

C_D is required to decouple the internal feedback loop and in order to obtain a flat frequency response make $C_D \geq C_C$.

The earth lead of the supply decoupling capacitor should be as close as possible to that of R_1.

R_B may be used to increase the output quiescent current up to a maximum of 5 mA. The value is given by:

$$I_O = \frac{10\ (Vcc - 1.34)}{R_B'}$$

Where R_B' is the parallel combination of R_B and 40KΩ.

The gain and bandwidth may be modified by means of R_F and C_F. The gain is given by:

$$A = \frac{10^3 . R_F}{R_F + 19} \quad \text{with } R_F \text{ in k}\Omega$$

and the bandwidth by :

$$f_c = \frac{10^{12}}{2\pi R_F' (C_F + 1.4)} \quad \text{Hz with } C_F \text{ in pF}$$

Where R_F' is the parallel combination of R_F and 19KΩ.

The recommended minimum value of R_F is 6KΩ since a lesser value reduces the output swing below $2V_{pp}$.

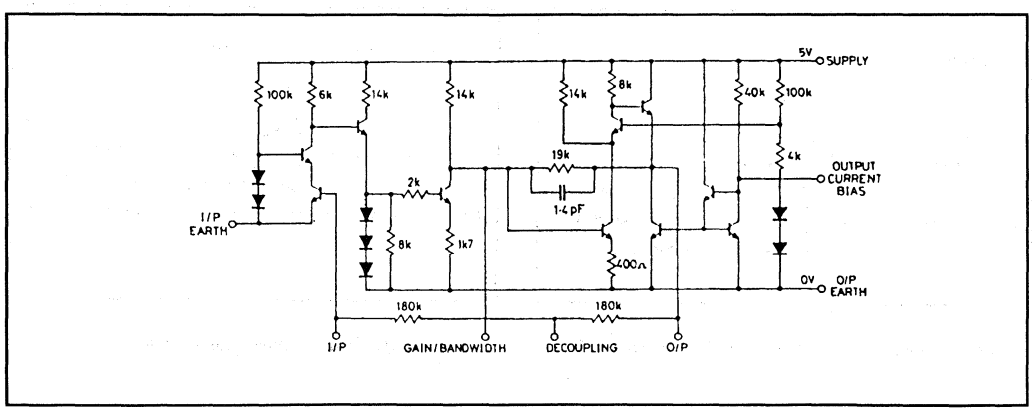


Fig.5 ZN460 Circuit digram (typical values)

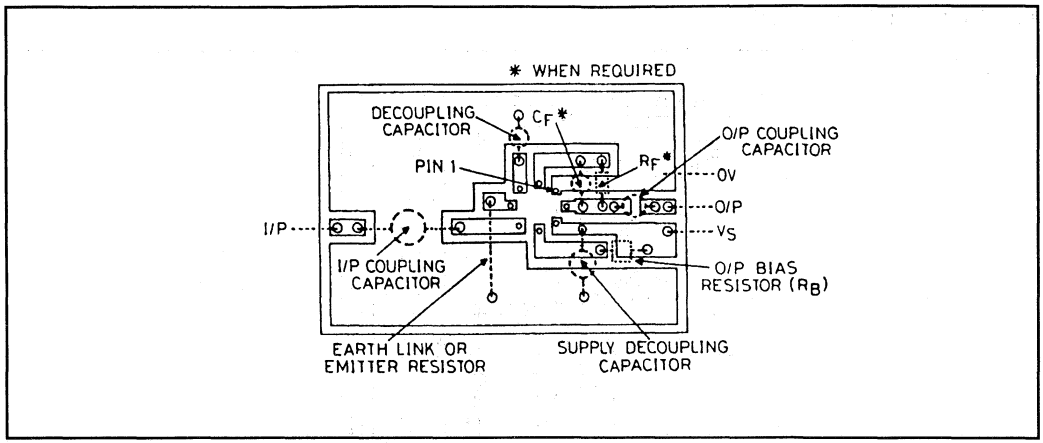


Fig.6 PCB Layout - ZN460

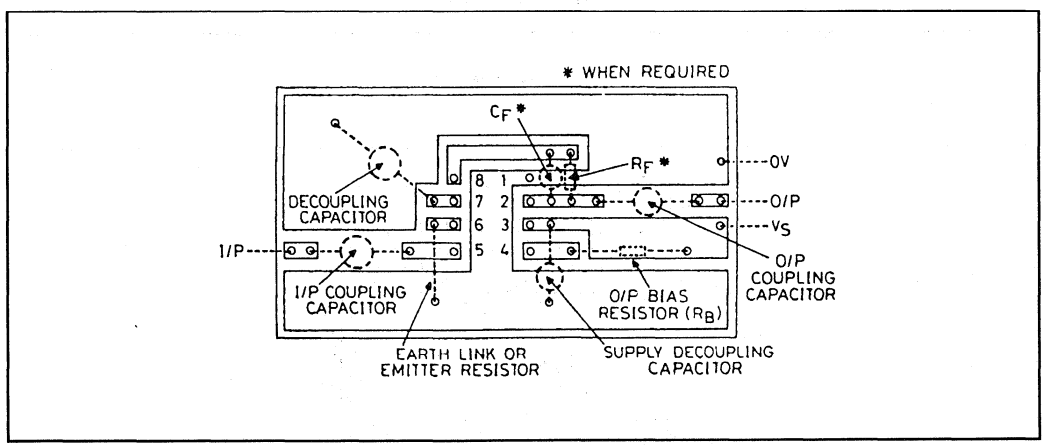


Fig.7 PCB Layout - ZN460CP

TYPICAL CHARACTERISTICS

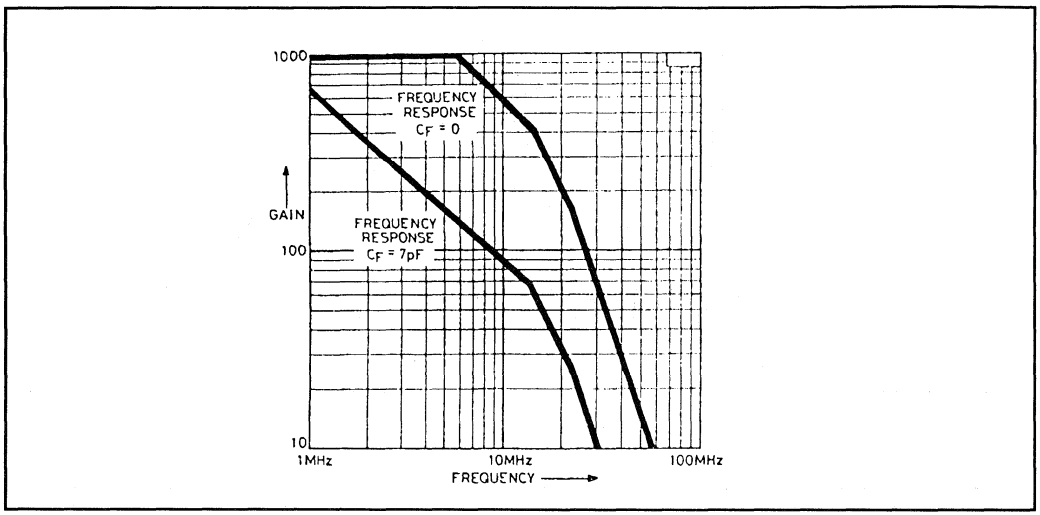


Fig.8 Gain V_s Frequency ($R_F = \infty$)

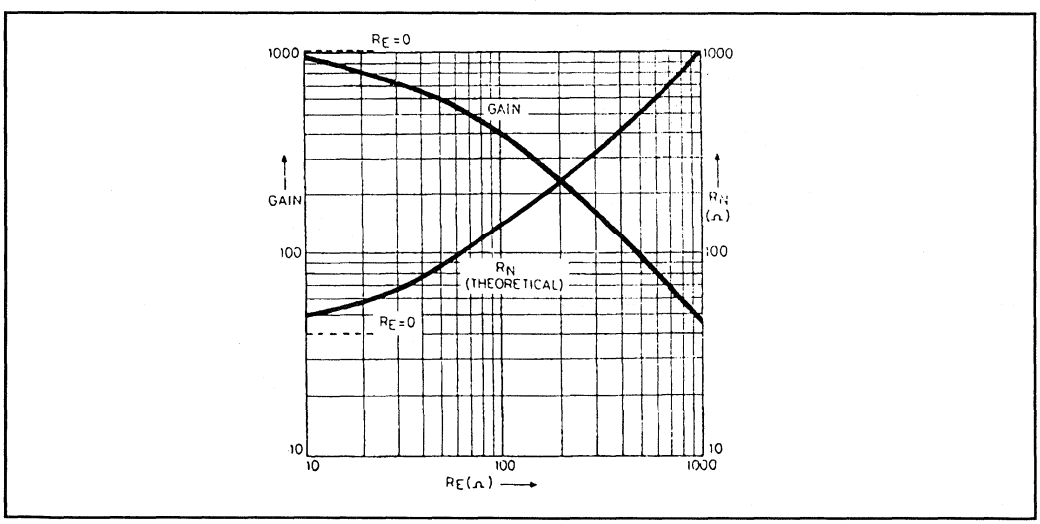


Fig.9 Gain and noise resistance V_s emitter resistance ($R_F = \infty$)

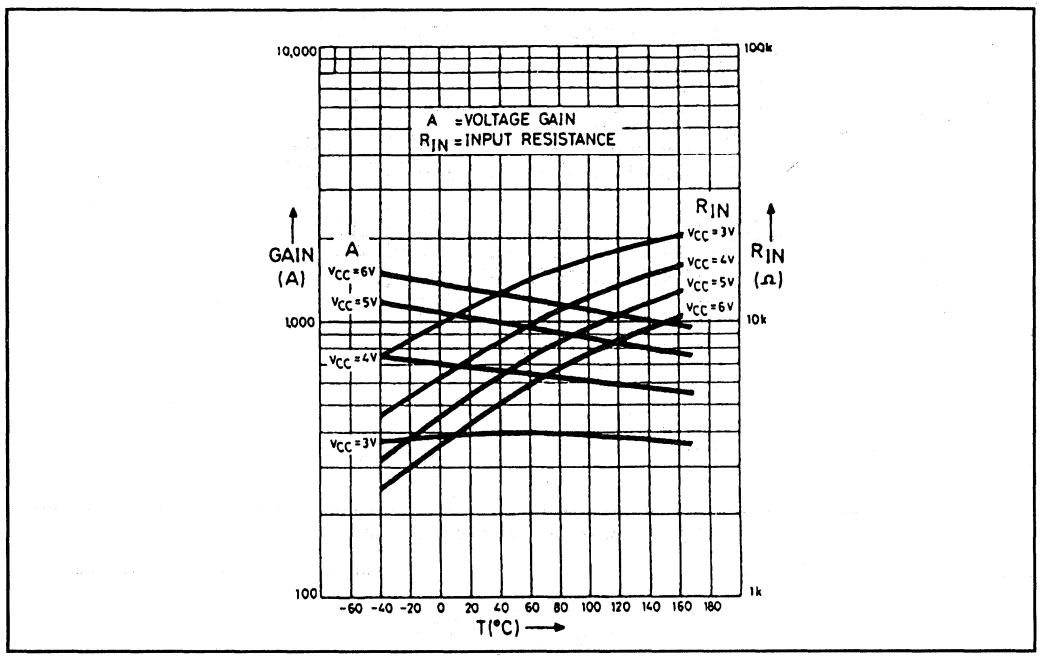


Fig.10 Gain and Input Impedance

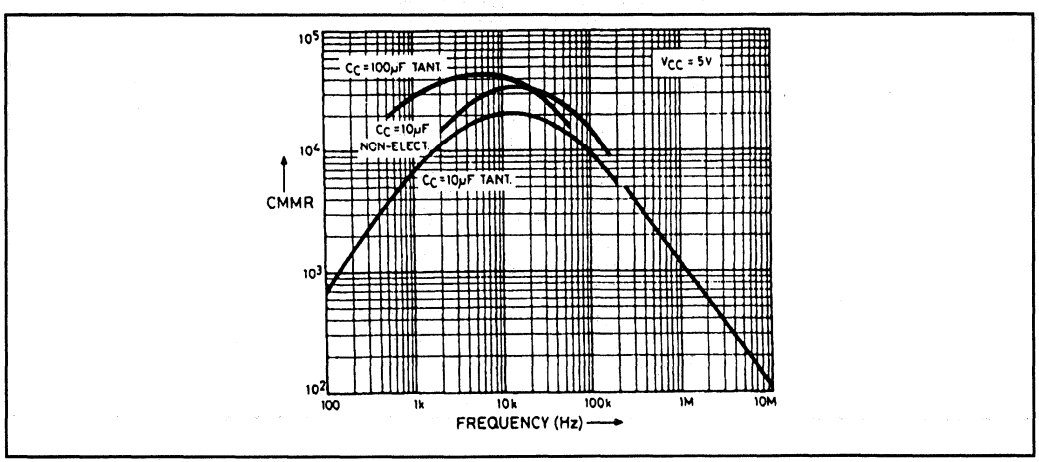


Fig.11 Common Mode Rejection Vs Frequency
(Measured between input earth and output earth)

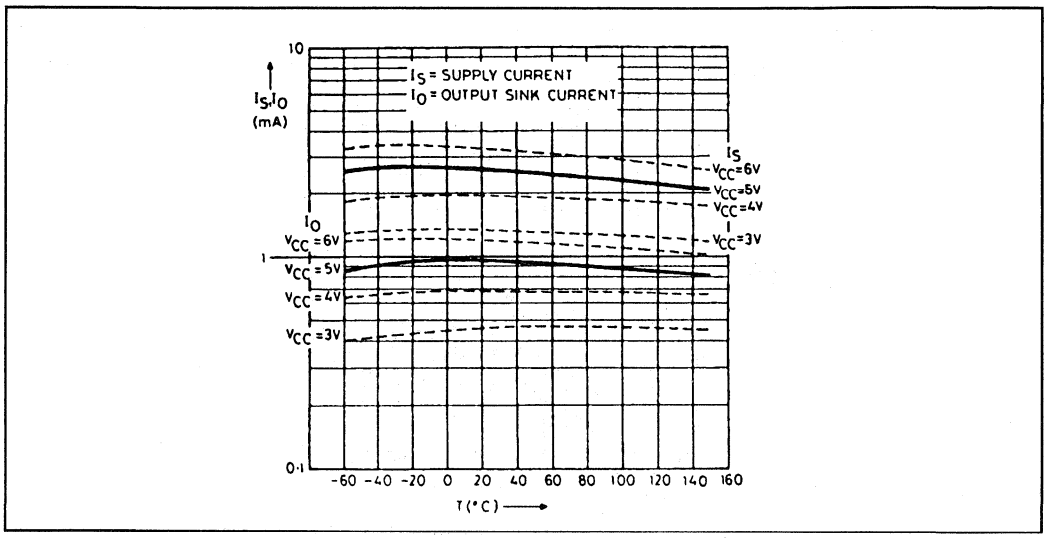


Fig.12 Supply current and output sink current

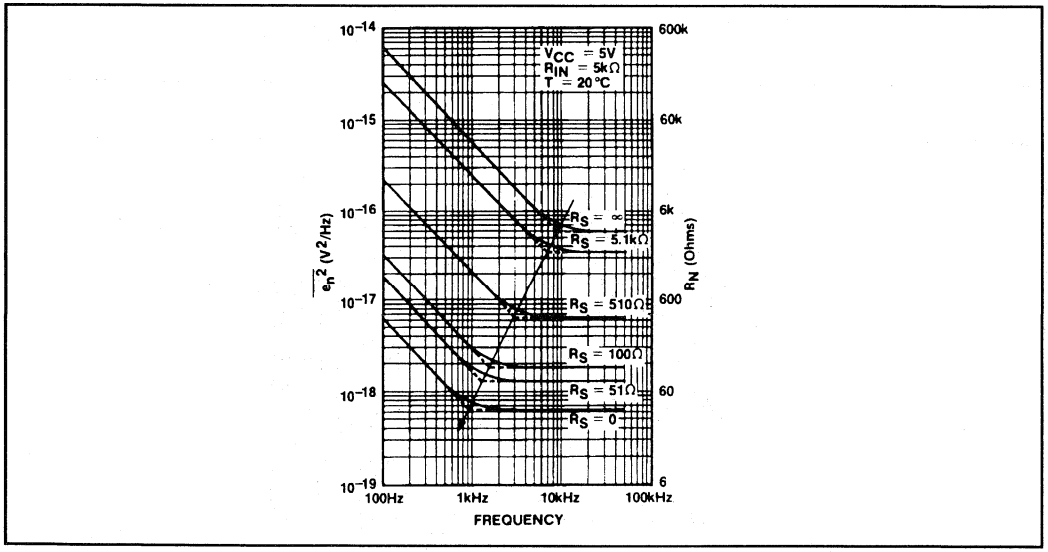


Fig.13 Noise voltage

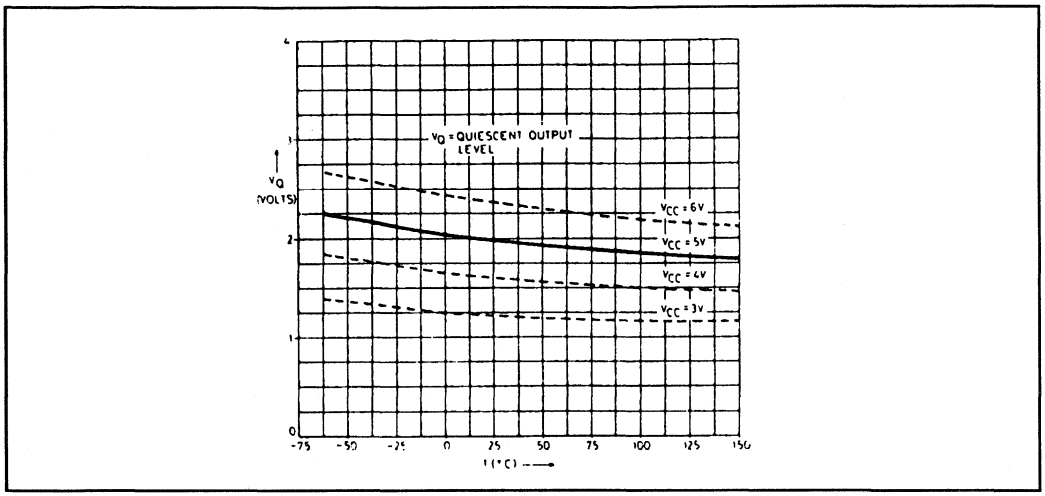


Fig.13 Quiescent Output Level

Section 2
Frequency Synthesisers

MIL-STD-883 Class B

Many of the integrated circuits detailed in this section are available screened in conformance with MIL-STD-883 Class B and are identified in their ordering codes by the letters **AC** immediately following the device type number. Separate data sheets for these circuits are available from your local GEC Plessey Semiconductors Sales Office.

GEC PLESSEY
SEMICONDUCTORS

SP2002

350/400MHz DIRECT FREQUENCY SYNTHESISER

(Supersedes version in May 1991 Professional Products IC Handbook)

The SP2002 is a Direct Frequency Synthesiser (DFS) with square and selectable sine or triangular output waveforms available from on–chip 8–bit D–A converters.

The maximum programmable output frequency and resolution is dependant on the clock frequency. With a clock frequency of 1.074GHz the output frequency can be programmed in 0.5Hz steps from 0.5Hz to 268MHz by means of an externally applied binary word. Inputs are ECL 100k compatible.

The SP2002 is the first in a new range of DFS products.

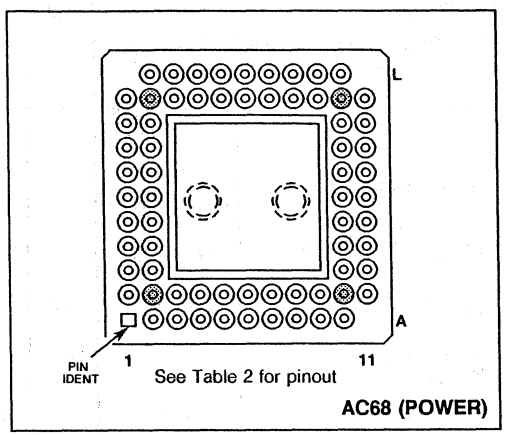


Fig.1 Pin connections - bottom view

FEATURES

- 400MHz Output Frequency
- In–Phase (I) and Quadrature (Q) Outputs
- 0.5Hz resolution with 1074MHz Clock
- Sine, Square or Triangle Output

APPLICATIONS

- LO Synthesis in Frequency Agile Radio/Radar
- ECM/ECCm
- Deceptive Countermeasures
- Multi–Function Radio
- Instrumentation

ORDERING INFORMATION

SP2002/B/AC Industrial Temperature Range PGA Package
SP2002/A/AC Military Temperature Range PGA Package
SP2002/AA/AC GPS HiRel Level 'A'
SP2002/AB/AC GPS HiRel Level 'B'

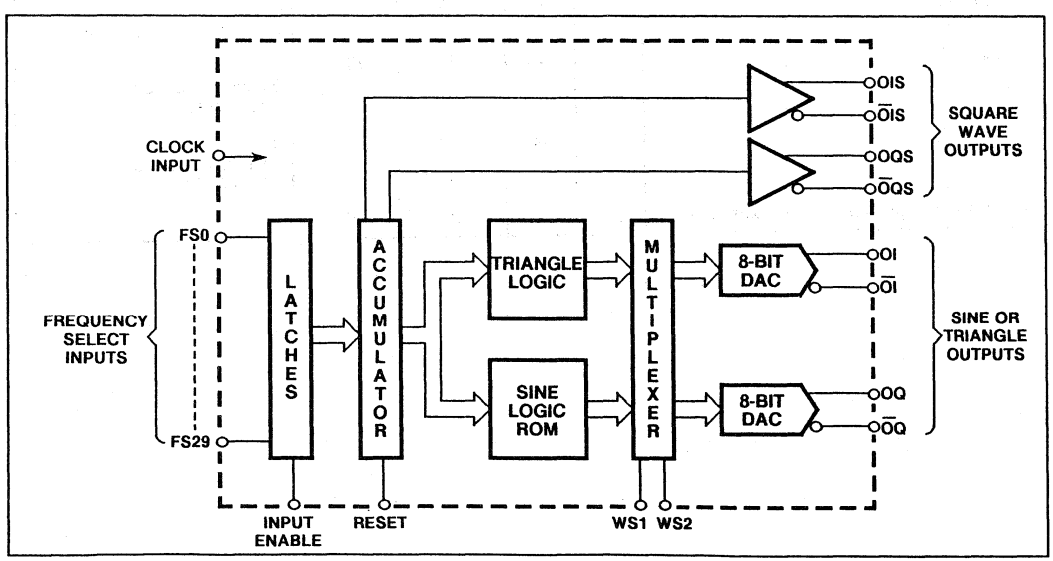


Fig. 2 SP2002 direct frequency synthesiser block diagram

ELECTRICAL CHARACTERISTICS

Guaranteed over the following temperature and supply voltage range.
A grade V_{EE} = - 4.25V to -4.75V, T_{CASE} = -55°C to +125°C Clock input fc = 100MHz to 1.4GHz
B grade V_{EE} = -4.25V to -4.75V, T_{CASE} = -40°C to +85°C, Clock input fc = 100MHz to 1.6GHz

Test conditions (unless otherwise stated)
Supply Voltage: V_{EE} = -4.25V and -4.75V V_{IL} = -1.67V, V_{IH} = -1V
A grade, Temperature T_{CASE} = -55°C and +125°C, fc = 1.4GHz
B grade, Temperature T_{AMB} = 25°C, fc = 1.6GHz

Characteristic	Signal Name	Value			Units	Conditions
		Min	Typ	Max		
Supply current	I_{EE}	0.85	1.1	1.35	A	Note 1
Sine/Triangle Output Current	OQ (bar) OQ OI (bar) OI	14	24	32	mA p-p	See Operating Notes, fOUT = $\frac{fc}{2^9}$
Square Wave Output Current	OQS(bar) OQS OIS(bar) OIS	6	11	16	mA p-p	See Operating Notes fOUT = $\frac{fc}{2^9}$
ECL Input Bias Current, all I/Ps except Clock	FS0-FS29 I/P EN, RESET		150		µA	
Waveform Select Input Current	WS1, WS2		1		mA	V_{IH} = 0V
Waveform Select Input High Voltage	WS1, WS2	-0.5V		0V	V	
Waveform Select Input Low Voltage	WS1, WS2	$-V_{EE}$		$-V_{EE}$ + 0.5	V	
Clock Input Current	CLOCK		40		µA	
Output Frequency Range	All Outputs			$\frac{fc}{4}$	Hz	Note 2
Channel Spacing	All Outputs	0.5			Hz	fc = 1.074GHz, Note 2
Close to Carrier Noise			-135		dBc/Hz	10kHz offset, Note 6
Spurious Output levels	Sine Output					In 10kHz Bandwidth
$f_{out} = \frac{fc}{2^9}$			-48	-45	dBc	Note 3 Decimal input code = 8389631
$f_{out} = \frac{fc}{2^4}$			-45	-41	dBc	Note 3 Decimal input code = 167773183
$f_{out} = \frac{fc}{2^3}$			-30	-20		Note 3 Decimal input code = 268436479
1/4 Crossover Spurious	Sine Output		-30	-21	dBc	

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Signal Name	Value			Units	Conditions
		Min	Typ	Max		
2nd Harmonic Content $F_{OUT} = \frac{fc}{2^9}$	Sine Output		-55	-40	dBc	
3nd Harmonic Content $F_{OUT} = \frac{fc}{2^9}$	Sine Output		-43	-35	dBc	
5nd Harmonic Content $F_{OUT} = \frac{fc}{2^9}$	Sine Output		-50	-30	dBc	
Frequency Change Range Time		8		40	Clock Cycle	Note 4
Package Thermal Resistance Chip to Case			4		°C/W	Note 5

NOTES
(1) The power taken by the synthesiser depends upon the 'Waveform Select' inputs (see Fig. 2). The I_{EE} current quoted is for the square wave plus sine wave 'I' and 'Q' outputs where all the SP2002 circuitry is powered up. The output waveform options and associated I_{EE} currents are shown in Table 1. (2) The SP2002 will operate at any clock frequency below 1.6 GHz e.g. at f_c = 214MHz, output frequency range = 0.1Hz to 50MHz in steps of 0.1Hz. (3) Levels refer to the highest rather than total spurious power. A sine wave output and clock frequency of 1.6 GHz is assumed. These figures will degrade by 10 to 20dB for triangle and 20 to 30dB for square wave output. (4) Minimum figure assumes only MSB Frequency Set Input is changed. Maximum figure assumes LSB Frequency Set Input is changed. (5) A suitable heatsink should be attached to the studs on the top of the package. (6) Assuming no spurious output at the offset frequency.

ABSOLUTE MAXIMUM RATINGS

Storage temperature range	-55°C to +150°C
Supply voltage (V_{EE})	-6V
Input voltages	V_{EE} to +0.5V
Junction temperature	+150°C

CIRCUIT DESCRIPTION

The sine, triangle or square wave output frequency is determined by a parallel 30 bit Frequency Set binary input word. With a clock input rate of 1.074GHz, the output frequency can be incremented in 0.5Hz steps from 0.5Hz to 268MHz. In phase ('I') and Quadrature ('Q') outputs are provided for all three waveform options, as are true and complementary phase outputs. Due to the internal organisation of the chip the maximum output frequency is limited to a quarter of the clock frequency.

Referring to the block diagram of Fig. 2, Waveform Select (WS) pins are provided to enable programming of different output waveform combinations by hard-wiring to the supplies as shown (see Table 1). Depending on the output option chosen, unused circuitry on-chip is automatically turned off to conserve power.

A Reset input is provided to initialise the internal circuits and allow the output waveforms to start from a known state as shown in Fig.4. Input Frequency Set data can be latched if required, by holding the Input Enable pin high.

Referring to Fig. 2, the basic operation is as follows. Frequency Set data is entered via the data latches to an accumulator which is incremented by the clock input.

The accumulator MSB output provides the square wave. The 8 MSB outputs are used to generate the sine and triangle functions. The output of the accumulator is effectively a sawtooth which is converted to a triangle by the triangle logic. The sinewave is generated by circuitry including a ROM containing a quadrant of sinewave data which, with the associated logic, produces a complete sinewave in digital form. A multiplexer selects triangle or sine output under the control of the Waveform Select pins. The analog triangle or sine outputs are generated via 8-bit DACs.

OPERATING NOTES

The SP2002 is a very high speed ECL circuit with a maximum clock frequency in excess of 1.6GHz and output frequency capability above 400MHz. In order to achieve correct operation at these frequencies and to ensure output waveform integrity, attention must be paid to the layout of the application board. The use of a ground plane and good RF techniques is recommended. Power supply pins should be well decoupled using high frequency capacitors. All power supply and ground pins must be connected.

The clock input is 100k ECL compatible and if a relatively low frequency clock is required the input may be driven directly from a 100k ECL gate with a 50 Ohm termination resistor to -2V mounted close to the clock pin. At frequencies greater than a few hundred MHz, clock drive from ECL is not practicable and a sinewave drive ac-coupled to the clock input may be used. The application diagram in figure 4 shows a typical arrangement where the 68 Ohm and 160 Ohm resistors set a suitable bias voltage for the clock input and also provide a 50 Ohm termination for the connecting cable or stripline. A suitable drive level is +4dBm or 1V p-p, but at very high clock frequencies this may need to be increased by a few dB to make up for losses.

The frequency set, input enable and reset inputs are 100K ECL compatible, and when very fast frequency hopping is required, for instance when generating chirp waveforms the input data will necessarily come from an ECL source. Many other applications may require much slower data which may be generated from a CMOS source. CMOS data cannot be connected directly to the SP2002 inputs since the high logic is equal to the positive supply which would saturate the input transistors and cause the circuit to malfunction.

A possible interface to CMOS logic is shown in Fig. 3 where the CMOS positive power rail is dropped approximately 0.7V below that feeding the SP2002 by including a diode in series with the CMOS supply.

The low logic level for the SP2002 may be equal to the VEE supply but should not be taken more negative.

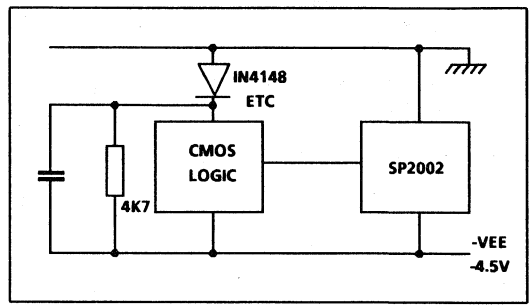


Fig. 3 Interface to CMOS Logic

The output frequency and step size is a function of the clock rate and the frequency select data. The output frequency can be calculated from the formula

$$fout = \frac{Kfc}{2^N} \text{ where } N = 31, \text{ the number}$$

of bits in the accumulator, fc is the clock frequency and K the number on the frequency select inputs.

The minimum output frequency and step size are given by

$$fmin = \frac{fc}{2^N}$$

The reset pin sets the 31 bit accumulator to zero regardless of the state of any other inputs.

The input is active high and when reset, the sine triangle and square wave outputs remain at the level obtained when the accumulator reaches zero in dynamic operation. The effect of the Input enable and Reset inputs is shown diagramatically in figure 4.

All the outputs are current sources, the sine and triangle outputs being obtained from the DAC outputs whilst the square wave outputs are fed from a separate buffer circuit driven direct from the accumulator MSB. Normally the output signal is obtained by loading the output with a 50 Ohm resistor to ground, but in practice the resistor can be any value from zero to 50 Ohms allowing control of the output voltage. If necessary the output load resistor can be returned to an output voltage up to 1V more positive than ground. This feature may be used to produce output signals symmetrical about ground, in the case of the sine triangle outputs, 50 Ohm resistors connected to +0.5V will produce ≃ 1V peak to peak output centred about ground.

A heatsink is required to maintain the chip operating temperature at a safe value. The heatsink should be attached to the studs on the top of the package using M3 nuts. A thermal resistance of 10°C/W is suitable for operation at 25°C.

The frequency select input is positive logic, ie the minimum output frequency is obtained when the LSB is high and all other inputs low.

All frequency select inputs have a nominal 30K input pull down resistor to VEE and will therefore be pulled low if left open circuit.

The waveform select pins WS1 and WS2 are intended to be hard wired to VEE or ground depending on the output waveform requirements. When necessary, the inputs could be switched using external transistors provided the minimum level requirements specified in the table of characteristics are met. The waveform select inputs should not be left open circuit.

The input Enable pin controls entry of input data to the input latches. When the input is low the input latches are transparent and any data change results in a change to the output frequency. When the input is taken high the data present on the frequency select inputs before the low to high transition is retained on the input latches and sets the output frequency.

The frequency select input can be changed without changing the output frequency until the frequency select input is again taken low, and the new data enters the latches. The Input Enable pin has an internal nominally 30K pull down resistor to VEE and will therefore go low if left open circuit.

Waveform Select input		Output waveform selected	I_{EE} (A) TYP	Power (W)
WS1	WS2			
V_{EE}	V_{EE}	Square wave 'I' and 'Q' Triangle 'I' and 'Q'	1.0	4.5
GND	V_{EE}	Square wave 'I' and 'Q' Sine wave 'I'	1.0	4.5
V_{EE}	GND	Square wave 'I and Q'	0.6	2.7
GND	GND	Square wave 'I' and 'Q' Sine wave 'I' and 'Q'	1.1	5.0

Table 1 Output waveform options

Pin No.	Pin name	Pin No.	Pin name
B1	WS2	K11	FS23
B2	WS1	K10	FS24
C1	TDI	J11	FS25
C2	TRC	J10	FS26
D1	RESET	H11	FS27
D2	GND	H10	FS28
E1	GND	G11	FS29
E2	V_{EE}	G10	I PEN
F1	GND	F11	CLOCK
F2	FS0	F10	V_{EE}
G1	FS1	E11	GND
G2	FS2	E10	GND
H1	FS3	D11	GND
H2	FS4	D10	TOQ
J1	FS5	C11	TOI
J2	FS6	C10	$\overline{O}$QS
K1	FS7	B11	OQS
L2	FS8	A10	$\overline{O}$IS
K2	FS9	B10	OIS
L3	FS10	A9	IC
K3	FS11	B9	NC
L4	FS12	A8	$\overline{O}$Q
K4	FS13	B8	OQ
L5	FS14	A7	NC
K5	GND	B7	V_{EE}
L6	V_{EE}	A6	GND
K6	FS15	B6	IC
L7	FS16	A5	NC
K7	FS17	B5	$\overline{O}$I
L8	FS18	A4	OI
K8	FS19	B4	NC
L9	FS20	A3	V_{EE}
K9	FS21	B3	GND
L10	FS22	A2	NC

Table 2 SP2002 pin assignment. IC pins are not required for normal use but should be left open.

Pin name	Function
WS1, WS2	Waveform select, see Table 1.
TDI, TRC, TOQ,TOI	Test pins only. Not required for normal operation. Leave open circuit.
RESET	A logic '1' on this pin resets the accumulator
FS0-FS29	Frequency Select inputs. FS0 is the LSB.
I PEN	Frequency Select Input Enable. A logic '1' on this pin latches data into the accumulator.
CLOCK	Clock input.
OQS, OIS	Square wave outputs.
OQ, OI	Sine or triangle outputs.
GND	0V
V_{EE}	Negative power supply (-4.5V).
NC	Not connected.

Table 3 SP2002 pin descriptions

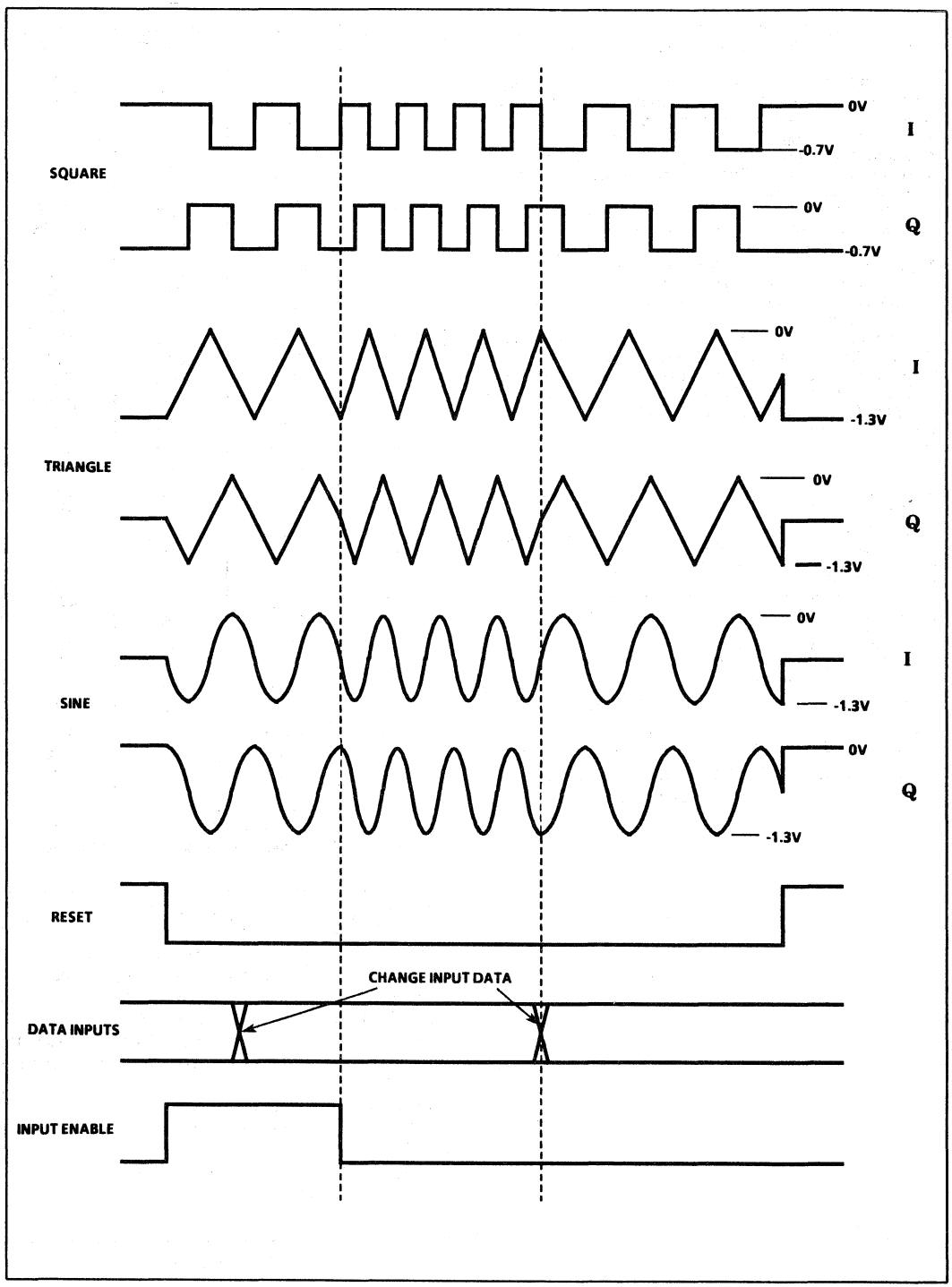
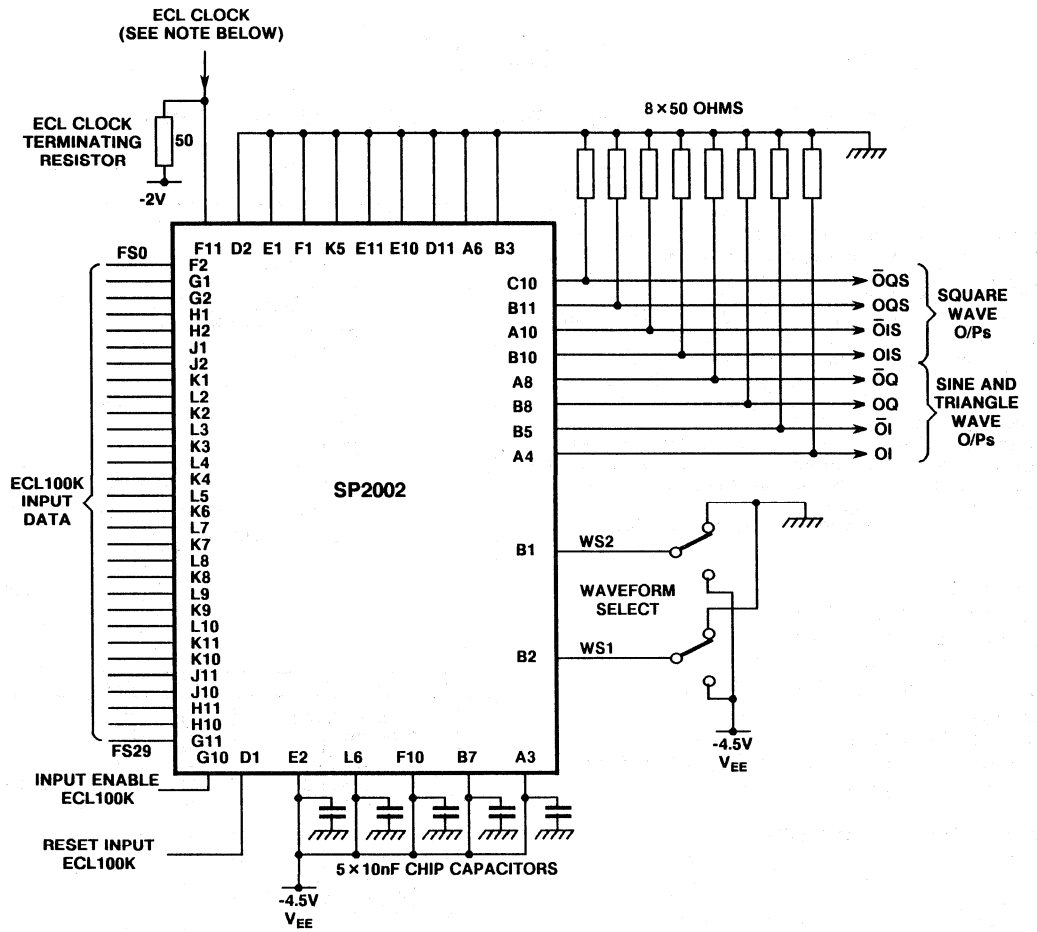


Fig. 4 SP2002 timing and waveform diagram.



NOTE

The clock input may be ECL level DC-coupled as shown above or a sinewave input of 1V peak-to-peak amplitude AC-coupled. When sinewave drive is used the input should be biased to -1.3V and the input cable terminated close to the IC with 50 ohms.

Minimum operating frequency with sinewave drive is 50MHz.

Use chip components mounted as close as possible to the IC pins.

Typical sinewave clock bias and termination circuit

Fig. 5 SP2002 typical application circuit

SP8852D

1.7GHz PARALLEL LOAD PROFESSIONAL SYNTHESISER

The SP8852D is one of a family of parallel load synthesisers containing all the elements apart from the loop amplifier to fabricate a PLL synthesis loop. Other parts in the series are the SP8854D which has hard wired reference counter programming and requires only a single 16 bit programming word, and the SP8855D which is fully programmable using hard wired links or switches.

The SP8852D is programmed using a 16 bit parallel data bus. Data can be stored in one of two internal buffers, selected by a single address bit on the input interface. In order to fully program the device, two 16 bit words are required, one to select the RF division ratio (A&M counters) and phase detector gain, and one to set the ten bit reference divider count, phase detector state and sense. Once the reference divide ratio has been set, frequency changes can be made by a single 16 bit data load entry to the RF divider chain.

FEATURES

- 1.7GHz Operating Frequency
- Single 5V Supply Operation
- Low Power Consumption <1.3W
- High Comparison Frequency 20MHz
- High Gain Phase Detector 1mA/rad
- Zero "Dead Band" Phase Detector
- Wide Range of RF and Reference Divide Ratios
- Programming by Dual Word Data Transfer

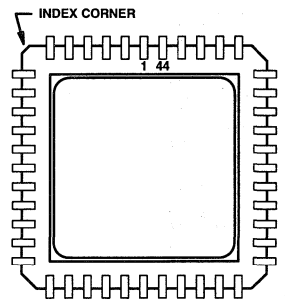
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	−0.3V to 6V
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +100°C
Prescaler & reference Input Voltage	2.5V p–p
Data Inputs	V_{CC} +0.3V
	V_{EE} −0.3V

ORDERING INFORMATION

SP8852D KG HCAR (non standard temperature range −55°C to +100°C standard product screening)

SP8852D IG HCAR (Industrial temperature range −40°C to +85°C standard product screening)



HC44

Pin	Description	Pin	Description
1	Input bus bit 10	23	NC
2	Input bus bit 9	24	F_{pd}*
3	Input bus bit 8	25	F_{ref}*
4	Input bus bit 7	26	+5V
5	Input bus bit 6	27	Ref. osc capacitor
6	Input bus bit 5	28	Ref in/XTAL
7	Input bus bit 4	29	NC
8	Input bus bit 3	30	NC
9	Input bus bit 2	31	NC
10	Input bus bit 1	32	NC
11	Input bus bit 0	33	NC
12	0V (prescaler)	34	NC
13	RF input	35	NC
14	RF input	36	NC
15	V_{CC} +5V (prescaler)	37	NC
16	V_{EE} 0V	38	Address input
17	Lock detect output	39	Strobe
18	C–lock detect	40	Input bus bit 15
19	R_{set}	41	Input bus bit 14
20	Charge pump output	42	Input bus bit 13
21	Charge pump ref.	43	Input bus bit 12
22	NC	44	Input bus bit 11

* F_{pd} and F_{ref} outputs are reversed by the phase detector sense bit, bit 12 in the programming word. The table above is correct when the sense bit is high.

Fig. 1 Pin connections – top view

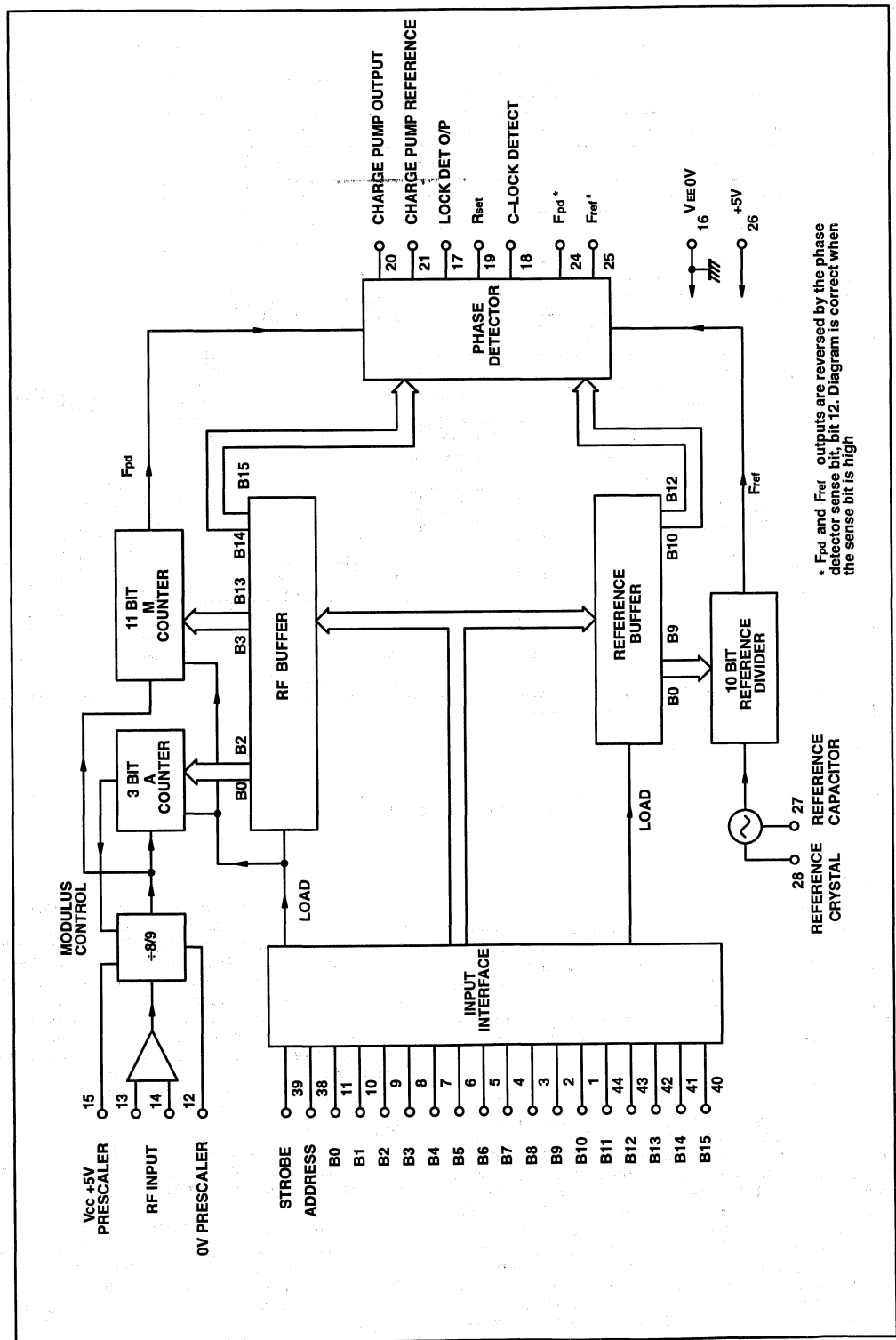


Fig. 2 SP8852D block diagram

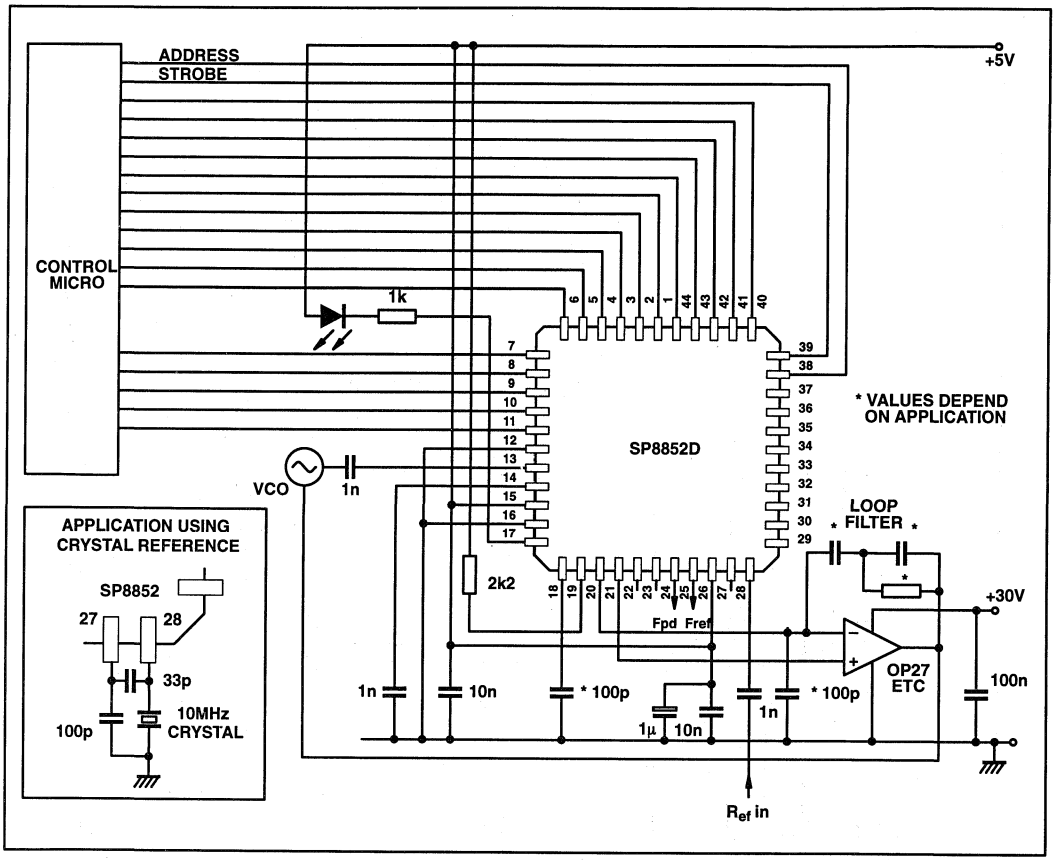


Fig. 3 Typical application diagram

DESCRIPTION

Prescaler and AM counter

The programmable divider chain is of A M counter construction and therefore contains a dual modulus front end prescaler, an A counter which controls the dual modulus ratio and an M counter which performs the bulk multi–modulus division. A programmable divider of this construction has a division ratio of MN+A and a minimum integer steppable division ratio of N(N–1), where N is the prescaler value.

Data entry and storage

Data is loaded from the 16 bit bus into one of the internal buffers by applying a positive pulse to the strobe input. The input bus can be driven from TTL or CMOS logic levels. When the strobe input is low, the inputs are isolated and the data can be changed without affecting the programmed state. The data is loaded into the RF buffer when the address input is high and into the reference buffer when low. When the strobe input is taken high, the A and M and reference counters are reset and the input data is applied to the internal storage register. When the strobe input is again taken low, the data on the input bus is stored in the selected register and the counters released. The strobe input is level triggered so that if the data is changed whilst the input is high, the final value before the strobe goes low will be stored.

In order to prevent disturbances on the VCO control voltage when frequency changes are made, the strobe input disables the charge pump outputs when high. During this period the VCO control voltage will be maintained by the loop filter components around the loop amplifier, but due to the combined effects of the amplifier input current and charge pump leakage a gradual change will occur. In order to reduce the change, the duration of the strobe pulse should be minimised. Selection of a loop amplifer with low input current will reduce the VCO voltage droop during the strobe pulse and result in minimum reference sidebands from the synthesiser.

Reference input

The reference source can be either driven from an external sine or square wave source of up to 100MHz or a crystal can be connected as shown in Fig. 3.

Phase Comparator and Charge pump

The SP8852D has a digital phase/frequency comparator driving a charge pump with programmable current output. The charge pump current level at the minimum gain setting is approximately equal to the current fed into the R_{set} input pin 19 and can be increased by programming the bus according to Table 1 by up to 4 times.

Bit 15	Bit 14	Current Multiplication Factor
0	0	1.0
0	1	1.5
1	0	2.5
1	1	4.0

Table 1

$$\text{Pin 19 current} = \frac{V_{cc} - 1.6V}{R_{set}}$$

$$\text{Phase detector gain} = \frac{I_{pin\ 19}(mA) \times \text{multiplication factor}}{2\pi}\ mA/\text{radian}$$

To allow for control direction changes introduced by the design of the PLL, bit 12 on the input bus address 0 can be programmed to reverse the sense of the phase detector by transposing the F_{pd} and F_{ref} connections. In order that any external phase detector will also be reversed by this programming bit, the F_{pd}/F_{ref} outputs are also interchanged by bit 12 as shown in Table 2.

Output for RF Phase Lag	
Sense Bit (Bit 12)	Pin 20
1	Current Source
0	Current Sink

Table 2

The F_{pd} and F_{ref} signals to the phase detector are available as ECL 10k levels on pin 24 and 25 and may be used to monitor the frequency input to the phase detector or used in conjunction with an external phase detector. These outputs may be programmed by bits 10 and 11 of word 0 according to table 3. State 3 where the outputs are disabled by the lock detect circuit is useful where the user wishes to use an external phase detector. The internal phase/frequency detector may be used to pull the loop into lock and an automatic switch over to the external phase detector made. When the F_{pd}/F_{ref} outputs are to be used at high frequencies, an external pull down resistor of minimum value 330Ω may be connected to ground to reduce the fall time of the output pulse.

Bit 11	Bit 10	Phase Detector State
0	0	Phase detector enable F_{pd}/F_{ref} outputs off
0	1	Phase detector enable F_{pd}/F_{ref} outputs on
1	0	Phase detector disable by lock detect F_{pd}/F_{ref} outputs on
1	1	Phase detector disabled F_{pd}/F_{ref} outputs on

Table 3

The charge pump connections to the loop amplifier consist of the charge pump output and the charge pump reference. The matching of the charge pump up and down currents will only be maintained if the charge pump output is held at a voltage equal to the charge pump reference using an operational amplifier to produce a virtual earth condition at pin 20. Because the operational amplifiers will have limited response time compared with the pulse frequency at the charge pump output, pin 20 will not remain at the same voltage as pin 21 without an additional capacitor to ground to decouple the high frequencies. The value of capacitor required will vary with comparison frequency and the bandwidth of the op amp but a value between 50pF and 5nF will normally be required.

The lock detect circuit can drive an LED to give visual indication of phase lock or provide an indication to the control system if a pull up resistor is used in place of the LED. A small capacitor connected from the C–lock detector pin to ground may be used to delay lock detect indication and remove glitches produced by momentary phase coincidence during lock up.

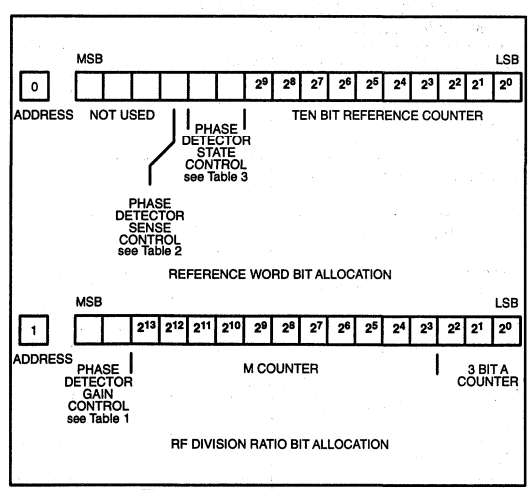


Fig. 4 Programming data format

ELECTRICAL CHARACTERISTICS

Guaranteed over the full temperature and supply voltage range (unless otherwise stated)
Temperature T_{amb} for KG parts –55°C and +100 °C
Temperature T_{amb} for IG parts –40°C and +85°C
Supply Voltage V_{CC} = 4.75V and 5.25V.

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	15, 26		180	240	mA	
RF input sensitivity	13, 14	–5.0		+7.0	dBm	100MHz to 1.7GHz See Fig. 8
RF division ratio	13,14,24	56		16383		
Reference division ratio	28, 25	1		1023		
Comparison frequency	28,24,25			50	MHz	
Reference input frequency	28	10		100	MHz	Reference division ratio ≥2 See Note 1
Reference input voltage	28	0	+6	+10	dBm	
F_{ref}/F_{pd} output voltage high	24, 25		–0.8		Vwrt V_{CC}	330Ω to 0V
F_{ref}/F_{pd} output voltage low	24, 25		–1.4		Vwrt V_{CC}	330Ω to 0V
Lock detect output voltage	17		300	500	mV	I_{OUT} = 3mA
Charge pump current at multiplication factor =1	19,20,21	±1.4	±1.5	±1.7	mA	$V_{pin\ 20} = V_{pin\ 21}$ $I_{pin\ 19}$ = 1.6mA
Charge pump current at multiplication factor =1.5	19,20,21	±2.0	±2.3	±2.5	mA	$V_{pin\ 20} = V_{pin\ 21}$ $I_{pin\ 19}$ = 1.6mA
Charge pump current at multiplication factor =2.5	19,20,21	±3.4	±3.8	±4.1	mA	$V_{pin\ 20} = V_{pin\ 21}$ $I_{pin\ 19}$ = 1.6mA
Charge pump current at multiplication factor =4.0	19,20,21	±5.4	±6.1	±6.5	mA	$V_{pin\ 20} = V_{pin\ 21}$ $I_{pin\ 19}$ = 1.6mA
Input bus high logic level	1 –11,38 39,40,44	3.5			V	
Input bus low logic level	1–11,38 39,40–44			1	V	
Input bus current source	1–11,38 39,40–44	200			µA	V_{IN} = 0V
Input bus current sink	1–11,38 39,40–44			10	µA	$V_{IN} = V_{CC}$
Up down current matching	20			±2	%	$V_{pin\ 20} = V_{pin\ 21}$ $I_{pin\ 19}$ = 1.6mA
Charge pump reference voltage	21			V_{CC} – 0.5	V	$I_{pin\ 19}$ = 1.6mA current multiplication factor 1
Charge pump reference voltage	21	V_{CC}–1.6			V	$I_{pin\ 19}$ = 1.6mA current multiplication factor 4
R_{set} current	19	0.5		2	mA	See Note 2
R_{set} Voltage	19		1.6		V	$I_{pin\ 19}$ = 1.6 mA
C–lock detect current	18		+10		µA	V_{pin}18=4.7V
Strobe pulse width		50			nS	Note 3
Data set up time		100			nS	Note 3

Notes: 1. lower reference frequencies may be used if slew rates are maintained.

2. Pin 19 current × multiplication factor must be less than 5mA if charage pump accuracy is to be maintained..

3. Guaranteed but not tested.

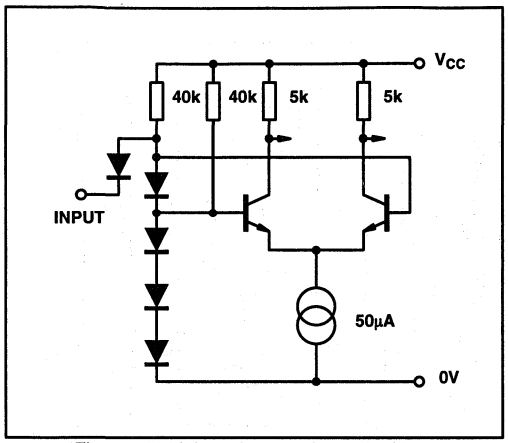


Fig. 5a 16 bit input bus, strobe and address

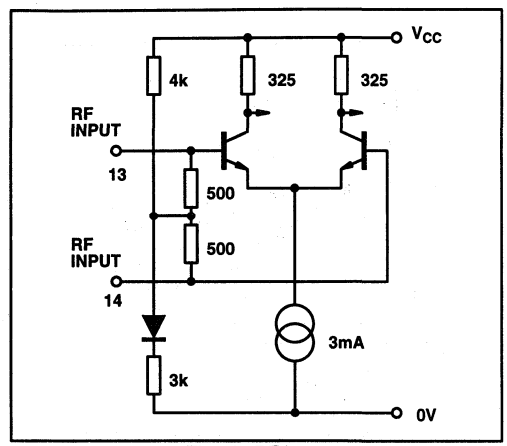


Fig. 5b RF inputs

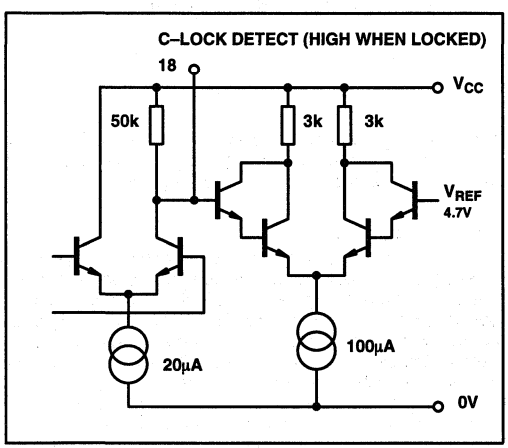


Fig. 5c Lock detect decouple

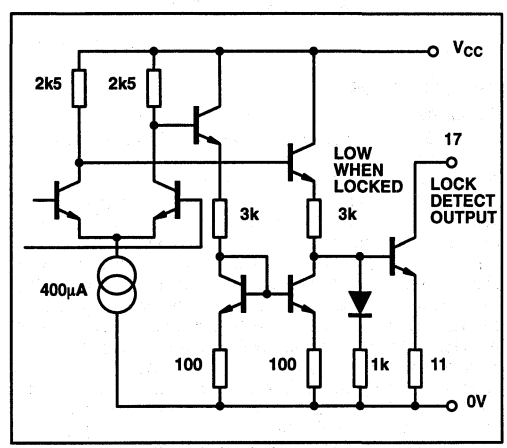


Fig. 5d Lock detect output

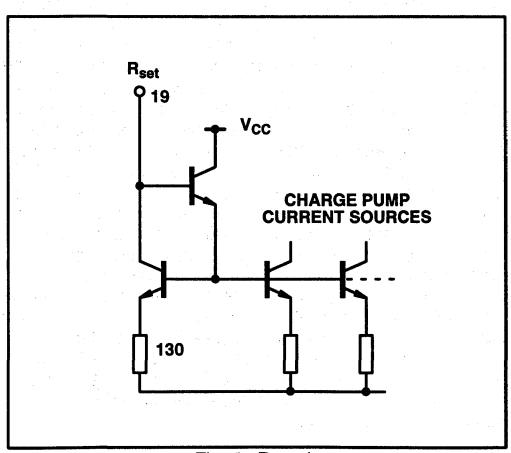


Fig. 5e R_{set} pin.

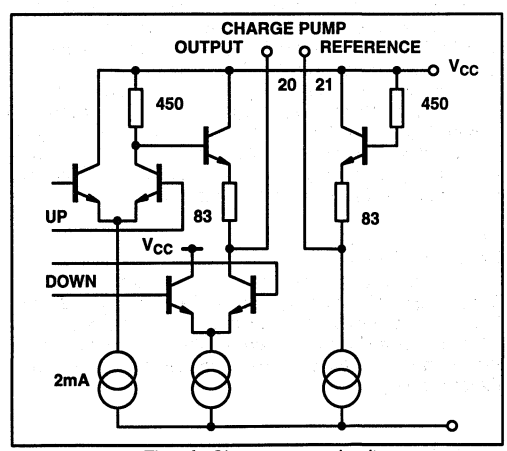


Fig. 5f Charge pump circuit

Fig. 5 Interface circuit diagrams

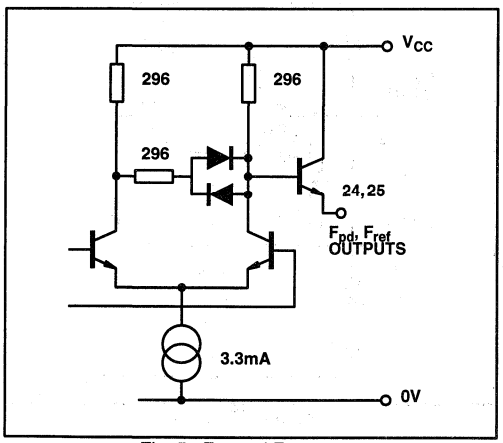


Fig. 5g F_{pd} and F_{ref} outputs

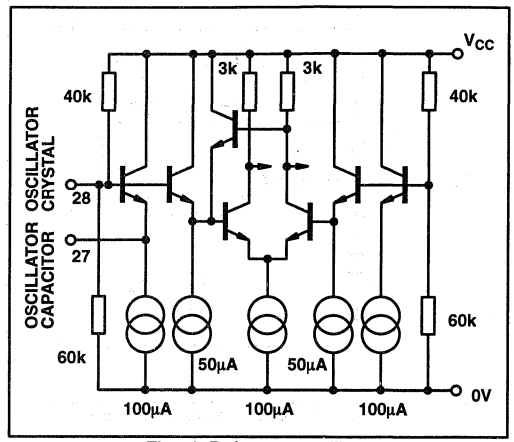


Fig. 5h Reference oscillator

Fig. 5 Interface circuit diagrams (cont)

APPLICATIONS

RF layout

The SP8852D can operate with input frequencies up to 1.7GHz but to obtain optimum performance, good RF layout practices should be used. A suitable layout technique is to use double sided printed circuit board with through plated holes. Wherever possible the top surface on which the SP8852D is mounted should be left as a continuous sheet of copper to form a low impedance earth plane. The ground pins 12 and 16 should be connected directly to the earth plane. Pins such as V_{CC} and the unused RF input should be decoupled with chip capacitors mounted as close to the device pin as possible with a direct connection to the earth plane, suitable values are 10nF for the power supplies and 1nF for the RF input pin. A larger decoupling capacitor mounted as close as possible to pin 26 should be used to prevent modulation of V_{CC} by the charge pump pulses. The R_{set} resistor should also be mounted close to the R_{set} pin to prevent noise pickup, and the capacitor connected from the charge pump output should be a chip component with short connections to the SP8852D.

When the reference is derived from a crystal connected to pins 27 and 28 as shown in Fig. 3 the oscillator components are best mounted close to the SP8852D.

All signals such as the programming inputs, RF in, reference in and the connections to the op–amp are best taken through the pc board adjacent to the SP8852D with through plated holes allowing connections to remote points without fragmenting the earth plane. The GEC Plessey evaluation board shown in Fig.6 uses this layout technique.

Programming bus

The input pins are designed to be compatible with TTL or CMOS logic with a switching threshold set at about 2.4V by three forward biased base emitter diodes. The inputs will be taken high by an internal pull up resistor if left open circuit but for best noise immunity it is better to connect unused inputs directly to V_{CC} or ground.

RF inputs

The prescaler has a differential input amplifer to improve input sensitivity. Generally the input drive will be single ended and the RF signal should be AC coupled to either of the inputs using a chip capacitor. The remaining input should be decoupled to ground, again using a chip capacitor. The inputs can be driven differentially but the input circuit should not provide a DC path between inputs or to ground.

Lock detect circuit

The lock detect circuit uses the up and down correction pulses from the phase detector to determine whether the loop is in or out of lock. When the loop is locked, both up and down pulses are very narrow compared to the reference frequency, but the pulse width in the out of lock condition continuously varies, depending on the phase difference between the outputs of the reference and RF counters. The logical AND of the up and down pulses is used to switch a 20mA current sink to pin 18 and a 50k resistor provides a load to V_{CC}. The circuit is shown in Fig. 5c. When lock is established, the narrow pulses from the phase detector ensure that the current source is off for the majority of the time and so pin 18 will be pulled high by the 50k resistor. A voltage comparator with a switching threshold at about 4.7V monitors the voltage at pin 18 and switches pin 17 low when pin 18 is more positive than the 4.7V threshold. When the loop is unlocked, the frequency difference at the counter outputs will produce a cyclic change in pulse width from the phase detector outputs with a frequency equal to the difference in frequency at the reference and RF counter outputs. A small capacitor connected to pin 18 prevents the indication of false phase lock conditions at pin 17 for momentary phase coincidence. Because of the variable width pulse nature of the signal at pin 18 the calculation of a suitable capacitor value is complex, but if an indication with a delay amounting to several times the expected lock up time is acceptable, the delay will be approximately equal to the time constant of the capacitor on pin 18 and the internal 50k resistor. If a faster indication is required, comparable with the loop lock up time, the capacitor will need to be 2–3 times smaller than the time constant calculation suggests. The time to respond to an out of lock condition is 2–3 times less than that required to indicate lock.

Charge pump circuit

The charge pump circuit converts the variable width up and down pulses from the phase detector into adjustable current pulses which can be directly connected to the loop amplifer.

The magnitude of the current and therefore the phase detector gain can be modified when new frequency data is entered to compensate for change in the VCO gain characteristic over its frequency band. The charge pump pulse current is determined by the current fed into pin 19 and is approximately equal to pin 19 current when the programmed multiplication ratio is one. The circuit diagram Fig. 5e shows the internal components on pin 19 which mirror the input current into the charge pump. The voltage at pin 19 will be approximately 1.6V above ground due to two V_{be} drops in the current mirror. This voltage will exhibit a negative temperature coefficient, causing the charge pump current to change with chip temperature by up to 10% over the full military temperature range if the current programming resistor is connected to V_{CC} as shown in the application diagram Fig. 3. In critical applications where this change in charge pump current would be too large the resistor to pin 19 could be increased in value and connected to a higher supply to reduce the effect of V_{be} variation on the current level. A suitable resistor connected to a 30V supply would reduce the variation in pin 19 current due to temperature to less than 1.5%. Alternatively a stable current source could be used to set pin 19 current.

The charge pump output on pin 20 will only produce symmetrical up and down currents if the voltage is equal to that on the voltage reference pin 21. In order to ensure that this voltage relationship is maintained, an operational amplifier must be used as shown in the typical application Fig. 3. Using this configuration pin 20 voltage will be forced to be equal to that on pin 21 since the operational amplifier differential input voltage will be no more than a few millivolts (the input offset voltage of the amplifier). When the synthesiser is first switched on or when a frequency outside the VCO range is programmed the amplifier output will limit, allowing pin 20 voltage to differ from that on pin 21. As soon as an achievable frequency value is programmed and the amplifer output starts to slew the correct voltage relationship between pin 20 and 21 will be restored. Because of the importance of voltage equality between the charge pump reference and output pins, a resistor should never be connected in series with the operational amplifier inverting input and pin 20 as is the case with a phase detector giving voltage outputs. Any current drawn from the charge pump reference pin should be limited to the few micro amps input current of a typical operational amplifier. A resistor between the charge pump reference and the non inverting input could be added to provide isolation but the value should not be so high that more than a few millivolts drop are produced by the amplifier input current.

When selecting a suitable amplifer for the loop filter, a number of parameters are important; input offset voltage in most designs is only a few milivolts and an offset of 5mV will produce a mismatch in the up and down currents of about 4% with the charge pump multiplication factor set at 1. The mismatch in up down currents caused by input offset voltage will be reduced in proportion to the charge pump multiplication factor in use. If the linearity of the phase detector about the normal phase locked operating point is critical, the input offset voltage of most amplifiers can be adjusted to near zero by means of a potentiometer.

The charge pump reference voltage on pin 21 is about 1.3V below the positive supply and will change with temperature and with the programmed charge pump multiplication factor. In many cases it is convenient to operate the amplifier with the negative power supply pin connected to 0V as this removes the need for an additional power supply. The amplifier selected must have a common mode range to within 3.4V (minimum charge pump reference voltage) of the negative supply pin to operate correctly without a negative supply. Most popular amplifiers can be operated from a 30V positive supply to give a wide VCO voltage drive range and have adequate common mode range to operate with inputs at +3.4V with respect to the negative supply. Input bias and offset current levels to most operational amplifiers are unlikely to be high enough to significantly affect the accuracy of the charge pump circuit currents but the bias current can be important in reducing reference side bands and local oscillator drift during frequency changes. When the loop is locked, the charge pump produces only very narrow pulses of sufficient width to make up for any charge lost from the loop filter components during the reference cycle. The charge lost will be due to leakage from the charge pump output pin and to the amplifier input bias current, the latter usually being more significant. The result of the lost charge is a sawtooth ripple on the VCO control line which frequency modulates the phase locked oscillator at the reference frequency and its harmonics. A similar effect will occur whenever the strobe input is taken high during a programming sequence. In this case the charge pump is disabled when the strobe input is high and any leakage current will cause the oscillator to drift off frequency. To reduce this effect, the duration of the strobe pulse should be minimised.

The necessity to maintain the charge pump output voltage at the same voltage as the reference pin has already been mentioned. This is important because the design of the positive current source has no voltage compliance and any departure from the reference voltage will introduce an error in the positive current source. The operational amplifier will maintain the DC charge pump voltage very close to the reference but the current from the charge pump is a series of pulses at the reference frequency. When the loop is locked the output pulses are very short in duration, the only current necessary being that required to restore and charge lost during the reference period. The virtual earth mechanism which maintains the charge pump output at the reference voltage depends on the amplifier having significant gain, but the narrow pulses from the charge pump are so short that the amplifier output will be unable to respond, allowing the input voltage to change and the pulse magnitude to be effectively reduced, introducing a non linearity in the phase detector characteristic at the phase locked point.

The capacitor shown connected from the charge pump output pin to ground on the typical application diagram Fig. 3 is intended to decouple the output at high frequencies, preventing voltage changes at the amplifier input which can not be corrected by the feedback response. The capacitor should be a high frequency type mounted close to the charge pump pin with short connection to the earth plane as the frequency content of the charge pump pulses extends to very high frequencies. A suitable value for this component is very difficult to calculate as its value depends on many factors including the bandwidth of the amplifier used in the loop filter and how critical the application is in terms of phase detector linearity. A value between 50nF and 5nF will suit most applications and the size of capacitor can be increased well beyond that necessary to restore linearity of the phase detector without ill effect. Many less critical applications will operate satisfactorily without this capacitor.

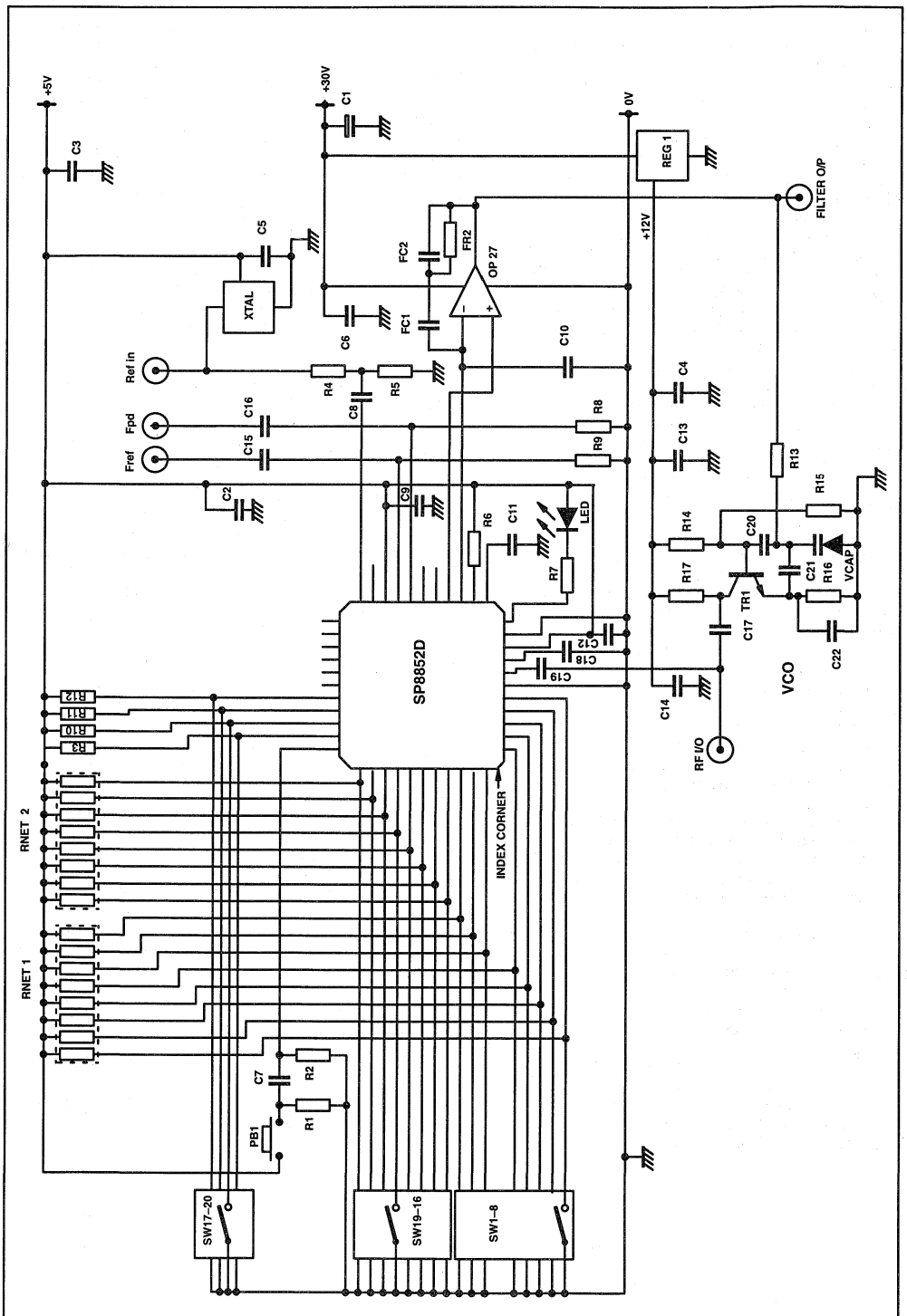


Fig. 6 Application board schematic

F_{pd} and F_{ref} outputs

These outputs provide access to the outputs from the RF and reference dividers and are provided for monitoring purposes during product development or test, and for connection of an external phase detector if required. The output circuit is of ECL type, the circuit diagram being shown in Fig. 5g. The outputs can be enabled or disabled under software control by the address 0 control word but are best left in the disabled state when not required as the fast edge speeds on the output can increase the level of reference sidebands on the synthesised oscillator.

The emitter follower outputs have no internal down resistor to save current and if the outputs are required an external pull down resistor should be fitted.The value should be kept as high as possible to reduce supply current, about 2.2k being suitable for monitoring with a high impedance oscilloscope probe or for driving an AC coupled 50ohm load. A minimum value for the pull down resistor is 330ohms. When the F_{pd} and F_{ref} outputs are disabled the output level will be at the logic low level of about 3.5V so that the additional supply current due to the load resistors will be present even when the outputs are disabled.

Reference input

The reference input circuit functions as an input amplifier or crystal oscillator. When an external reference signal is used this is simply AC coupled to pin 28, the base of the input emitter follower. When a low phase noise synthesiser is required the reference signal is critical since any noise present here will be multiplied by the loop. To obtain the lowest possible phase noise from the SP8852D it is best to use the highest possible reference input frequency and to divide this down internally to obtain the required frequency at the phase detector. The amplitude of the reference input is also important, and a level close to the maximum will give the lowest noise. When the use of a low reference input frequency say 4–10MHz is essential some advantage may be gained by using a limiting amplifier such as a CMOS gate to square up the reference input.

In cases where a suitable reference signal is not available, it may be more convenient to use the input buffer as a crystal oscillator in this case the emitter follower input transistor is connected as a colpitts oscillator with the crystal connected from the base to ground and with the feedback necessary for oscillation provided by a capacitor tap at the emitter. The arrangement is shown inset in Fig. 3

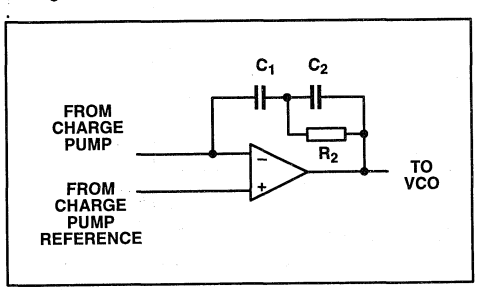


Fig. 7 Third order loop filter circuit diagram

Loop Filter Design

Generally the third order filter configuration shown in Fig.6 gives better results than the more commonly used second order because the reference sidebands are reduced. Three equations are required to determine values for the three constants where;

$$\tau_1 = C_1$$
$$\tau_2 = R_2 (C_1 + C_2)$$
$$\tau_3 = C_2 R_2$$

The equations are;

1 $$\tau_1 = \frac{K_\phi K_0}{N\omega_n^2}\left[\frac{1+\omega_n^2\tau_2^2}{1+\omega_n^2\tau_3^2}\right]^{1/2}$$

2 $$\tau_2 = \frac{1}{\omega_n^2\tau_3}$$

3 $$\tau_3 = \frac{-\tan\Phi_0 + \frac{1}{\cos\Phi_0}}{\omega_n}$$

Where;

- K_ϕ is the phase detector gain factor in mA/radian
- K_0 is the VCO gain factor in radian/second/Volt
- N is the total division ratio from VCO to reference frequency
- ω_n is the natural loop bandwidth
- ϕ_0 is the phase margin normally set to 45°

Since the phase detector is linear over a range of 2π radian, K_ϕ can be calculated from

K_ϕ = Phase comparator current setting / 2π mA/radian

These values can now be substituted in equation 1 to obtain a value for C_1 and equation 2 and 3 used to determine values for C_2 and R_2

EXAMPLE

Calculate values for a loop with the following parameters

Frequency to be synthesised:	1000MHz
Reference frequency	10MHz
Division ratio	1000MHz/10MHz = 100
ω_n natural loop frequency	100kHz
K_0 VCO gain factor	2π x 10MHz/Volt
Φ_0 phase margin	45°
Phase comparator current	6.3mA

The phase detector gain factor K_ϕ
= 6.3mA/2π = 1mA/radian

From equation 3:

$$\tau_3 = \frac{-\tan 45° + \frac{1}{\cos 45°}}{100\text{kHz} \times 2\pi} = \frac{0.4142}{628319}$$

$$\tau_3 = 659 \times 10^{-9}$$

From equation 2:

$$\tau_2 = \frac{1}{(100\text{kHz} \times 2\pi)^2 \times 659 \times 10^{-9}}$$

$$\tau_2 = 3.844 \times 10^{-6}$$

Using these values in equation 1:

$$\tau_1 = \frac{1 \times 10^{-3} \times 2\pi \times 10\text{MHz/V}}{100 \times (2\pi \times 100\text{kHz})^2}\ [\text{A}]^{1/2}$$

Where A is :

$$\frac{1 + \omega_n^2 \tau_2^2}{1 + \omega_n^2 \tau_3^2} = \frac{1 + (2\pi \times 100\text{kHz})^2 \times (3.844 \times 10^{-6})^2}{1 + (2\pi \times 100\text{kHz})^2 \times (659 \times 10^{-9})^2}$$

$$\tau_1 = \frac{62832}{39.48 \times 10^{12}} \left[\frac{6.833}{1.1714}\right]^{\frac{1}{2}}$$

$$\tau_1 = 1.59 \times 10^{-9} \times 2.415$$

$$\tau_1 = 3.84 \times 10^{-9}$$

Now $\tau_1 = C_1 \therefore C_1 = 3.84\text{nF}$

$\tau_2 = R_2 (C_1 + C_2)$

$\tau_3 = C_2 R_2$

Substituting for C_2

$$\tau_2 = R_2\left[C_1 + \frac{\tau_3}{R_2}\right] \quad \therefore \tau_2 = R_2 C_1 + \tau_3$$

$$\therefore R_2 = \frac{\tau_2 - \tau_3}{C_1} = \frac{3.844 \times 10^{-6} - 659 \times 10^{-9}}{9.61 \times 10^{-9}}$$

$R_2 = 829.4\Omega$

$$\tau_3 = C_2 R_2 \therefore C_2 = \frac{\tau_3}{R_2} = \frac{659 \times 10^{-9}}{829.4}$$

$C_2 = 0.794\text{nF}$

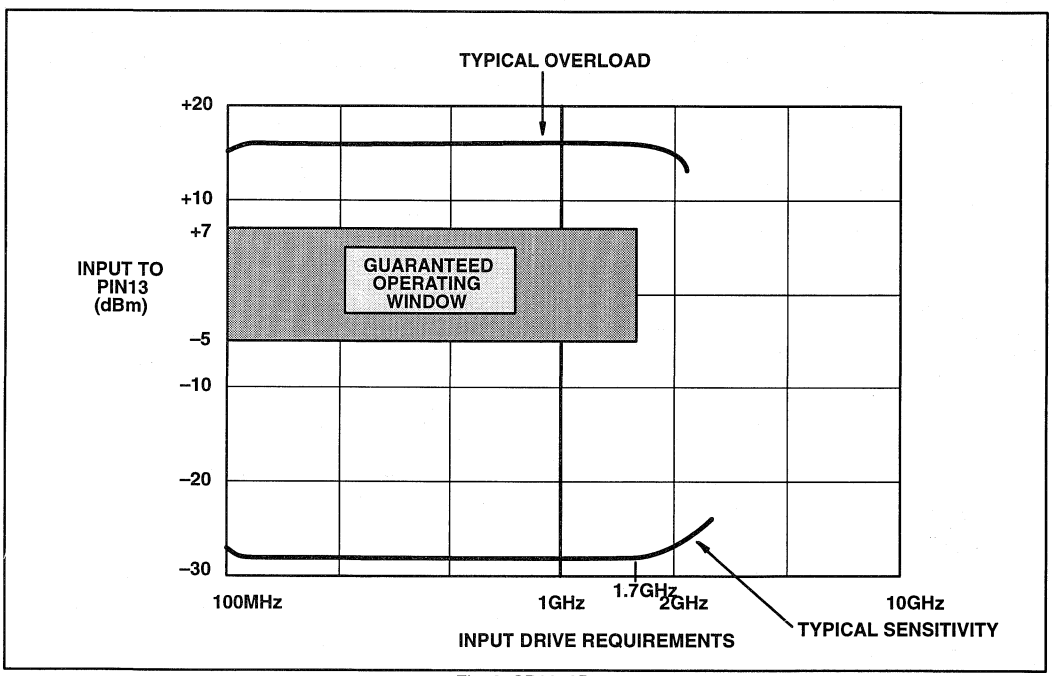
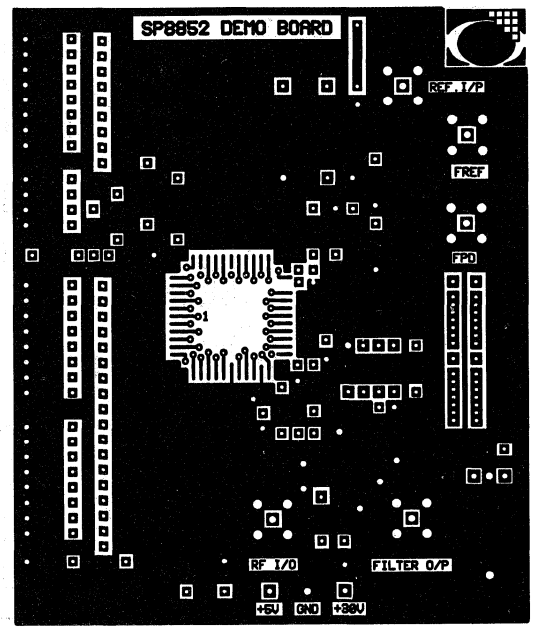


Fig. 8 SP8852D

TRACK LAYOUT (topside)



TRACK LAYOUT (underside)

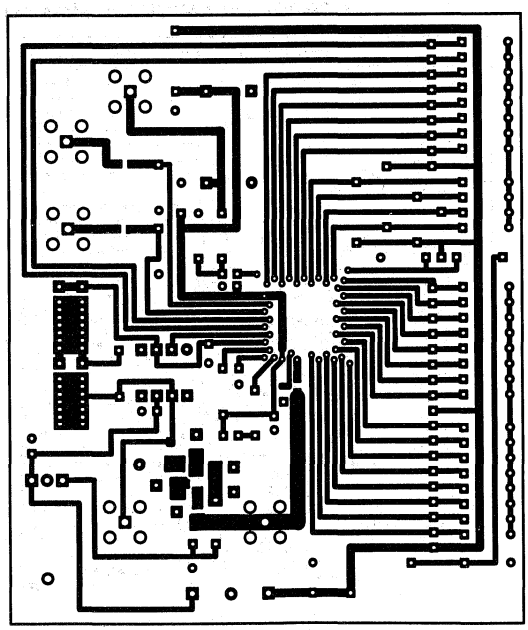


Fig. 9 P.C.B. layout

COMPONENT LAYOUT (topside)

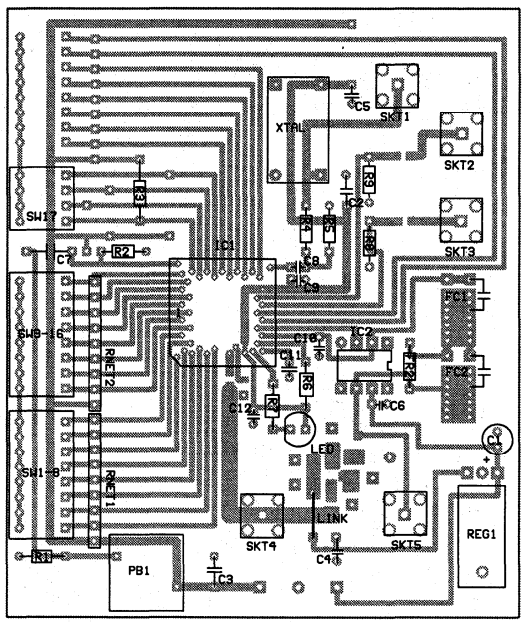


Fig.10 component layout.

COMPONENT LAYOUT (underside)

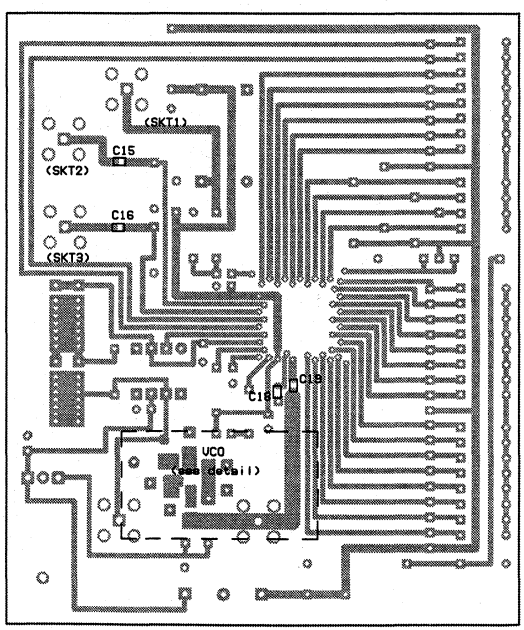


Fig.11 component layout.

Component List.

C1	47µF	electrolytic
C2	10µF	tant
C3	1µF	tant
C4	1µF	tant
C5	100nF	ceramic
C6	100nF	ceramic
C7	22nF	polyester
C8	10nF	ceramic
C9	10nF	ceramic
C10	10nF	ceramic
C11	100pF	ceramic
C12	10nF	ceramic
C13	10nF	chip
C14	10nF	chip
C15	10nF	chip
C16	10nF	chip
C17	1nF	chip
C18	1nF	chip
C19	1nF	chip
C20	1.5pF	chip
C21	1.5pF	chip
C22	1.5pF	chip

Note C13 to C22 are mounted on the underside of the board.

R1	100K	
R2	2K7	
R3	10K	
R4	2K2	
R5	2K2	
R6	2K2	
R7	1K	
R8	1K	
R9	1K	
R10	N/U	
R11	N/U	
R12	N/U	
R13	47K	chip
R14	10K	chip
R15	1K8	chip
R16	180R	chip
R17	50R	chip
RNET1	10K	
RNET2	10K	

Note R13 to R17 are mounted on the underside of the board

IC1	SP8852D
IC2	OP–27G
REG1	L7812CP
TR1	AT–41486
VARICAP	BB405B
LED	5mm round

XTAL	40MHz crystal (optional)
SW1	to SW17 SPDT d.i.l toggle switches
PB1	pcb mount push button
SKT1	to SKT5 SMA pcb mount sockets
FC1, FC2 & FR2	are application dependant.

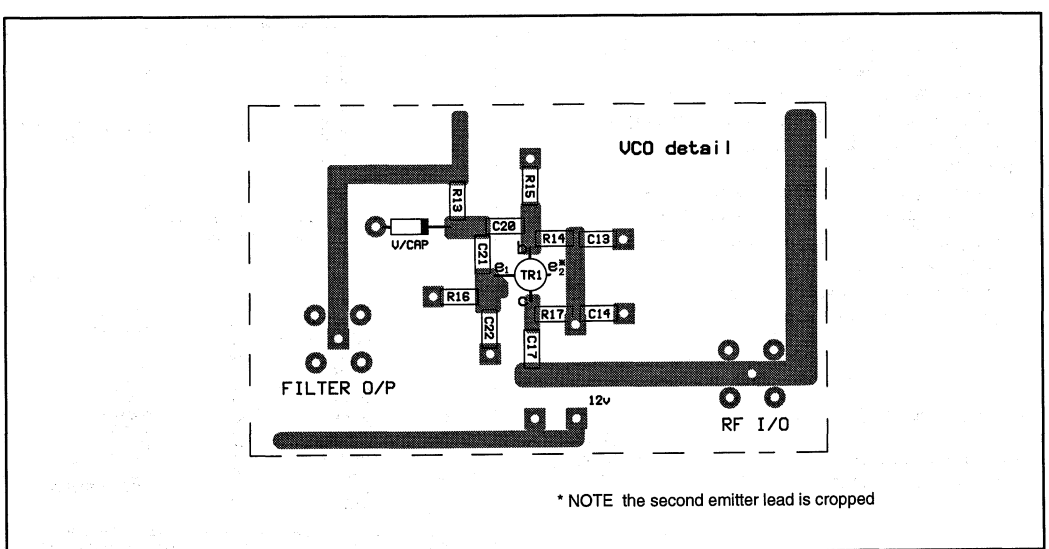


Fig. 12 VCO detail

SP8853A/B

1.3 / 1.5GHz PROFESSIONAL SYNTHESISER

(Supersedes the Edition in May 1991 Professional I.C Handbook)

The SP8853 is a low power single chip synthesiser intended for professional radio applications, and contains all the elements (apart from the loop amplifier) to fabricate a PLL frequency synthesis loop.

The device is serially programmable by a three wire data highway and contains three independent buffers to store one reference divider word and two local oscillator divider words. A digital comparator, with two charge pump, programmable in phase and gain are provided to improve lock up performance. the preset tandem operation of the charge pumps can be overwritten or the comparison frequencies switched to output ports under control of the divider word. the dual modulus ratio and so operating range is also programmable through the same word.

A power down mode is incorporated as a battery economy feature.

The part is specified to 1.5GHz at +85°C and to 1.3GHz at +125°C in the DG package. In the HC package the part is specified to 1.3GHz at +85°C and +125°C.

FEATURES

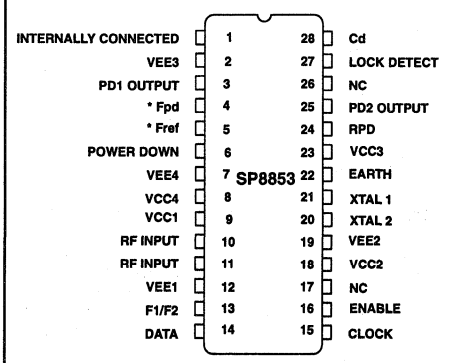
- Improved Digital Phase Detector to Eliminate "Dead Band" Effects
- Low Operating Power, Typically 175mW
- 1.5GHz Operating Frequency (DG package)
- Complete Phase Locked Loop
- High Input Sensitivity
- Programmed through Three Wire Data Bus
- Wide Range of Reference Division Ratios
- Local Storage for Two Frequency Words giving Rapid Frequency Toggling
- Programmable Phase Detector Gain
- Power Down Mode

ABSOLUTE MAXIMUM RATINGS

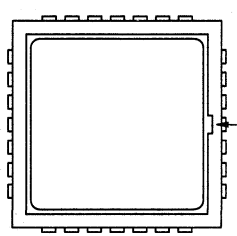
Supply voltage	–0.3V to 7V
Storage temperature	–55°C to +150°C
Prescaler input voltage	2.5V p–p

ORDERING INFORMATION

SP8853/A/DG Military temperature range
SP8853/B/DG Industrial temperature range
SP8853/AC/DG Mil std 883
SP8853/A/HC Military temperature range
SP8853/B/HC Industrial temperature range
SP8853/AC/HC Mil std 883



DG28



HC28

1	IC	15	CLOCK
2	VEE3	16	ENABLE
3	PD1 OUTPUT	17	NC
4	* Fpd	18	VCC2
5	* Fref	19	VEE2
6	POWER DOWN	20	XTAL 2
7	VEE4	21	XTAL 1
8	VCC4	22	EARTH
9	VCC1	23	VCC3
10	RF INPUT	24	RPD
11	RF INPT	25	PD2 OUTPUT
12	VEE1	26	NC
13	F1/F2	27	LOCK DETECT
14	DATA	28	Cd

* Fpd and Fref outputs are reversed by the phase detector sense bit in the programming word. Diagram above is correct when sense bit is low.

VCC1, VEE1 – Preamp and Prescaler
VCC2, VEE2 – Oscillator Supplies
VCC3, VEE3 – Charge Pump 2 Supplies
VCC4, VEE4 – ECL Supplies.

Fig. 1 Pin connections – top view

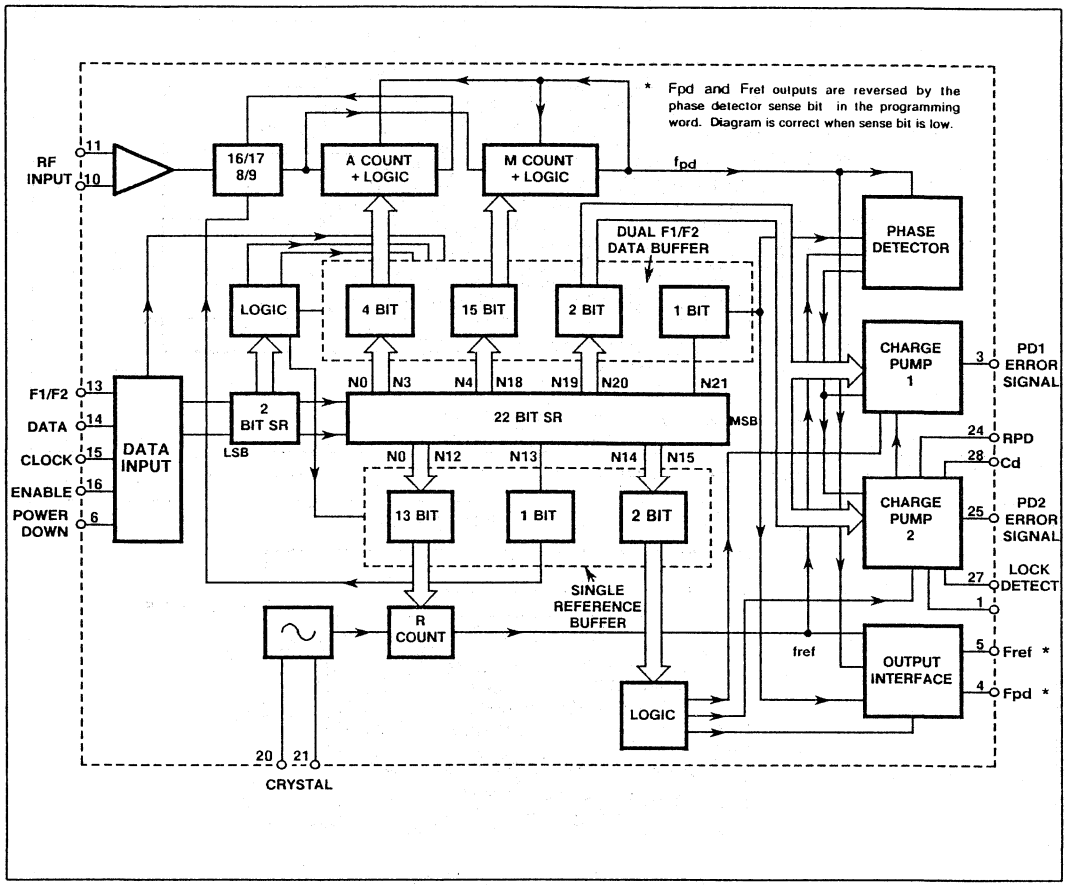


Fig. 2 SP8853 block diagram

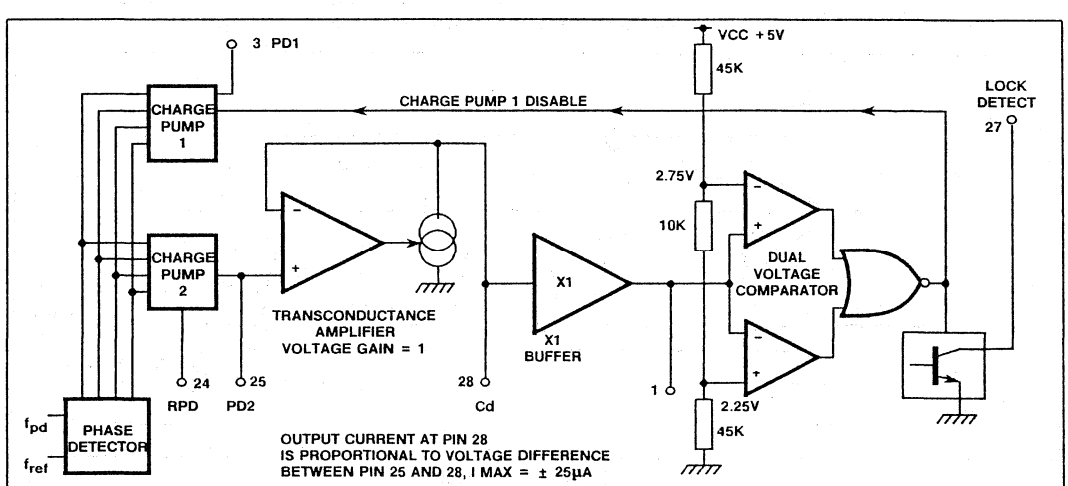


Fig. 3 Detailed Block Diagram of Lock Detect Circuit

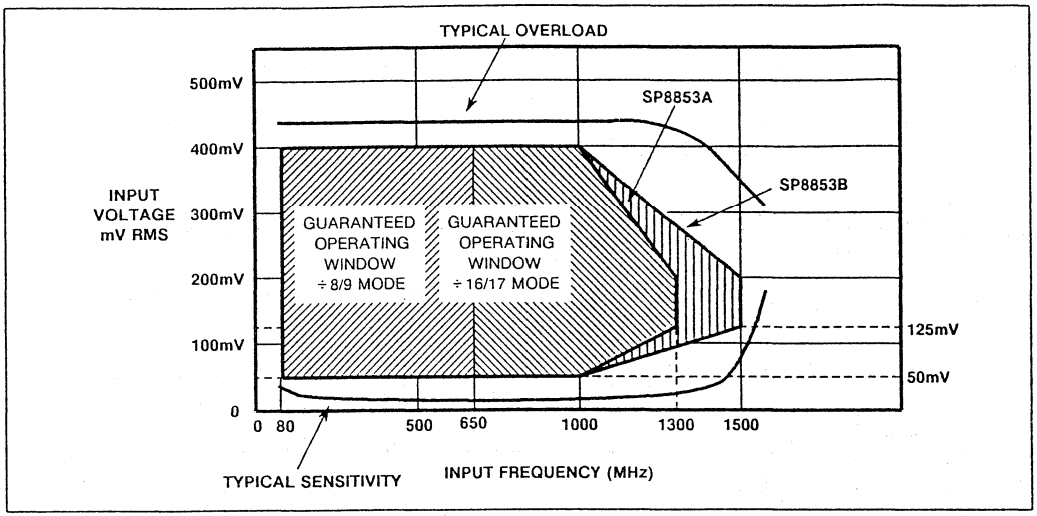


Fig. 4a Typical input characteristics and input drive requirements (DG package)

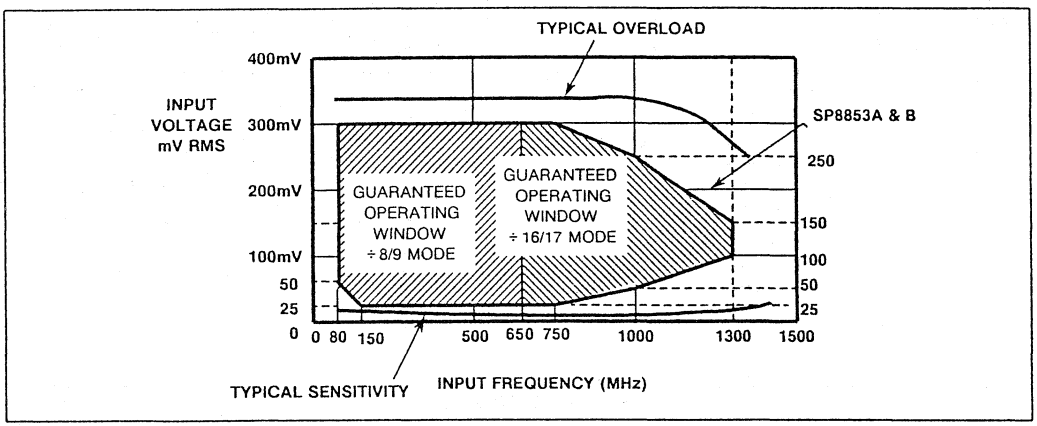


Fig. 4b Typical input characteristics and input drive requirements (HC package)

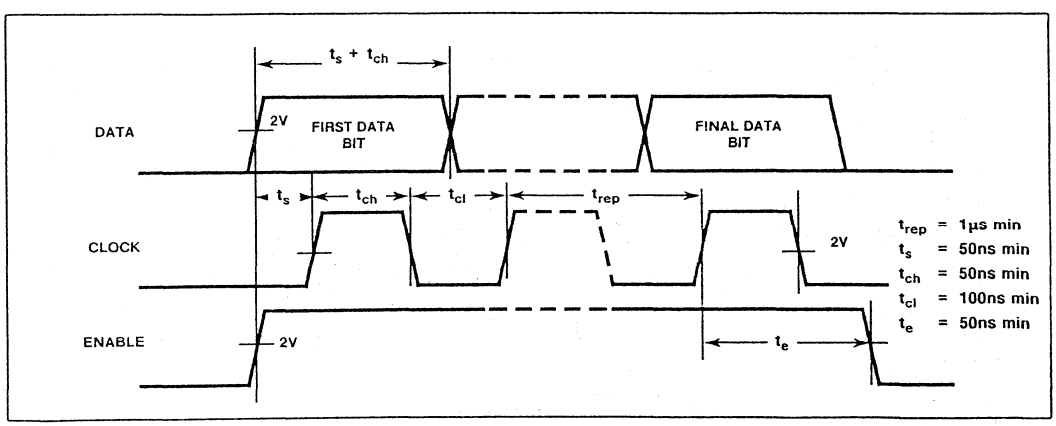


Fig. 5 Data and clock timing requirements

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated)

Supply Voltage V_{CC} +4.75 to + 5.25V

Temperature A Grade T_{amb} = -55°C to + 125°C

B Grade T_{amb} = -40°C to +85°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ	Max.		
Supply Current	8,9					
	18,23		33	40	mA	
Supply Current in Power Down Mode	8		4.5	7.5	mA	
Input Sensitivity	10,11					See Figure 4a and b
Input Overload	10,11					See Figure 4a and b
RF Input Division Ratio	10,11,4	256		524287		With 16/17 selected
		56		262143		With 8/9 selected
Comparison Frequency	4,5			5	MHz	
Reference Oscillator Input Frequency	20,21	4		20	MHz	
External Reference Input Voltage	20	10		500	mVrms	
Reference Division Ratio	20,5	1		8191		
Data Clock Repetition Rate t_{rep}	15			1	µs	See Figure 5
Minimum Set up Time t_s	14,15	50			ns	See Figure 5
Data Input High	14	0.6Vcc		Vcc	V	
Low	14	Vee		0.3Vcc	V	
Clock Input High	15	0.6Vcc		Vcc	V	
Low	15	Vee		0.3Vcc	V	
Data Enable High	16	0.6Vcc		Vcc	V	
Low	16	Vee		0.3Vcc	V	
F1/F2 Input High	13	0.6Vcc		Vcc	V	F1 buffer selected
Low	13	Vee		0.3Vcc	V	F2 buffer selected
Power Down Input High	6	0.6Vcc		0.9Vcc	V	
Low	6	Vee		0.3Vcc	V	
F1/F2 Input Current	13			5	µA	V Pin 13 = 5.0V
Power Down Input Current	6			5	µA	v Pin 6 = 4.5V
RPD External Resistance	24	68		330	KOhms	
Lock Detect Output Voltage "in lock"	27			1	V	I pin 27 = 1mA
Lock Detect Switching Voltage High	25	2.7			V	Vcc = 5V
Low	25			2.3	V	Vcc = 5V
Fpd and Fref Output Voltage Swing			0.9		V	Vcc = 5V. External pull down may be required

DESCRIPTION

Prescaler and A M counter

The programmable divider chain is of A M counter construction and therefore contains a dual modulus front end prescaler, an A counter which controls the dual modulus ratio and an M counter which performs the bulk multi-modulus division. A programmable divider of this construction has a division ratio of MN + A and a minimum integer steppable division ratio of N(N-1).

In the SP8853 the dual modulus front end prescaler is a dual N ratio device capable of being statically switched between 16/17 and 8/9 ratios. The controlling A counter is of four bit design enabling a maximum count sequence of 15, (2^4-1) which begins with the start of the M counter sequence and stops when it has counted by the preloaded number of cycles. Whilst the A counter is counting the dual modulus prescaler is held in the N + 1 mode, then relaxes back to the N mode at the completion of the sequence. The M counter is a 15-bit asynchronous divider which counts with a ratio set by a control word. In both A and M counters the controlling data from the F1/F2 buffer is loaded in sequence with every M count cycle. The N ratio of the dual modulus prescaler is selected by a one bit word in the reference divider buffer and, when a ratio of 8/9 is selected the A counter requires only three programming bits, having an impact on the frequency bit allocation as described in the data entry section.

Reference source and divider

The reference source in the SP8853 is obtained from an on board oscillator, frequency controlled by an external crystal. The oscillator can also function as a buffer amplifier allowing the use of an external reference source. In this mode the source is simply AC coupled into the oscillator transistor base on pin 20.

The oscillator output is coupled to a programmable reference divider whose output is the reference for the phase detector. The reference divider is a fully programmable 13-bit asynchronous design and can be set to any division ratio between 1 and 8191. The actual division ratio is controlled by a data word stored in the internal reference buffer.

Phase comparator

The SP8853 is provided with a digital phase comparator feeding two charge pump circuits. Charge pump 1 has preset currents programmable as shown in table 1. Charge pump 2 has a current level set by an external resistor: the current is multiplied by a factor determined by the F1 or F2 word (see table 1).

A lock detect circuit is connected to the output of charge pump 2. When the voltage level at pin 25 is between approximately 2.25 and 2.75 volts, pin 27 will be low and charge pump 1 disabled depending on the PD1 and PD2 programming bits as shown in table 4.

The output signals from the reference and M counters are available on pins 4 and 5 when programmed by the reference programming word: the various options are shown in table 4. An external phase detector may be connected to pins 4 and 5 and may be used independently or in conjunction with the on chip detector.

To allow for control direction changes introduced by the design of the control loop, a programming bit in the F1/F2 programming word interchanges the inputs to the on chip phase detector and reverses the functions on pins 4 and 5.

F1 OR F2 WORD G2	G1	CHARGE PUMP 1 CURRENT	CHARGE PUMP 2 MULTIPLIER
0	0	50µA	1
1	0	75µA	1.5
0	1	125µA	2.5
1	1	200µA	4

Table 1 Charge pump currents

Note: ***Charge pump 2*** *is pin 24 current × multiplication factor.* $I_{pin\ 24} = \frac{VCC-1.5V}{RPD}$

Data entry and storage

The data section of the SP8853 consists of a data input interface, an internal data shift register and three internal data buffers.

Data is entered to the data input interface by a three wire data highway with data, clock and chip enable inputs. The input interface then routes this data to a 24-bit shift register with bus connections to three data buffers. Data entered via the serial bus is transfered to the appropriate data buffer on the negative transition of the chip enable input according to the two final data bits as shown in Table 3. The MSB of the data is entered first.

The dual F1/F2 buffer can receive two 22-bit words and controls the programmable divider A and M counters using 19-bits, the phase detector gain with two bits and the phase detector sense with one bit. A fourth input from the synthesiser control system selects the active buffer.

OUTPUT FOR RF PHASE LAG	
Sense Bit	Pins 3 and 25
0	Current source
1	Current sink

Table 2

The third buffer contains only 16 bits, 13 being used to set the reference counter division ratio, and 2 to control the phase comparator enable logic. The remaining bit sets the dual modulus prescaler N ratio.

2 Bit S.R. Contents	Buffer Loaded
00	F1
10	F2
01	Active A *
11	Reference

Table 3

** Transfer of A counter bits into buffer controlling the programmable counter*

The data words may be entered in any individual multiple sequence and the shift register can be updated whilst the data buffers retain control of the synthesiser with the previously loaded data. This enables four unique data words to be stored in the device, with three in the data buffers and a fourth in the shift register, whilst the chip is enabled. F1 word may also be updated whilst F2 is controlling the programmable divider and vice versa.

The dual F1/F2 buffer enables the device to be toggled between two frequencies using the F1/F2 select input at a rate determined by the comparasion frequency

and also enables random frequency hopping at a rate determined by a byte load period, since the loop can be locked to F1 whilst F2 is updated by entering new data via the shift register. The F1/F2 input is high to select F1.

An F1 or F2 update cycle will consist of a byte containing 24 bits, whereas the reference byte will contain 18 bits. The device requires 3 bytes, each with a chip select sequence, totalling 66 bits to fully program.

When the dual modulus counter (A count) is set to ÷8/9, the data required to set the counter is reduced by one bit, leaving an unused bit in the 22-bit F1/F2 buffer. this bit must always be set to zero when ÷8/9 mode is required. Various programming sequences are shown in Fig. 7

The data entry and storage registers are always powered up, making it possible to enter data when the device is in the powered down state.

PD2	PD1	
0	0	Fref and Fpd outputs off, charge pump 1 and 2 on
0	1	Fref and Fpd outputs on, charge pump 1 off. Charge pump 2 on
1	0	Fref and Fpd outputs off, charge pump 1 disabled by lock detect. Charge pump 2 on
1	1	Fref and Fpd outputs on, charge pump 1 disabled by lock detect. Charge pump 2 on

Table 4

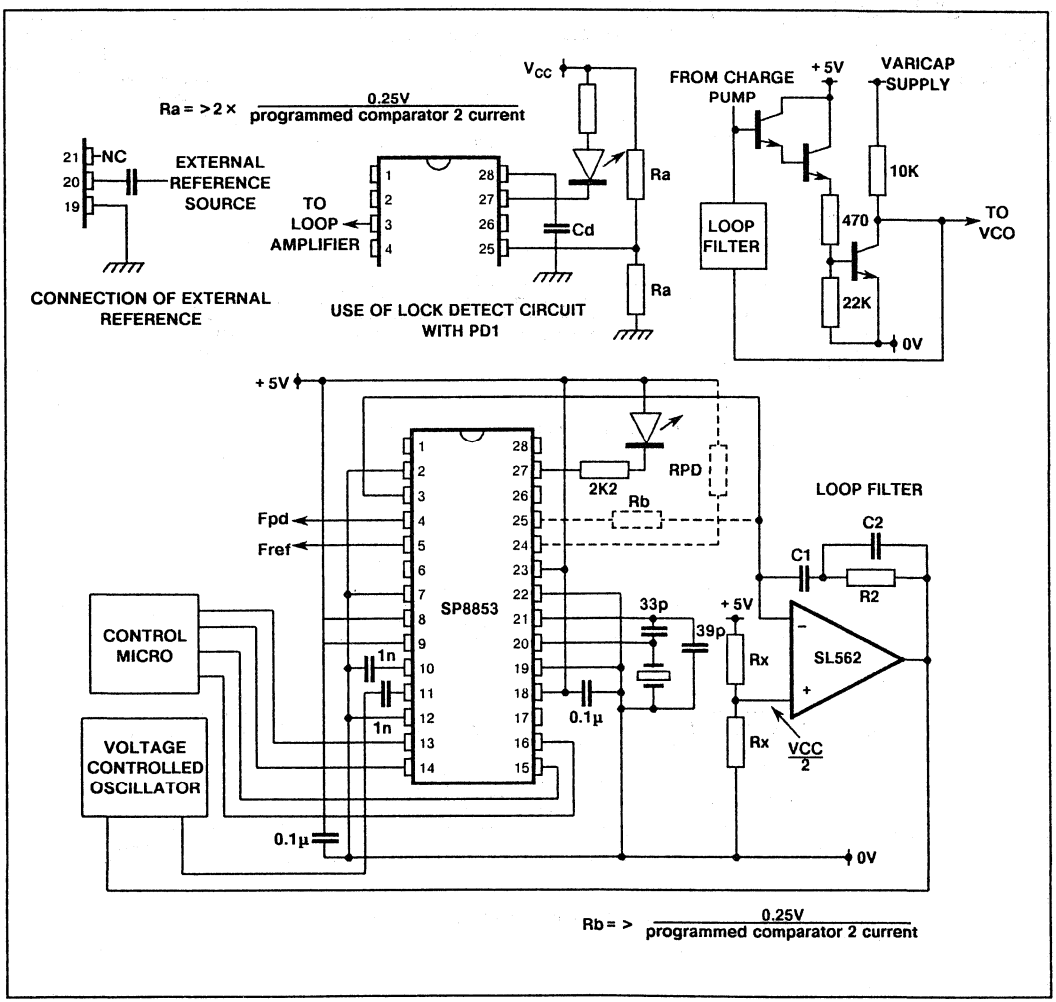


Fig. 6 Typical application diagram

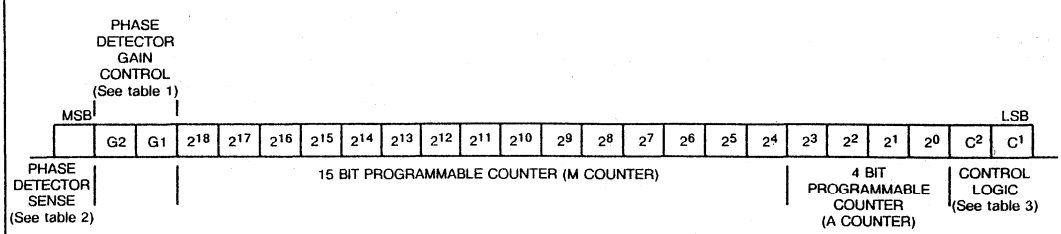


FIG.7(a) F1 or F2 word, bit allocation with 16/17 selected

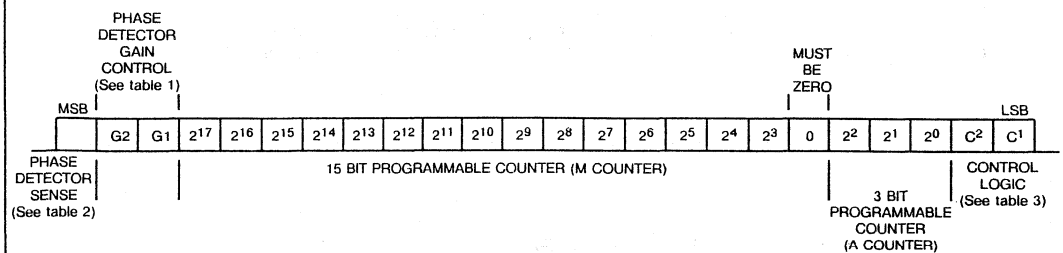


FIG.7(b) F1 or F2 word, bit allocation with 8/9 selected

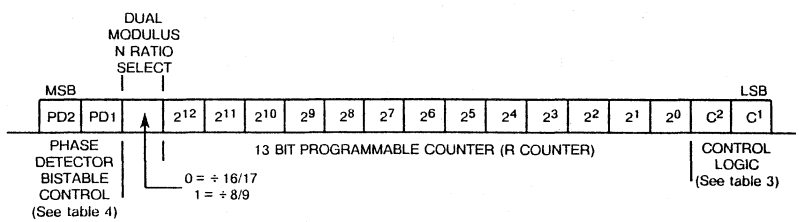


FIG.7(c) reference word bit allocation

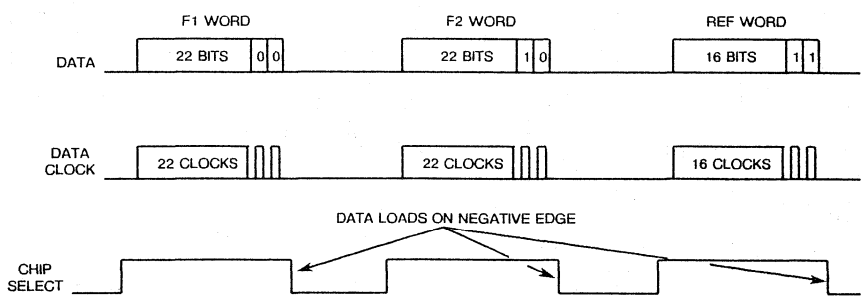


Fig.7(d) Typical data load sequence

Fig. 7 Data format diagrams

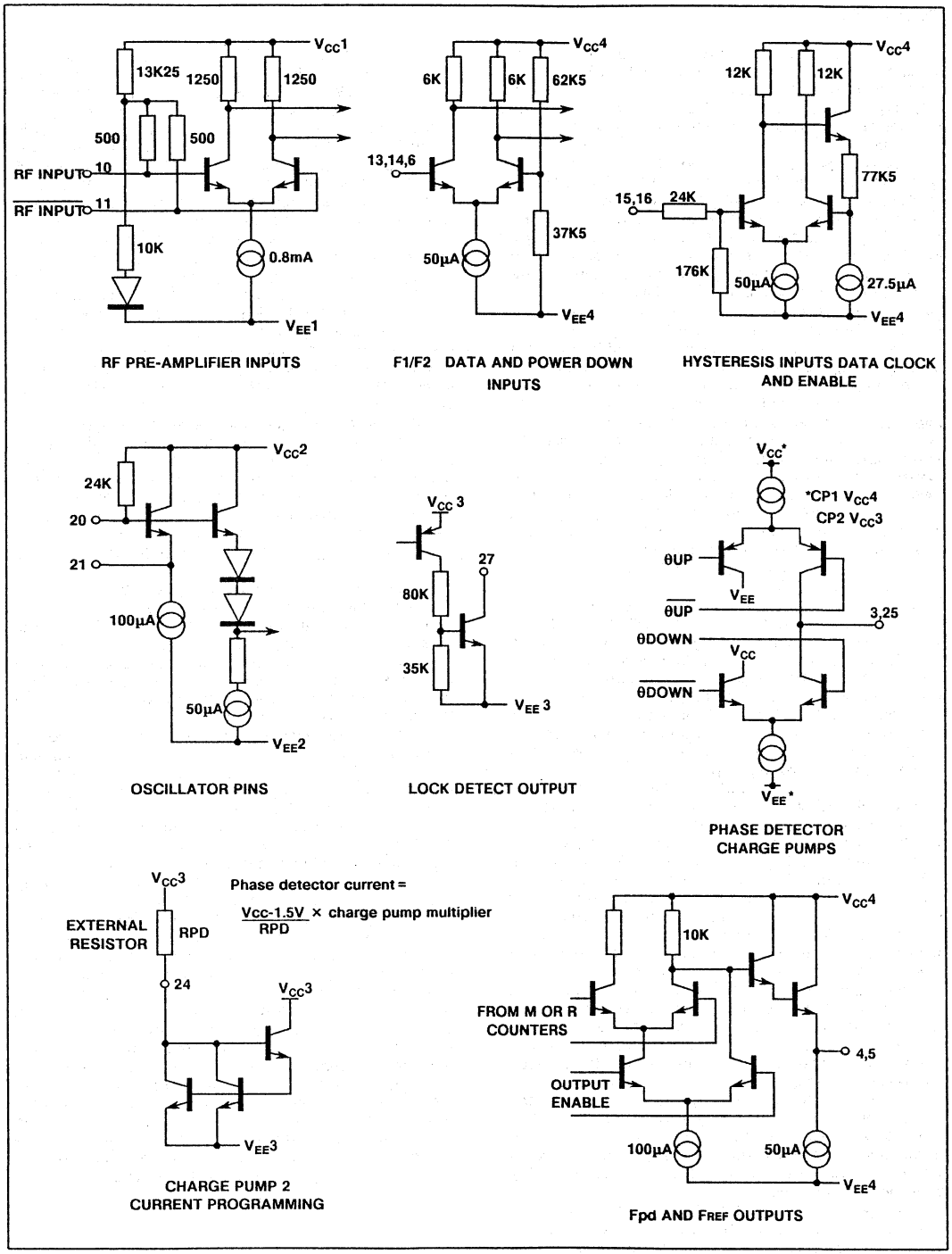


Fig. 8 Input and output interface diagrams

APPLICATIONS

A basic application using a single phase comparator is shown in figure 6. The SP8853 is a 1.5 GHz part, so good RF design techniques should be employed, including the use of a ground plane and suitable high frequency capacitors at the RF input and for power supply decoupling.

The RF input should be coupled to either pin 10 or 11, and the other pin decoupled to ground. The reference oscillator is of conventional Colpitts type with two capacitors required to provide a low impedance tap for the feedback signal to the transistor emitter. Typical values are shown in figure 6, although these may be varied to suit the loading requirements of particular crystals. Where a suitable reference signal already exists or where a very stable source is required, it is possible to apply an external reference as shown inset in figure 6. The amplitude should be kept below 0.5V RMS to avoid forward biasing the transistor collector base junction.

In some systems, it is useful to have an indication of phase lock. The output from pin 27 goes low when the output of charge pump 2 is between 2.25 and 2.75V and can be used to operate an LED to give visual indication of phase lock. Alternatively a pull-up resistor may be connected to V_{CC} and the output used to signal to the control microprocessor that the loop is locked thus speeding up system operation. The output current available from pin 27 is limited to 1.5mA. If this current is exceeded the logic low level will be uncertain.

The circuit diagram shown in figure 6 is a basic application with minimum component count which is nevertheless perfectly adequate for many applications. Charge pump 1 on pin 3 is used to drive the loop amplifier which provides the control voltage for the local oscillator. When charge pump 1 is used in this mode, the PD1 and PD2 bits in the reference programming word must be set to enable charge pump 1 continuously. This application could also use charge pump 2 output on pin 25 or if a higher phase comparator gain is required, pins 3 and 25 could be connected in parallel to use the combined output current from both charge pumps.

The lock detect circuit can be programmed to automatically disable charge pump 1 as shown in table 4. This feature can be used to reduce the system lock up time by connecting the charge pump outputs in parallel to the loop amplifier with a resistor, (shown dotted) in series with charge pump 2. This connection allows a relatively high current to be used from charge pump 1 to give short lock up time, and a low current to be set on charge pump 2 giving low reference frequency sidebands. The degree of lock up time improvement depends on the ratio of charge pump 1 to charge pump 2 currents.

When the loop is out of lock, both charge pumps will be enabled and will feed current to the loop amplifier to bring the oscillator to phase lock. The current from charge pump 2 will produce a voltage drop across the series resistor allowing operation of the lock detect circuit and enabling charge pump 1. The resistor must be chosen to give a voltage drop greater than 0.25V at the current level programmed for charge pump 2. When phase lock is achieved, there will be no charge pump current and therefore the voltage at pin 25 will be equal to that on the virtual earth point of the loop amplifier (2.5V), disabling charge pump 1.

Charge pump 1 should not be left open circuit when enabled as this prevents correct operation of the phase detector. The output on pin 3 should be biased to half supply with a pair of 4k7 resistors connected between supplies.

When charge pump 2 is used to drive the loop amplifier, the lock detect circuit will only give an out of lock indication when large frequency changes are made or when a frequency outside the range of the local oscillator is programmed. At other times the loop amplifier input is maintained at 2.5V by the action of the loop filter components. Again a resistor connected between pin 25 and the loop amplifier, producing a voltage drop greater than 0.25V at the charge pump current programmed will allow sensitive out of lock detection.

When phase lock detection is required using comparator 1 only, charge pump 2 output on (pin 25) should be biased to 2.5V using two equal value resistors across the supply. The values should be chosen to give a voltage change greater than 0.25V at the programmed comparator 2 charge pump current. A small capacitor connected from pin 28 to ground may be used to reduce chatter at the lock detect output. (see inset figure 6) A detailed block diagram showing the lock detect circuitry is shown in fig 3.

An amplifier is required to convert the current pulses from the phase comparator into a voltage of suitable magnitude to drive the chosen VCO. The choice of amplifier must be determined by the voltage swing required at the VCO to achieve the necessary frequency range, and in most cases an operational amplifier will be used to provide the essential characteristics of high input impedance, high gain and low output impedance required in this application.

Although it is expected that an operational amplifier will be used in most cases, a simple discrete design can be used and a suitable design is shown inset in figure 6. This arrangement can be particularly useful when the minimum VCO control voltage must be close to ground and where negative supplies are inconvenient. This form of amplifier is not suitable for use with charge pump 2 when the lock detect circuit is required.

When an operational amplifier is used in the inverting configuration shown in figure 6, the charge pump output is connected directly to the virtual earth point and will therefore operate at a voltage similar to that set on the non-inverting input. Normaly this operating point should be set at half supply using a potentiometer of two equal resistors, but if necessary this voltage can be set up to 1V higher or lower than half supply without detrimental effect. When the lock detect function is required on charge pump 2, the non inverting input must be at half supply.

The digital phase comparator and charge pump used on the SP8853 produces bi-directional current pulses in order to correct errors between the reference and VCO divider outputs. Once synchronisation is achieved, in theory no further output from the charge pump should be required, but in practice, due to leakage currents and particularly the input current of the amplifier, the capacitors forming the loop filter around the amplifier will gradually discharge, modifying the VCO voltage and requiring further outputs from the charge pump to restore the charge. The effect of this continuous correction of the local oscillator frequency, is to frequency modulate the VCO and thus produce sidebands at the reference frequency. In order to reduce this effect to a minimum, an amplifier with low input bias current is essential.

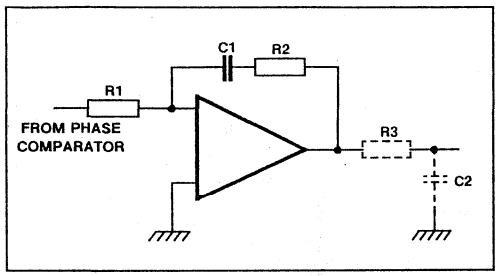


Fig. 9 Standard Form of Second Order Loop Filter

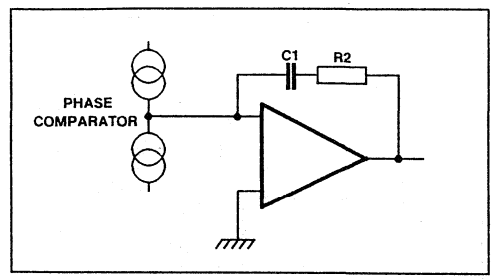


Fig.10 Modified Second Order Loop Filter

Loop calculations

Many frequency synthesiser designs use a second order loop with a loop filter of the form shown in figure 9.

In practice an additional RC time constant (shown dotted in figure 9) is often added to reduce noise from the amplifier. In addition any feedthrough capacitor or local decoupling at the VCO will be added to the value of C2. These additional components in fact form a third order loop, and if the values are chosen correctly, the additional filtering provided can considerably reduce the level of reference frequency sidebands and noise without adversly affecting the loop settling time. The calculation of values for both forms of loop is shown below.

Second Order Loop.

For this filter two equations are required to determine the time constants τ_1 and τ_2 where:

$$\tau_1 = C_1 R_1$$
$$\tau_2 = C_1 R_2$$

The equations are:

$$1 \quad \tau_1 = \frac{K_\theta K_0}{\omega_n^2 N}$$

$$2 \quad \tau_2 = \frac{2\zeta}{\omega_n}$$

where:

K_θ is the phase detector gain factor in V/Radian
K_0 is the VCO gain factor in radians second /Volt
N is the division ratio from VCO to reference frequency
ω_n is the natural loop bandwidth
ζ is the damping factor: normaly 0.7071

The SP8853 phase comparator is a current source rather than a conventional voltage source and has a gain factor specified in µA/radian. Since the equations deal with a filter where R_1 is feeding the virtual earth point of an operational amplifier from a voltage source, R_1 is setting the input current to the filter which is similar to the circuit shown in fig. 10 where a current source phase comparator is connected directly to the virtual earth point of the operational amplifier.

The equivalent voltage gain of the phase comparator can be calculated by assuming a value for R_1 and calculating a gain in volts/radian which would produce the set current.

The digital phase comparator used in the SP8853 is linear over a range of 2π radians and therefore the phase comparator gain is given by:

$$\frac{\text{phase comparator current setting µA/Radian.}}{2\pi}$$

The phase comparator gain in V/radian is therefore:

$$\frac{50\,\mu A \times 1K \text{ ohm}}{2\pi}$$

assuming a value of 1K for R_1 and 50µA for the phase comparator current setting, these values can now be inserted in equation 1 to obtain values for C_1 and equation 2 used to determine a value for R_2.

Example:

Calculate values for a second order loop with the following parameters.

Frequency to be synthesised	800Mhz
Reference frequency	100KHz
Division ratio N	$\frac{800MHz}{100KHz}$ = 8000
Natural loop frequency ω_n	500Hz
VCO gain factor K_0	2π x 10MHz/Volt
Damping factor ζ	0.7071
Phase comparator current setting	50µA

Assuming R_1 is 1K ohm, then the equivalent phase comparator gain K_θ in V/radian $= \frac{50\mu A}{2\pi} \times 1000$

$$K_\theta = 0.00796 \text{V/radian.}$$

$$\text{From equation 1} \quad \tau_1 \frac{0.00796 \times 2 \times \pi \times 10MHz}{(2 \times \pi \times 500)^2 \times 8000}$$

$$\tau_1 = 6.334 \times 10^{-6}$$

$$\text{From equation 2} \quad \tau_2 = \frac{2 \times 0.7071}{2 \times \pi \times 500}$$

$$\tau_2 = 4.50 \times 10^{-4}$$

$$\text{Now} \quad \tau_1 = C_1 R_1 \quad \therefore C_1 = \frac{6.334 \times 10^{-6}}{1Kohm}$$

1K is chosen value for R_1

$$C_1 = 6.33nF$$

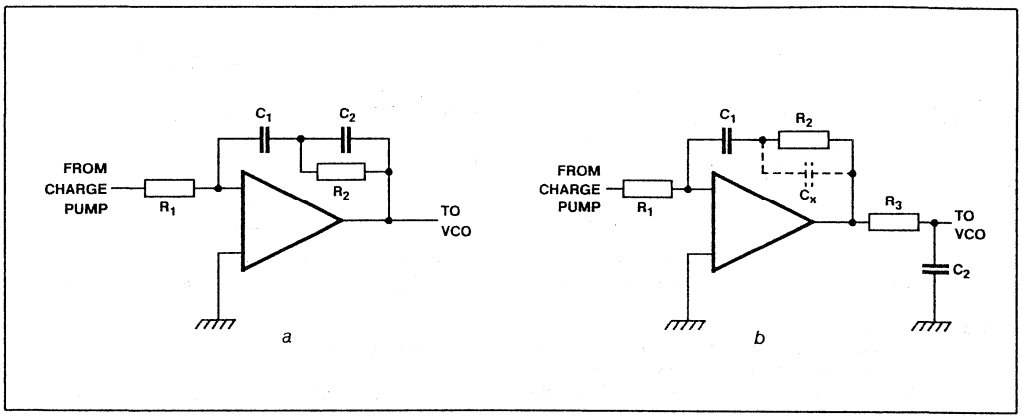


Fig. 11a and 11b Standard and Modified Form of Third Order Loop Filter

$$\tau_2 = C_1 R_2 \therefore \frac{4.50\times10^{-4}}{6.33\times10^{-9}} = R_2$$

$$R_2 = 71000 \text{ ohms}$$

Third Order Loop

The third order loop filter is normally shown as in figure 11. Figure 11b shows the circuit redrawn to use an RC time constant after the amplifier, allowing any feedthrough capacitance on the VCO line to be included in the loop calculations. Where the modified form in figure 11b is used it is advantageous to connect a small capacitor Cx of typically 100pF (shown dotted), across the amplifier to reduce sidebands caused by the amplifier being forced into non linear operation by the phase comparator pulses.

Three equations are required to determine the time constants, τ_1, τ_2 and τ_3 where :

for figure 11a

$$\tau_1 = C_1 R_1$$
$$\tau_2 = R_2 (C_1 + C_2)$$
$$\tau_3 = C_2 R_2$$

and for figure 11b

$$\tau_1 = C_1 R_1$$
$$\tau_2 = C_1 R_2$$
$$\tau_3 = C_2 R_3$$

The equations are:

1. $$\tau_1 = \frac{K_\theta K_0}{N\omega_n^2}\left[\frac{1+\omega_n^2\tau_2^2}{1+\omega_n^2\tau_3^2}\right]^{\frac{1}{2}}$$

2. $$\tau_2 = \frac{1}{\omega_n^2 \tau_3}$$

3. $$\tau_3 = \frac{-\tan\phi_0 + \frac{1}{\cos\phi_0}}{\omega_n}$$

Where:

K_θ is the phase detector gain factor in V/Radian
K_0 is the VCO gain factor in radians second/Volt
N is the total division ratio from VCO to reference frequency
ω_n is the natural loop bandwidth
ϕ_0 is the Phase margin normaly set to 45°

As in the second order filter example a value for R1 can be assumed and an equivalent gain K_θ in V/radian calculated from:

$$\frac{\text{phase comparator current setting } \mu\text{A/radian}}{2\pi} \times 1\text{K}$$

Where 1K ohm is the assumed value for R_1

These values can now be substituted in equation 1 to obtain a value for C_1 and equations 2 and 3 used to determine values for C_2 and R_2.

EXAMPLE

Calculate values for a loop with the following parameters.

Frequency to be synthesised:	800MHz
Reference frequency	100KHz
Division ratio	$\frac{800\text{MHz}}{100\text{KHz}} = 8000$
ω_n natural loop frequency	500Hz
K_0 VCO gain factor	2π x 10MHz/Volt
ϕ_0 phase margin	45°
Phase comparator current	50µA

assuming R_1 is 1K Ohm, then the equivalent phase comparator gain K_θ in V/radian is:

$$\frac{50\mu A}{2\pi} \times 1000 = 0.00796 \text{ V/Radian}$$

From equation 3:

$$\tau_3 = \frac{-\tan 45° + \frac{1}{\cos 45°}}{500\text{Hz} \times 2\pi} = \frac{0.4142}{3141.6}$$

$$\tau_3 = 1.318 \times 10^{-4}$$

From equation 2:

$$\tau_2 = \frac{1}{(500 \times 2 \times \pi)^2 \times 1.318 \times 10^{-4}}$$

$$\tau_2 = 7.687 \times 10^{-4}$$

Using these values in equation 1:

$$\tau_1 = \frac{7.96 \times 10^{-3} \times 2 \times \pi \times 10\text{MHz/V}}{8000 \times (2\pi \times 500)^2} \left[A\right]^{\frac{1}{2}}$$

Where A is:

$$\frac{1+\omega_n^2 \tau_2^2}{1+\omega_n^2 \tau_3^2} = \frac{1+(2\pi \times 500)^2 \times (7.687 \times 10^{-4})^2}{1+(2\pi \times 500)^2 \times (1.318 \times 10^{-4})^2}$$

$$\tau_1 = \frac{500141.6}{7.896 \times 10^{10}} \left[\frac{6.832}{1.1714}\right]^{\frac{1}{2}}$$

$$\tau_1 = 6.334 \times 10^{-6} \times 2.415$$

$$\tau_1 = 1.53 \times 10^{-5}$$

now $\tau_1 = C_1 R_1$

$$\therefore C_1 = \frac{1.53 \times 10^{-5}}{1\text{K Ohm}} \quad (R_1 \text{ is chosen as 1K})$$

$$C_1 = 0.0153\mu\text{F}$$

for figure 11a $\tau_2 = R_2 (C_1 + C_2)$

for figure 11a $\tau_3 = C_2 R_2$

substituting for C_2

$$\tau_2 = R_2 \left[C_1 + \frac{\tau_3}{R_2}\right] \quad \therefore \tau_2 = R_2 C_1 + \tau_3$$

$$\therefore R_2 = \frac{\tau_2 - \tau_3}{C_1} = \frac{7.687 \times 10^{-4} - 1.318 \times 10^{-4}}{0.0153 \times 10^{-6}}$$

$$R_2 = 41627 \text{ Ohms}$$

$$\tau_3 = C_2 R_2 \quad \therefore C_2 = \frac{\tau_3}{R_2} = \frac{1.318 \times 10^{-4}}{41627}$$

$$C_2 = 3.17\text{nF}$$

for figure 11b $\tau_1 = C_1 R_1 \quad \therefore C_1 = \frac{1.53 \times 10^{-5}}{1\text{k}}$

$$C_1 = 0.0153\mu\text{F}$$

$$\tau_2 = C_1 R_2 \quad \therefore R_2 = \frac{7.687 \times 10^{-4}}{1.53 \times 10^{-8}}$$

$$R_2 = 50.242 \text{ Kohms}$$

$$\tau_3 = C_2 R_3$$

Since both values are independent of the other components, either C2 or R3 can be chosen and the other calculated.

assume R_3 = 1K ohm $\therefore C_2 = \frac{1.318 \times 10^{-4}}{1000}$

$$C_2 = 1.318 \times 10\text{-}7$$

$$C_2 = 0.1318\mu\text{F}$$

SP8854D

1.7GHz PARALLEL LOAD PROFESSIONAL SYNTHESISER

The SP8854D is one of a family of parallel load synthesisers containing all the elements apart from the loop amplifier to fabricate a PLL synthesis loop. Other parts in the series are the SP8852D which is fully programmable requiring two 16 word bit words to set the RF and reference counters, and the SP8855D which is programmed by hard wired links or switches.

The SP8854D is programmed using a 16 bit parallel data bus. This Data is stored in an internal buffer. The 10 bit programmable reference divider is programmed by connecting the 10 programming pins either to ground or +5V. The device can therefore be programmed with a single transfer from the control microprocessor. Hard wired inputs can also control the F_{pd} and F_{ref} outputs and the control sense of the loop.

FEATURES

- 1.7GHz Operating Frequency
- Single 5V Supply Operation
- Low Power Consumption <1.3W
- High Comparison Frequency 20MHz
- High Gain Phase Detector 1mA/rad
- Zero "Dead Band" Phase Detector
- Wide Range of RF and Reference Divide Ratios
- Programming by Single Word Data Transfer

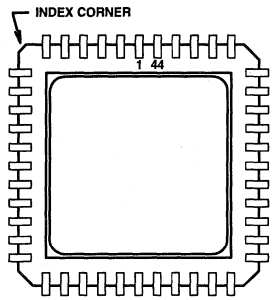
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	−0.3V to 6V
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +100°C
Prescaler & reference Input Voltage	2.5V p−p
Data inputs	V_{CC} +0.3V
	V_{EE} −0.3V

ORDERING INFORMATION

SP8854D KG HCAR (non standard temperature range −55°C to +100°C standard product screening)

SP8854D IG HCAR (Industrial temperature range −40°C to +85°C standard product screening)



HC44

Pin	Description	Pin	Description
1	Input bus bit 10	23	Control direction
2	Input bus bit 9	24	F_{pd}*
3	Input bus bit 8	25	F_{ref}*
4	Input bus bit 7	26	+5V
5	Input bus bit 6	27	Ref. osc capacitor
6	Input bus bit 5	28	Ref in/XTAL
7	Input bus bit 4	29	Ref divider bit 9
8	Input bus bit 3	30	Ref divider bit 8
9	Input bus bit 2	31	Ref divider bit 7
10	Input bus bit 1	32	Ref divider bit 6
11	Input bus bit 0	33	Ref divider bit 5
12	0V (prescaler)	34	Ref divider bit 4
13	RF input	35	Ref divider bit 3
14	RF input	36	Ref divider bit 2
15	V_{CC} +5V (prescaler)	37	Ref divider bit 1
16	V_{EE} 0V	38	Ref divider bit 0
17	Lock detect output	39	Strobe
18	C−lock detect	40	Input bus bit 15
19	R_{set}	41	Input bus bit 14
20	Charge pump output	42	Input bus bit 13
21	Charge pump ref.	43	Input bus bit 12
22	F_{pd}/F_{ref} enable	44	Input bus bit 11

* F_{pd} and F_{ref} outputs are reversed using the control direction input. The table above is correct when pin 23 is high.

Fig. 1 Pin connections – top view

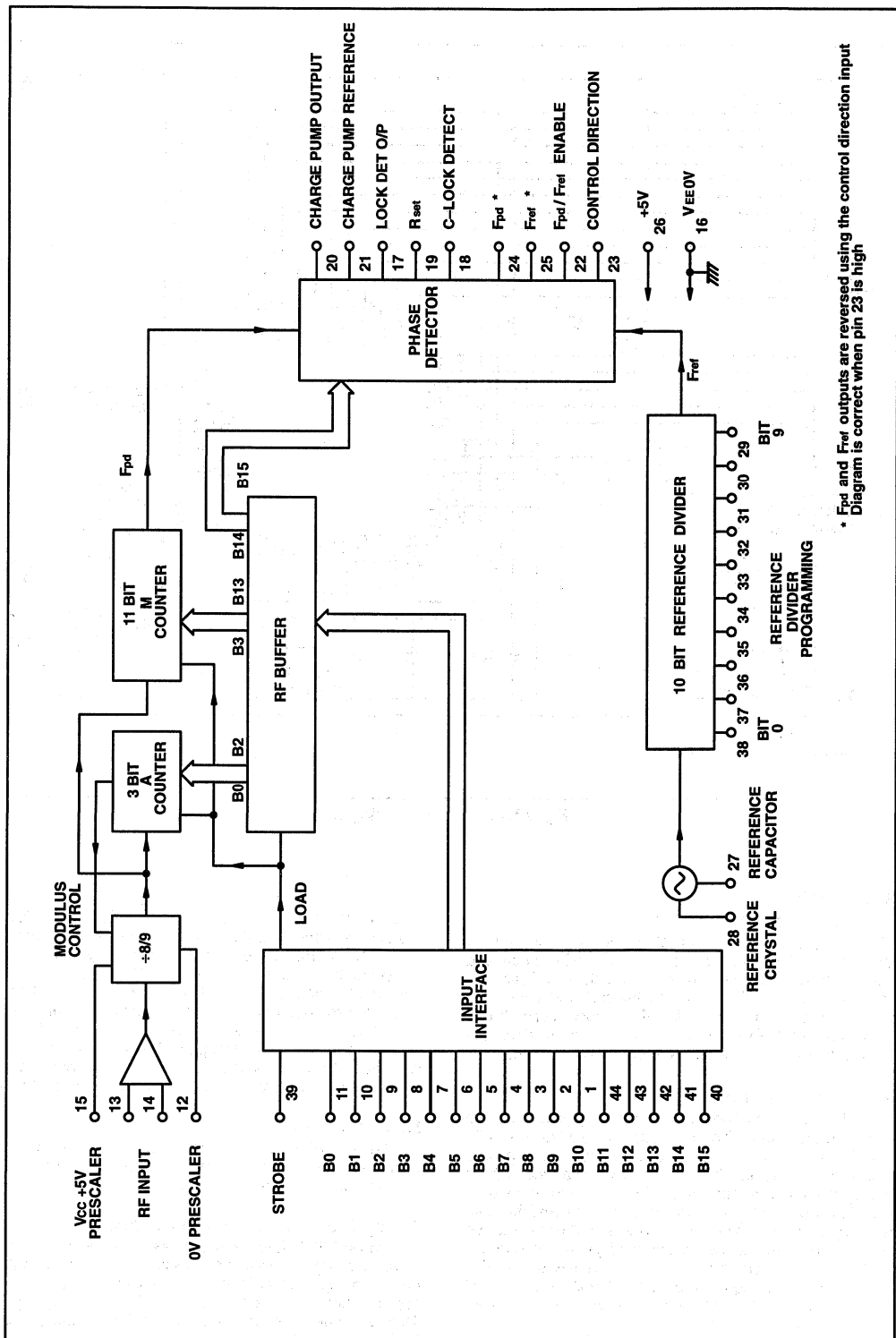


Fig. 2 SP8854D block diagram

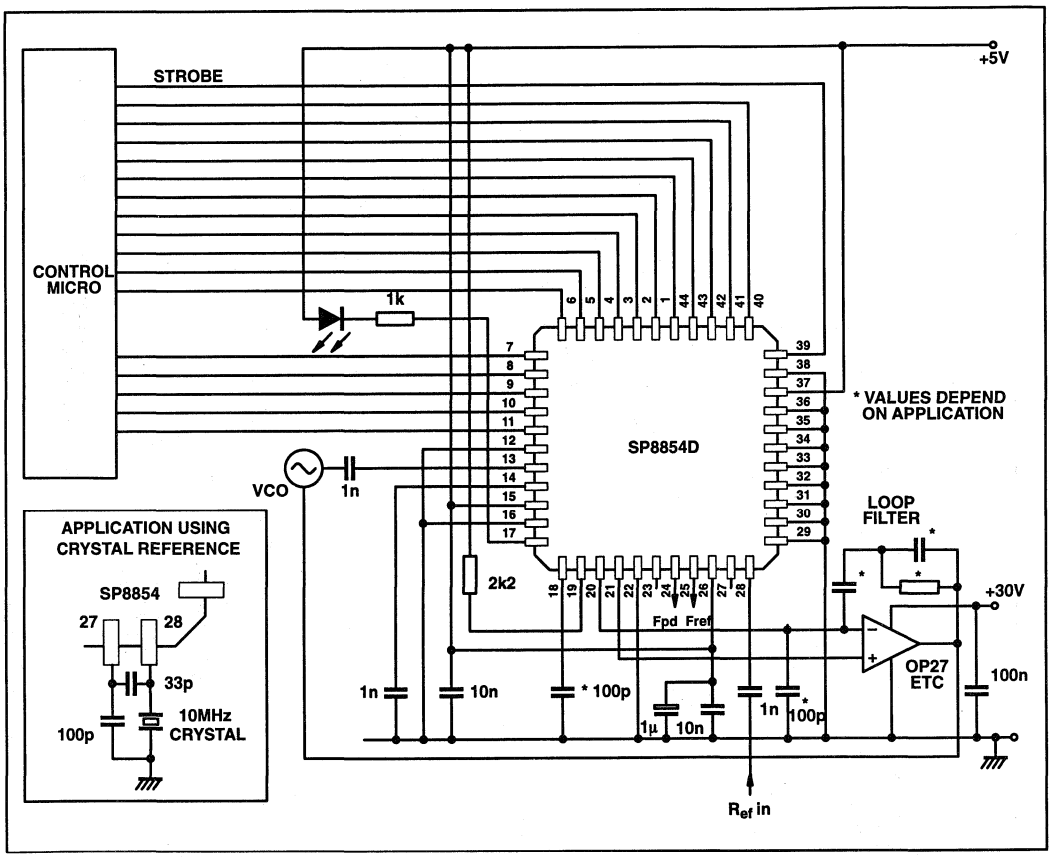


Fig. 3 Typical application diagram

DESCRIPTION

Prescaler and AM counter

The programmable divider chain is of A M counter construction and therefore contains a dual modulus front end prescaler, an A counter which controls the dual modulus ratio and an M counter which performs the bulk multi–modulus division. A programmable divider of this construction has a division ratio of MN+A and a minimum integer steppable division ratio of N(N–1), where N is the prescaler ratio.

Data entry and storage

Data is loaded from the 16 bit bus by applying a positive pulse to the strobe input. The input bus can be driven from TTL or CMOS logic levels. When the strobe input is low, the bus inputs are isolated and the data can be changed without affecting the programmed state. When the strobe input is taken high, the A and M and counters are reset and the input data is applied to the internal storage register. When the strobe input is again taken low, the data on the input bus is stored in the internal register and the A and M counters released. The strobe input is level triggered so that if the data is changed whilst the input is high, the final value before the strobe goes low will be stored.

In order to prevent disturbances on the VCO control voltage when frequency changes are made, the strobe input disables the charge pump outputs when high. During this period the VCO control voltage will be maintained by the loop filter components around the loop amplifier, but due to the combined effects of the amplifier input current and charge pump leakage a gradual change will occur. In order to reduce the change, the duration of the strobe pulse should be minimised. Selection of a loop amplifer with low input current will reduce the VCO voltage droop during the strobe pulse and result in minimum reference sidebands from the synthesiser.

Reference input

The reference source can be either driven from an external sine or square wave source of up to 100MHz or a crystal can be connected as shown in Fig. 3.

Phase Comparator and Charge pump

The SP8854D has a digital phase/frequency comparator driving a charge pump with programmable current output. The charge pump current level at the minimum gain setting is approximately equal to the current fed into the R_{set} input pin 19 and can be increased by programming the bus according to Table 1 by up to 4 times.

Bit 15	Bit 14	Current Multiplication Factor
0	0	1.0
0	1	1.5
1	0	2.5
1	1	4.0

Table 1

$$\text{Pin 19 current} = \frac{V_{cc} - 1.6V}{R_{set}}$$

$$\text{Phase detector gain} = \frac{I_{pin\ 19}(mA) \times \text{multiplication factor}}{2\pi}\ mA/\text{radian}$$

To allow for control direction changes introduced by the design of the PLL, pin 23 is used to reverse the sense of the phase detector by transposing the F_{pd} and F_{ref} connections. In order that any external phase detector will also be reversed, the F_{pd}/F_{ref} outputs are interchanged by pin 23 as shown in Table 2.

Output for RF Phase Lag	
Control direction pin 23	Pin 20
1	Current Source
0	Current Sink

Table 2

The F_{pd} and F_{ref} signals to the phase detector are available as ECL 10k levels on pin 24 and 25 and may be used to monitor the frequency input to the phase detector or used in conjunction with an external phase detector. The outputs are disabled by taking pin 22 low. When the F_{pd} and F_{ref} outputs are to be used at high frequencies, an external pull down resistor of minimum value 330Ω may be connected to ground to reduce the fall time of the output pulse.

The charge pump connections to the loop amplifier consist of the charge pump output and the charge pump reference. The matching of the charge pump up and down currents will only be maintained if the charge pump output is held at a voltage equal to the charge pump reference using an operational amplifier to produce a virtual earth condition at pin 20. Because the operational amplifiers will have limited response time compared with the pulse frequency at the charge pump output, pin 20 will not remain at the same voltage as pin 21 without an additional capacitor to ground to decouple the high frequencies. The value of capacitor required will vary with comparison frequency and the bandwidth of the op amp but a value between 50pF and 5nF will normally be required.

The lock detect circuit can drive an LED to give visual indication of phase lock or provide an indication to the control system if a pull up resistor is used in place of the LED. A small capacitor connected from the c–lock detector pin to ground may be used to delay lock detect indication and remove glitches produced by momentary phase coincidence during lock up.

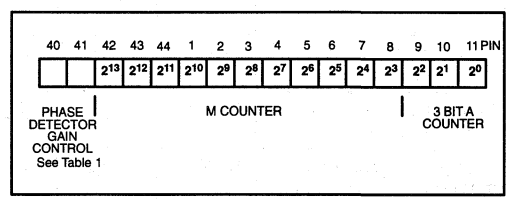


Fig. 4 Programming pin allocation

ELECTRICAL CHARACTERISTICS

Guaranteed over the full temperature and supply voltage range (unless otherwise stated)
Temperature T_{amb} for KG parts –55°C and +100 °C
Temperature T_{amb} for IG parts –40°C and +85°C
Supply Voltage V_{CC} = 4.75V and 5.25V

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	15, 26		180	240	mA	
RF input sensitivity	13, 14	–5.0		+7.0	dBm	100MHz to 1.7GHz See Fig. 8
RF division ratio	13,14,24	56		16383		
Reference division ratio	28, 25	1		1023		
Comparison frequency	28,24,25			50	MHz	
Reference input frequency	28	10		100	MHz	Reference division ratio ≥ 2 See Note 1
Reference input voltage	28	0	+6	+10	dBm	
F_{ref}/F_{pd} output voltage high	24, 25		–0.8		Vwrt V_{CC}	330Ω to 0V
F_{ref}/F_{pd} output voltage low	24, 25		–1.4		Vwrt V_{CC}	330Ω to 0V
Lock detect output voltage	17	2	300	500	mV	I_{out} = 3mA
Charge pump current at multiplication factor =1	19,20,21	±1.4	±1.5	±1.7	mA	$V_{pin\ 20} = V_{pin\ 21}$, $I_{pin\ 19}$ = 1.6mA
Charge pump current at multiplication factor =1.5	19,20,21	±2.0	±2.3	±2.5	mA	$V_{pin\ 20} = V_{pin\ 21}$, $I_{pin\ 19}$ = 1.6mA
Charge pump current at multiplication factor = 2.5	19,20,21	±3.4	±3.8	±4.1	mA	$V_{pin\ 20} = V_{pin\ 21}$, $I_{pin\ 19}$ = 1.6mA
Charge pump current at multiplication factor = 4.0	19,20,21	±5.4	±6.1	±6.5	mA	$V_{pin\ 20} = V_{pin\ 21}$, $I_{pin\ 19}$ = 1.6mA
Input bus high logic level	1–11,22 23,29,44	3.5			V	
Input bus low logic level	1–11,22, 23,29–44			1	V	
Input bus current source	1–11,22, 23,29–44	–200			µA	V_{IN} = 0V
Input bus current sink	1–11,22, 23,29–44			10	µA	$V_{IN} = V_{CC}$
Up down current matching	20			±2	%	$V_{pin\ 20} = V_{pin\ 21}$, $I_{pin\ 19}$ = 1.6mA
Charge pump reference voltage	21			V_{CC} – 0.5	V	$I_{pin\ 19}$ = 1.6mA current multiplication factor =1
Charge pump reference voltage	21	V_{CC}–1.6			V	$I_{pin\ 19}$ = 1.6mA current multiplication factor = 4
R_{set} current	19	0.5		2	mA	See Note 2
R_{set} Voltage	19		1.6		V	$I_{pin\ 19}$ = 1.6 mA
C–lock detect current	18		+10		µA	V_{pin}18=4.7V
Strobe pulse width		50			nS	Note 3
Data set up time		100			nS	Note 3

Notes: 1. Lower reference frequencies may be used if slew rates are maintained.

2. Pin 19 current x multiplication factor must be less than 5mA if charge pump current accuracy is to be maintained.

3. Guaranteed but not tested.

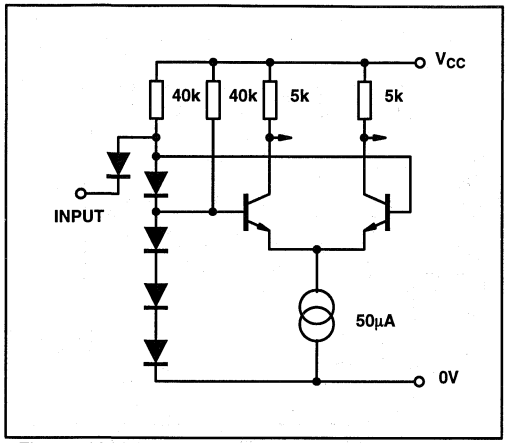


Fig. 5a 16 bit input bus, F_{pd}/F_{ref} enable, control direction, reference divider inputs and strobe

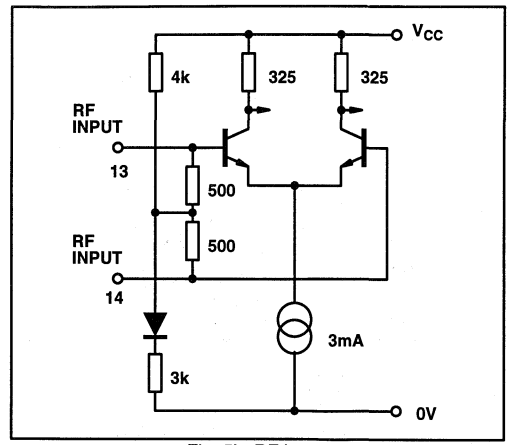


Fig. 5b RF inputs

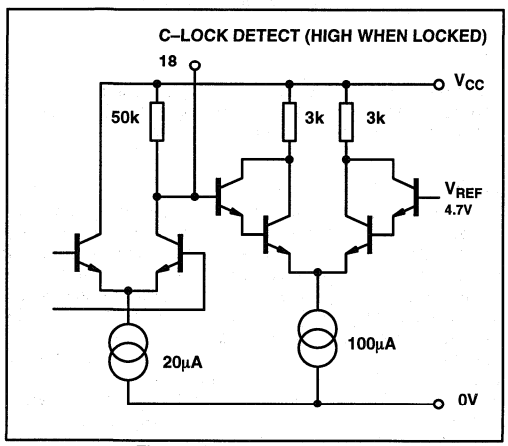


Fig. 5c Lock detect decouple

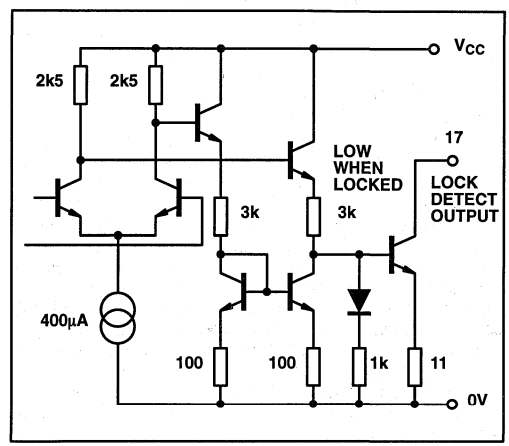


Fig. 5d Lock detect output

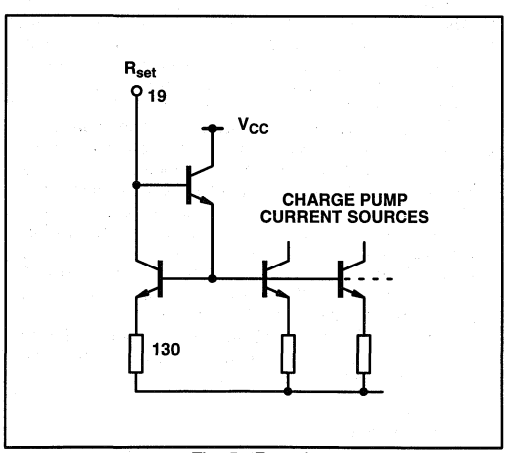


Fig. 5e R_{set} pin.

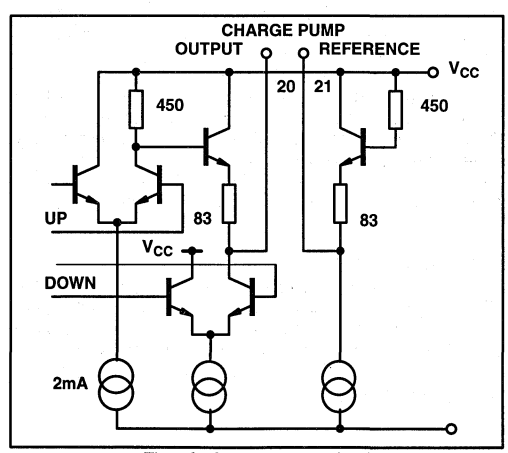


Fig. 5f Charge pump circuit

Fig. 5 Interface circuit diagrams

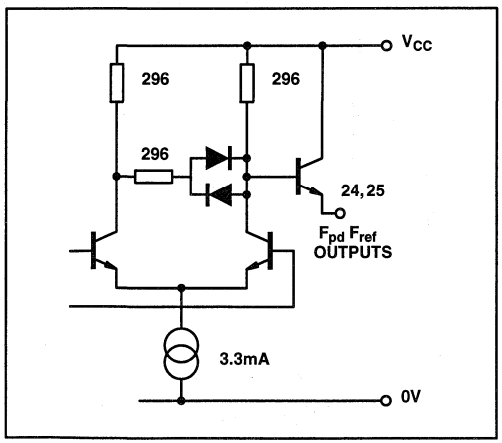


Fig. 5g F_{pd} and F_{ref} outputs

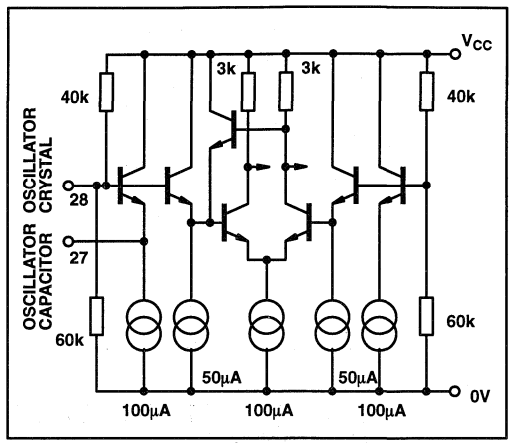


Fig. 5h Reference oscillator

Fig. 5 Interface circuit diagrams (cont)

APPLICATIONS

RF layout

The SP8854D can operate with input frequencies up to 1.7GHz but to obtain optimum performance, good RF layout practices should be used. A suitable layout technique is to use double sided printed circuit board with through plated holes. Wherever possible the top surface on which the SP8854D is mounted should be left as a continuous sheet of copper to form a low impedance earth plane. The ground pins 12 and 16 should be connected directly to the earth plane. Pins such as V_{CC} and the unused RF input should be decoupled with chip capacitors mounted as close to the device pin as possible with a direct connection to the earth plane, suitable values are 10nF for the power supplies and 1nF for the RF input pin. A larger decoupling capacitor mounted as close as possible to pin 26 should be used to prevent modulation of V_{CC} by the charge pump pulses. The R_{set} resistor should also be mounted close to the R_{set} pin to prevent noise pickup, and the capacitor connected from the charge pump output should be a chip component with short connections to the SP8854D.

When the reference is derived from a crystal connected to pins 27 and 28 as shown in Fig. 3 the oscillator components are best mounted close to the SP8854D.

All signals such as the programming inputs, RF in, reference in and the connections to the op–amp are best taken through the pc board adjacent to the SP8854D with through plated holes allowing connections to remote points without fragmenting the earth plane. The GEC Plessey evaluation board shown in Fig.6 uses this layout technique.

Programming bus

The input pins are designed to be compatible with TTL or CMOS logic with a switching threshold set at about 2.4V by three forward biased base emitter diodes. The inputs will be taken high by an internal pull up resistor if left open circuit but for best noise immunity it is better to connect unused inputs directly to V_{CC} or ground.

RF inputs

The prescaler has a differential input amplifer to improve input sensitivity. Generally the input drive will be single ended and the RF signal should be AC coupled to either of the inputs using a chip capacitor. The remaining input should be decoupled to ground, again using a chip capacitor. The inputs can be driven differentially but the input circuit should not provide a DC path between inputs or to ground.

Lock detect circuit

The lock detect circuit uses the up and down correction pulses from the phase detector to determine whether the loop is in or out of lock. When the loop is locked, both up and down pulses are very narrow compared to the reference frequency, but the pulse width in the out of lock condition continuously varies, depending on the phase difference between the outputs of the reference and RF counters. The logical AND of the up and down pulses is used to switch a 20mA current sink to pin 18 and a 50k resistor provides a load to V_{CC}. The circuit is shown in Fig. 5c. When lock is established, the narrow pulses from the phase detector ensure that the current source is off for the majority of the time and so pin 18 will be pulled high by the 50k resistor. A voltage comparator with a switching threshold at about 4.7V monitors the voltage at pin 18 and switches pin 17 low when pin 18 is more positive than the 4.7V threshold. When the loop is unlocked, the frequency difference at the counter outputs will produce a cyclic change in pulse width from the phase detector outputs with a frequency equal to the difference in frequency at the reference and RF counter outputs. A small capacitor connected to pin 18 prevents the indication of false phase lock conditions at pin 17 for momentary phase coincidence. Because of the variable width pulse nature of the signal at pin 18 the calculation of a suitable capacitor value is complex, but if an indication with a delay amounting to several times the expected lock up time is acceptable, the delay will be approximately equal to the time constant of the capacitor on pin 18 and the internal 50k resistor. If a faster indication is required, comparable with the loop lock up time, the capacitor will need to be 2–3 times smaller than the time constant calculation suggests. The time to respond to an out of lock condition is 2–3 times less than that required to indicate lock.

Charge pump circuit

The charge pump circuit converts the variable width up and down pulses from the phase detector into adjustable current pulses which can be directly connected to the loop amplifer. The magnitude of the current and therefore the phase detector gain can be modified when new frequency data is entered to

compensate for change in the VCO gain characteristic over its frequency band. The charge pump pulse current is determined by the current fed into pin 19 and is approximately equal to pin 19 current when the programmed multiplication ratio is one. The circuit diagram Fig. 5e shows the internal components on pin 19 which mirror the input current into the charge pump. The voltage at pin 19 will be approximately 1.6V above ground due to two V_{be} drops in the current mirror. This voltage will exhibit a negative temperature coefficient, causing the charge pump current to change with chip temperature by up to 10% over the full military temperature range if the current programming resistor is connected to V_{CC} as shown in the application diagram Fig. 3. In critical applications where this change in charge pump current would be too large the resistor to pin 19 could be increased in value and connected to a higher supply to reduce the effect of V_{be} variation on the current level. A suitable resistor connected to a 30V supply would reduce the variation in pin 19 current due to temperature to less than 1.5%. Alternatively a stable current source could be used to set pin 19 current.

The charge pump output on pin 20 will only produce symmetrical up and down currents if the voltage is equal to that on the voltage reference pin 21. In order to ensure that this voltage relationship is maintained, an operational amplifier must be used as shown in the typical application Fig. 3. Using this configuration pin 20 voltage will be forced to be equal to that on pin 21 since the operational amplifier differential input voltage will be no more than a few millivolts (the input offset voltage of the amplifier). When the synthesiser is first switched on or when a frequency outside the VCO range is programmed the amplifier output will limit, allowing pin 20 voltage to differ from that on pin 21. As soon as an achievable frequency value is programmed and the amplifier output starts to slew the correct voltage relationship between pin 20 and 21 will be restored. Because of the importance of voltage equality between the charge pump reference and output pins, a resistor should never be connected in series with the operational amplifier inverting input and pin 20 as is the case with a phase detector giving voltage outputs. Any current drawn from the charge pump reference pin should be limited to the few micro amps input current of a typical operational amplifier. A resistor between the charge pump reference and the non inverting input could be added to provide isolation but the value should not be so high that more than a few millivolts drop are produced by the amplifier input current.

When selecting a suitable amplifer for the loop filter, a number of parameters are important; input offset voltage in most designs is only a few milivolts and an offset of 5mV will produce a mismatch in the up and down currents of about 4% with the charge pump multiplication factor set at 1. The mismatch in up down currents caused by input offset voltage will be reduced in proportion to the charge pump multiplication factor in use. If the linearity of the phase detector about the normal phase locked operating point is critical, the input offset voltage of most amplifiers can be adjusted to near zero by means of a potentiometer.

The charge pump reference voltage on pin 21 is about 1.3V below the positive supply and will change with temperature and with the programmed charge pump multiplication factor. In many cases it is convenient to operate the amplifier with the negative power supply pin connected to 0V as this removes the need for an additional power supply. The amplifier selected must have a common mode range to within 3.4V (minimum charge pump reference voltage) of the negative supply pin to operate correctly without a negative supply. Most popular amplifiers can be operated from a 30V positive supply to give a wide VCO voltage drive range and have adequate common mode range to operate with inputs at +3.4V with respect to the negative supply. Input bias and offset current levels to most operational amplifiers are unlikely to be high enough to significantly affect the accuracy of the charge pump circuit currents but the bias current can be important in reducing reference side bands and local oscillator drift during frequency changes. When the loop is locked, the charge pump produces only very narrow pulses of sufficient width to make up for any charge lost from the loop filter components during the reference cycle. The charge lost will be due to leakage from the charge pump output pin and to the amplifier input bias current, the latter usually being more significant. The result of the lost charge is a sawtooth ripple on the VCO control line which frequency modulates the phase locked oscillator at the reference frequency and its harmonics. A similar effect will occur whenever the strobe input is taken high during a programming sequence. In this case the charge pump is disabled when the strobe input is high and any leakage current will cause the oscillator to drift off frequency. To reduce this effect, the duration of the strobe pulse should be minimised.

The necessity to maintain the charge pump output voltage at the same voltage as the reference pin has already been mentioned. This is important because the design of the positive current source has no voltage compliance and any departure from the reference voltage will introduce an error in the positive current source. The operational amplifier will maintain the DC charge pump voltage very close to the reference but the current from the charge pump is a series of pulses at the reference frequency. When the loop is locked the output pulses are very short in duration, the only current necessary being that required to restore and charge lost during the reference period. The virtual earth mechanism which maintains the charge pump output at the reference voltage depends on the amplifier having significant gain, but the narrow pulses from the charge pump are so short that the amplifier output will be unable to respond, allowing the input voltage to change and the pulse magnitude to be effectively reduced, introducing a non linearity in the phase detector characteristic at the phase locked point.

The capacitor shown connected from the charge pump output pin to ground on the typical application diagram Fig. 3 is intended to decouple the output at high frequencies, preventing voltage changes at the amplifier input which can not be corrected by the feedback response. The capacitor should be a high frequency type mounted close to the charge pump pin with short connection to the earth plane as the frequency content of the charge pump pulses extends to very high frequencies. A suitable value for this component is very difficult to calculate as its value depends on many factors including the bandwidth of the amplifier used in the loop filter and how critical the application is in terms of phase detector linearity. A value between 50pF and 5nF will suit most applications and the size of capacitor can be increased well beyond that necessary to restore linearity of the phase detector without ill effect. Many less critical applications will operate satisfactorily without this capacitor.

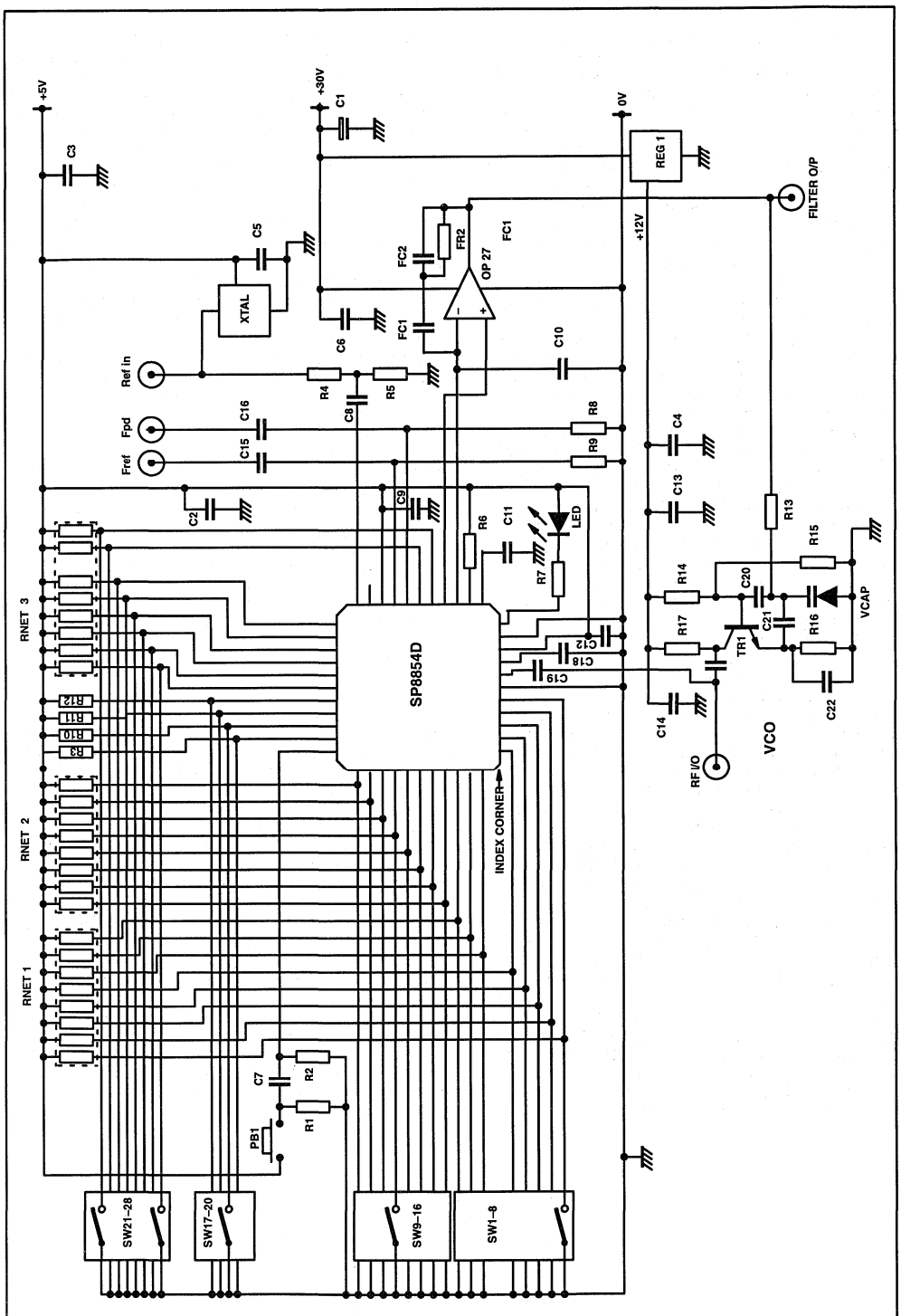


Fig. 6 Application board schematic

F_{pd} and F_{ref} outputs

These outputs provide access to the outputs from the RF and reference dividers and are provided for monitoring purposes during product development or test, and for connection of an external phase detector if required. the output circuit is of ECL type, the circuit diagram being shown in Fig. 5g. The outputs can be enabled or disabled under software control by the address 0 control word but are best left in the disabled state when not required as the fast edge speeds on the output can increase the level of reference sidebands on the synthesised oscillator.

The emitter follower outputs have no internal down resistor to save current and if the outputs are required an external pull down resistor should be fitted.The value should be kept as high as possible to reduce supply current, about 2.2k being suitable for monitoring with a high impedance oscilloscope probe or for driving an AC coupled 50ohm load. A minimum value for the pull down resistor is 330ohms. When the F_{pd} and F_{ref} outputs are disabled the output level will be at the logic low level of about 3.5V so that the additional supply current due to the load resistors will be present even when the outputs are disabled.

Reference input

The reference input circuit functions as an input amplifier or crystal oscillator. When an external reference signal is used this is simply AC coupled to pin 28, the base of the input emitter follower. When a low phase noise synthesiser is required the reference signal is critical since any noise present here will be multiplied by the loop. To obtain the lowest possible phase noise from the SP8854D it is best to use the highest possible reference input frequency and to divide this down internally to obtain the required frequency at the phase detector. The amplitude of the reference input is also important, and a level close to the maximum will give the lowest noise. When the use of a low reference input frequency say 4–10MHz is essential some advantage may be gained by using a limiting amplifier such as a CMOS gate to square up the reference input.

In cases where a suitable reference signal is not available, it may be more convenient to use the input buffer as a crystal oscillator in this case the emitter follower input transistor is connected as a colpitts oscillator with the crystal connected from the base to ground and with the feedback necessary for oscillation provided by a capacitor tap at the emitter. The arrangement is shown inset in Fig. 3

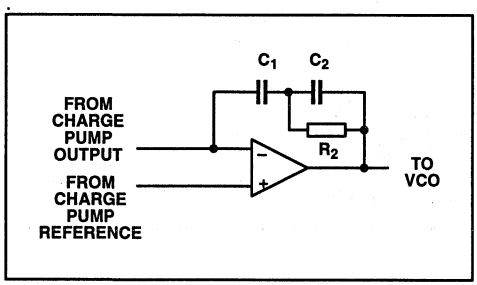


Fig. 7. Third order loop filter circuit diagram

Loop Filter Design

Generally the third order filter configuration shown in Fig.7 gives better results than the more commonly used second order because the reference sidebands are reduced. Three equations are required to determine values for the three constants where;

$$\tau_1 = C_1$$
$$\tau_2 = R_2 (C_1 + C_2)$$
$$\tau_3 = C_2 R_2$$

The equations are;

1 $$\tau_1 = \frac{K_\phi K_0}{N\omega_n^2}\left[\frac{1+\omega_n^2\tau_2^2}{1+\omega_n^2\tau_3^2}\right]^{1/2}$$

2 $$\tau_2 = \frac{1}{\omega_n^2\tau_3}$$

3 $$\tau_3 = \frac{-\tan\Phi_0 + \frac{1}{\cos\Phi_0}}{\omega_n}$$

Where;

- K_ϕ is the phase detector gain factor in mA/radian
- K_0 is the VCO gain factor in radian/second/Volt
- N is the total division ratio from VCO to reference frequency
- ω_n is the natural loop bandwidth
- Φ_0 is the phase margin normally set to 45°

Since the phase detector is linear over a range of 2π radian, K_ϕ can be calculated from

K_ϕ = Phase comparator current setting/2π mA/radian

These values can now be substituted in equation 1 to obtain a value for C_1 and equation 2 and 3 used to determine values for C_2 and R_2

EXAMPLE

Calculate values for a loop with the following parameters

Frequency to be synthesised:	1000MHz
Reference frequency	10MHz
Division ratio	1000MHz/10MHz = 100
ω_n natural loop frequency	100kHz
K_0 VCO gain factor	2π x 10MHz/Volt
Φ_0 phase margin	45°
Phase comparator current	6.3mA

The phase detector gain factor K_ϕ
= 6.3mA /2π = 1mA/radian

From equation 3:

$$\tau_3 = \frac{-\tan 45° + \frac{1}{\cos 45°}}{100\text{kHz} \times 2\pi} = \frac{0.4142}{628319}$$

$$\tau_3 = 659 \times 10^{-9}$$

From equation 2:

$$\tau_2 = \frac{1}{(100\text{kHz} \times 2\pi)^2 \times 659 \times 10^{-9}}$$

$$\tau_2 = 3.844 \times 10^{-6}$$

Using these values in equation 1:

$$\tau_1 = \frac{1 \times 10^{-3} \times 2\pi \times 10\text{MHz/V}}{100 \times (2\pi \times 100\text{kHz})^2}\ [\text{A}]^{1/2}$$

Where A is :

$$\frac{1 + \omega_n^2 \tau_2^2}{1 + \omega_n^2 \tau_3^2} = \frac{1 + (2\pi \times 100\text{kHz})^2 \times (3.844 \times 10^{-6})^2}{1 + (2\pi \times 100\text{kHz})^2 \times (659 \times 10^{-9})^2}$$

$$\tau_1 = \frac{62832}{39.48 \times 10^{12}} \left[\frac{6.833}{1.1714}\right]^{\frac{1}{2}}$$

$$\tau_1 = 1.59 \times 10^{-9} \times 2.415$$

$$\tau_1 = 3.84 \times 10^{-9}$$

Now $\tau_1 = C_1 \therefore C_1 = 3.84\text{nF}$

$$\tau_2 = R_2 (C_1 + C_2)$$

$$\tau_3 = C_2 R_2$$

Substituting for C_2

$$\tau_2 = R_2\left[C_1 + \frac{\tau_3}{R_2}\right] \quad \therefore \tau_2 = R_2 C_1 + \tau_3$$

$$\therefore R_2 = \frac{\tau_2 - \tau_3}{C_1} = \frac{3.844 \times 10^{-6} - 659 \times 10^{-9}}{9.61 \times 10^{-9}}$$

$R_2 = 829.4\Omega$

$$\tau_3 = C_2 R_2 \therefore C_2 = \frac{\tau_3}{R_2} = \frac{659 \times 10^{-9}}{829.4}$$

$C_2 = 0.794\text{nF}$

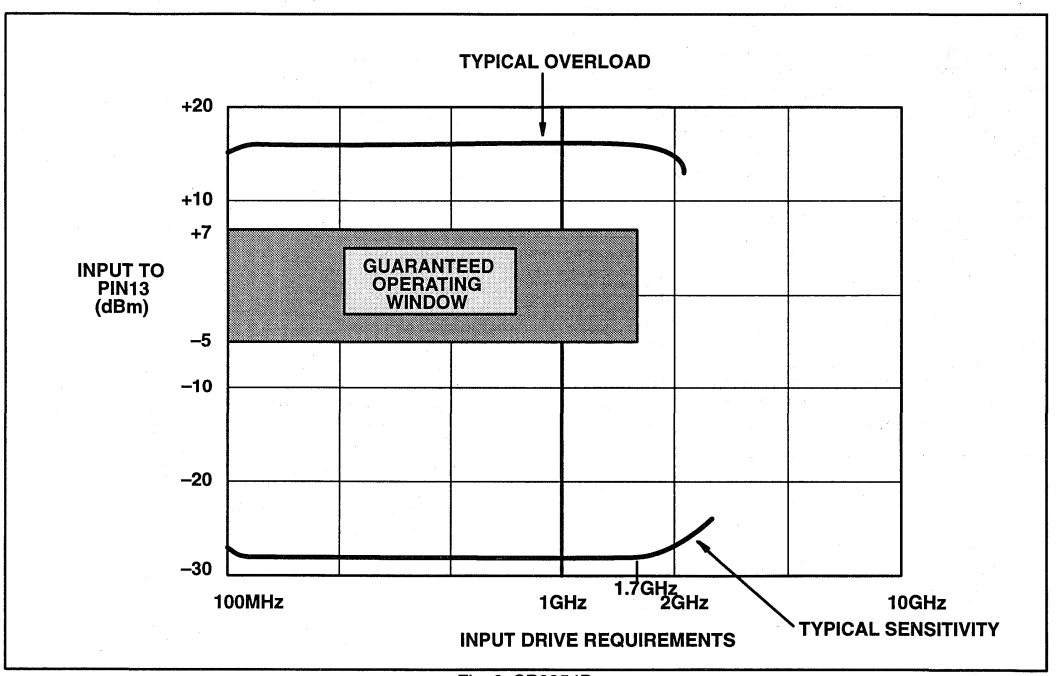
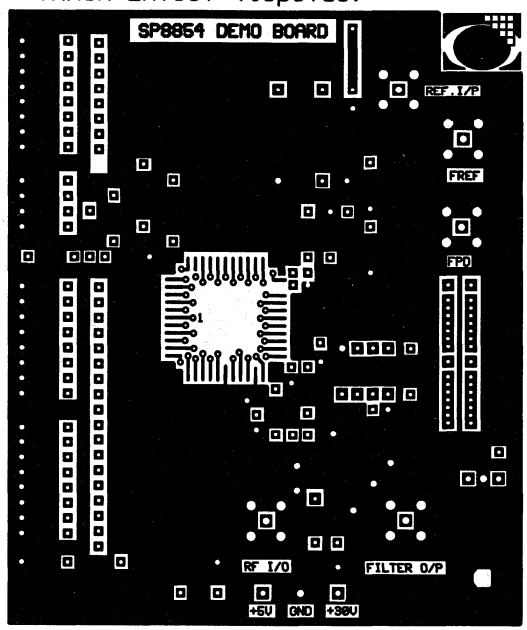


Fig. 8 SP8854D

TRACK LAYOUT (topside)



TRACK LAYOUT (underside)

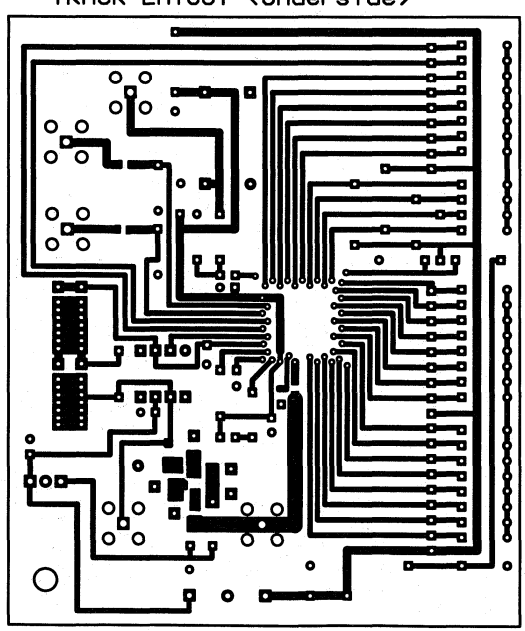


Fig. 9 P.C.B. layout

COMPONENT LAYOUT (topside)

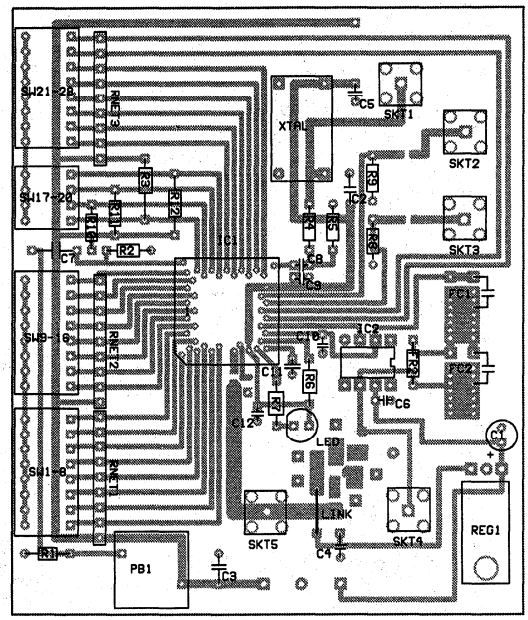


Fig. 10 Component layout

COMPONENT LAYOUT (underside)

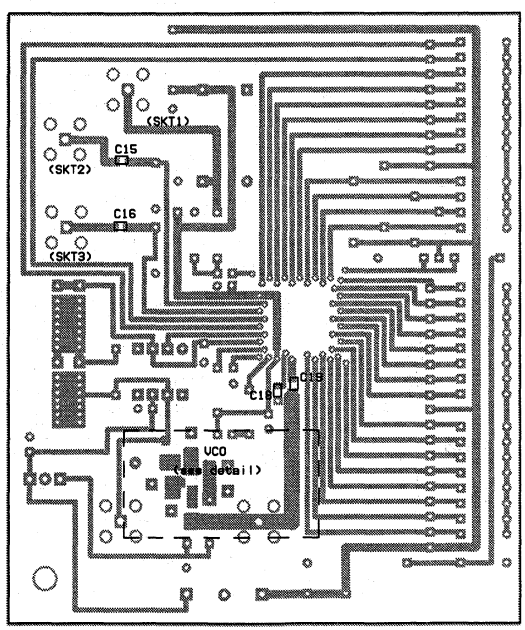


Fig. 11 Component layout

Component List.

C1	47µF	electrolytic
C2	10µF	tant
C3	1µF	tant
C4	1µF	tant
C5	100nF	ceramic
C6	100nF	ceramic
C7	22nF	polyester
C8	10nF	ceramic
C9	10nF	ceramic
C10	10nF	ceramic
C11	100pF	ceramic
C12	10nF	ceramic
C13	10nF	chip
C14	10nF	chip
C15	10nF	chip
C16	10nF	chip
C17	1nF	chip
C18	1nF	chip
C19	1nF	chip
C20	1.5pF	chip
C21	1.5pF	chip
C22	1.5pF	chip

R1	100K	
R2	2K7	
R3	10K	
R4	2K2	
R5	2K2	
R6	2K2	
R7	1K	
R8	1K	
R9	1K	
R10	10K	
R11	10K	
R12	10K	
R13	47K	chip
R14	10K	chip
R15	1K8	chip
R16	180R	chip
R17	50R	chip
RNET1	10K	
RNET2	10K	
RNET3	10K	

Note R13 to R17 are mounted on the underside of the board

Note C13 to C22 are mounted on the underside of the board.

IC1	SP8854D
IC2	OP–27G
REG1	L7812CP
TR1	AT–41486
VARICAP	BB405B
LED	5mm round

XTAL 40MHz crystal (optional)
SW1 to SW28 SPDT d.i.l toggle switches
PB1 pcb mount push button
SKT1 to SKT5 SMA pcb mount sockets
FC1, FC2 & FR2 are application dependent

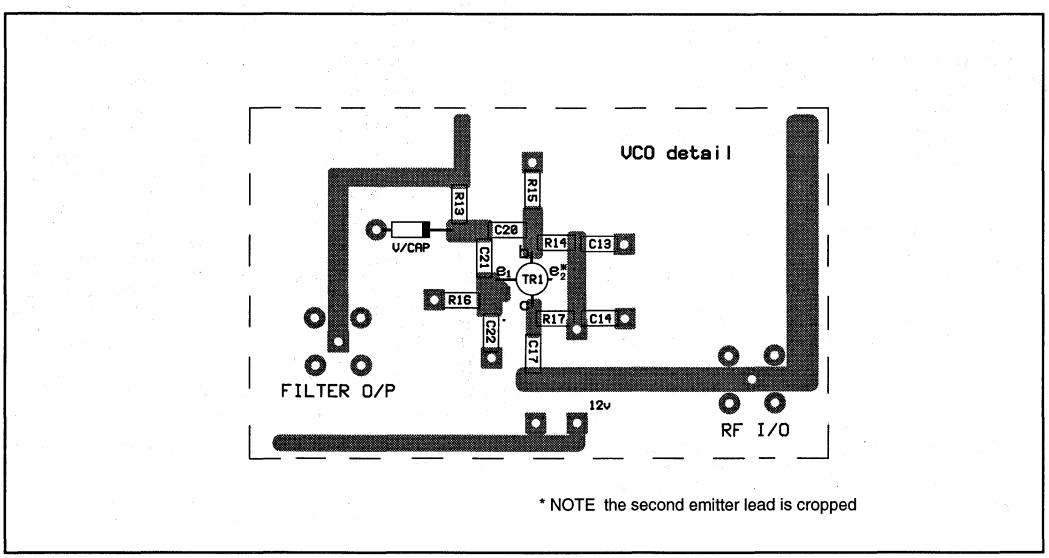


Fig. 12 VCO detail

SP8855D

1.7GHz PARALLEL LOAD PROFESSIONAL SYNTHESISER

The SP8855D is one of a family of parallel load synthesisers containing all the elements apart from the loop amplifier to fabricate a PLL synthesis loop. Other parts in the series are the SP8852D which is a fully programmable device requiring two 16 bit words to set the RF and reference counters, and the SP8854D which has hard wired reference counter programming and requires a single bit word to program the RF divider.

The SP8855D is intended for applications where a fixed synthesiser frequency is required although it can also be used where frequency selection is set by switches. In general the device will be programmed by connecting the programming pins to either V_{CC} or ground. Additional hard wired inputs can be used to control the F_{pd} and F_{ref} outputs, set the control direction of the loop and select the phase detector gain. Another input may be used to disable the phase detector output

FEATURES

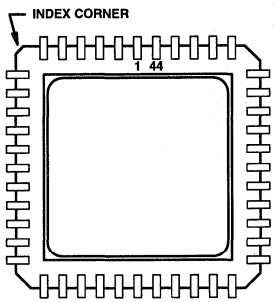
- 1.7GHz Operating Frequency
- Single 5V Supply Operation
- Low Power Consumption <1.3W
- High Comparison Frequency 50MHz
- High Gain Phase Detector 1mA/rad
- Programmable Phase Detector Gain
- Zero "Dead Band" Phase Detector
- Wide range of RF and Reference Divide Ratios
- Programming by Hard Wired Inputs

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	–0.3V to 6V
Storage Temperature	–65°C to+150°C
Operating Temperature	–55°C to+100°C
Prescaler & reference Input Voltage	2.5V p–p
Data Inputs	V_{CC} +0.3V
	V_{EE} –0.3V

ORDERING INFORMATION

SP8855D KG HCAR (non standard temperature range –55°C to +100°C standard product screening)
SP8855D IG HCAR (Industrial temperature range –40°C to +85°C standard product screening)



HC44

Pin	Description	Pin	Description
1	Input bus bit 10	23	Control Direction
2	Input bus bit 9	24	F_{pd}*
3	Input bus bit 8	25	F_{ref}*
4	Input bus bit 7	26	+5V
5	Input bus bit 6	27	Ref. osc capacitor
6	Input bus bit 5	28	Ref in/XTAL
7	Input bus bit 4	29	Reference bit 9
8	Input bus bit 3	30	Reference bit 8
9	Input bus bit 2	31	Reference bit 7
10	Input bus bit 1	32	Reference bit 6
11	Input bus bit 0	33	Reference bit 5
12	0V (prescaler)	34	Reference bit 4
13	RF input	35	Reference bit 3
14	RF input	36	Reference bit 2
15	V_{CC} +5V (prescaler)	37	Reference bit 1
16	V_{EE} 0V	38	Reference bit 0
17	Lock detect output	39	Phase Detect disable
18	C–lock detect	40	Phase Detect Gain 1.
19	R_{set}	41	Phase Detect Gain 0
20	Charge pump output	42	Input bus bit 13
21	Charge pump ref.	43	Input bus bit 12
22	F_{ref}/F_{pd} enable	44	Input bus bit 11

* F_{pd} and F_{ref} outputs are reversed using the Control Direction input. The table above is correct when pin 23 is high.

Fig. 1 Pin connections – top view

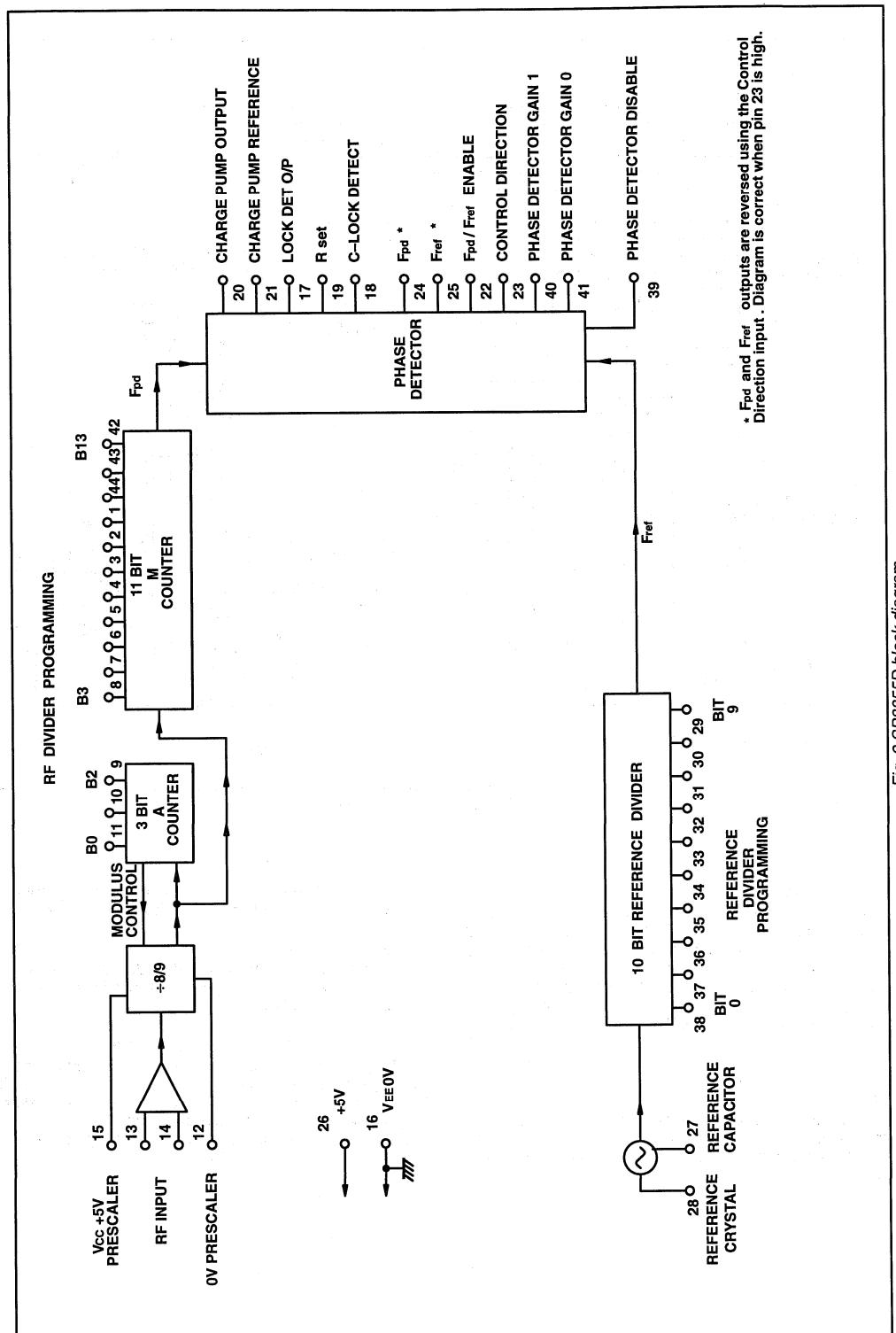


Fig. 2 SP8855D block diagram

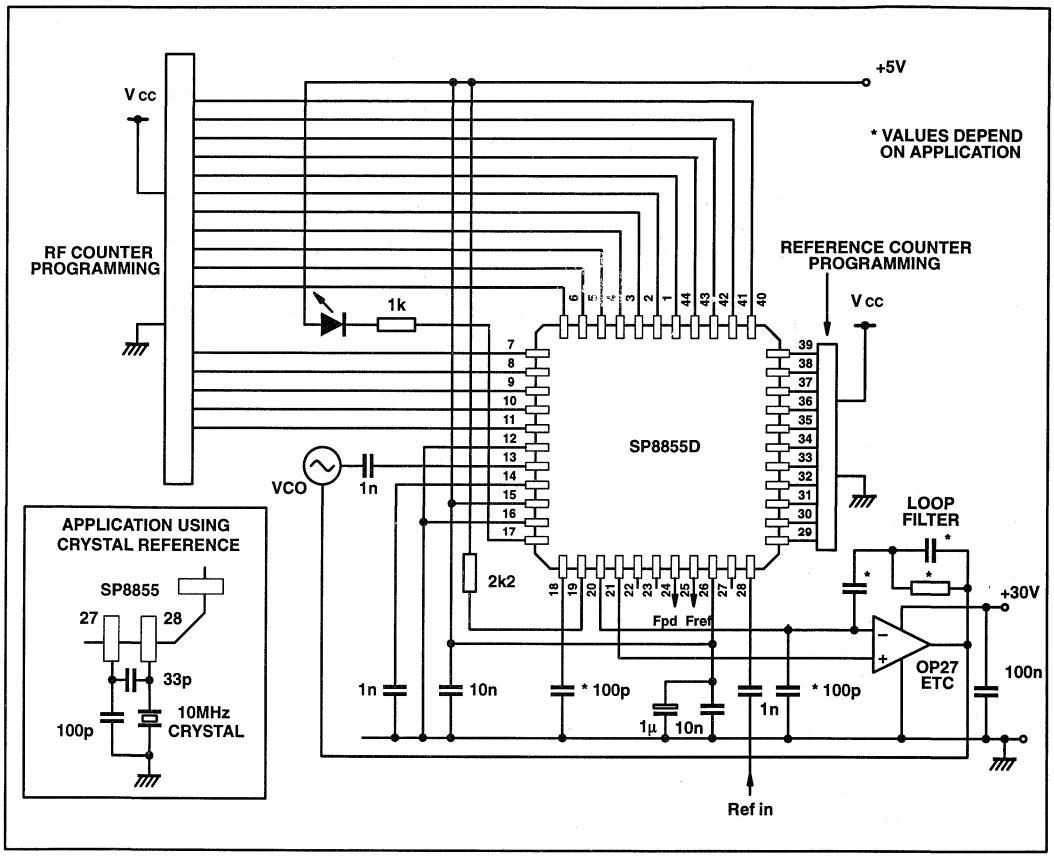


Fig. 3 Typical application diagram

DESCRIPTION

Prescaler and AM counter

The programmable divider chain is of A M counter construction and therefore contains a dual modulus front end prescaler, an A counter which controls the dual modulus ratio and an M counter which performs the bulk multi–modulus division. A programmable divider of this construction has a division ratio of MN+A and a minimum integer steppable division ratio of N(N–1), where N is the prescaler ratio.

Programming

The device is programmed by connecting the programming pins to either V_{CC} or ground. The programming inputs will go high if left open circuit but for best noise immunity a wired connection to V_{CC} is preferable. The programming inputs can be driven from TTL or CMOS logic levels if required.

Reference input

The reference source can be either driven from an external sine or square wave source of up to 100MHz or a crystal can be connected as shown in Fig. 3.

Phase Comparator and Charge pump

The SP8855D has a digital phase/frequency comparator driving a charge pump with programmable current output. The charge pump current level at the minimum gain setting is approximately equal to the current fed into the R_{set} input pin 19 and can be increased by programming pins 40 and 41 according to Table 1 by up to 4 times.

Pin 40	Pin 41	Current Multiplication Factor
0	0	1.0
0	1	1.5
1	0	2.5
1	1	4.0

Table 1

$$\text{Pin 19 current} = \frac{V_{cc} - 1.6V}{R_{set}}$$

$$\text{Phase detector gain} = \frac{I_{pin\ 19}(mA) \times \text{multiplication factor}}{2\pi}\ mA/\text{radian}$$

To allow for control direction changes introduced by the design of the PLL, pin 23 can be programmed to reverse the control direction of the loop by transposing the F_{pd} and F_{ref} connections. In order that any external phase detector will also be reversed by this function, the F_{pd} and F_{ref} outputs are also interchanged as shown in Table 2.

Output for RF Phase Lag	
Control direction pin 23	Pin 20
1	Current Source
0	Current Sink

Table 2

The F_{pd} and F_{ref} signals to the phase detector are available as ECL 10k levels on pin 24 and 25 and may be used to monitor the frequency input to the phase detector or used in conjunction with an external phase detector. When the F_{pd}/F_{ref} outputs are to be used at high frequencies, an external pull down resistor of minimum value 330Ω may be used connected to ground to reduce the fall time of the output pulse.

The charge pump connections to the loop amplifier consist of the charge pump output and the charge pump reference. The matching of the charge pump up and down currents will only be maintained if the charge pumps output is held at a voltage equal to the charge pump reference using an operational amplifier to produce a virtual earth condition at pin 20. Because the operational amplifiers will have limited response time compared with the pulse frequency at the charge pump output, pin 20 will not remain at the same voltage as pin 21 without an additional capacitor to ground to decouple the high frequencies. The value of capacitor required will vary with comparison frequency and the bandwidth of the op amp but a value between 50pF and 5nF will normally be required.

The lock detect circuit can drive an LED to give visual indication of phase lock or provide an indication to the control system if a pull up resistor is used in place of the LED. A small capacitor connected from the C–lock detector pin to ground may be used to delay lock detect indication and remove glitches produced by momentary phase coincidence during lock up. The phase detector can be disabled by pulling pin 39 to logic low.

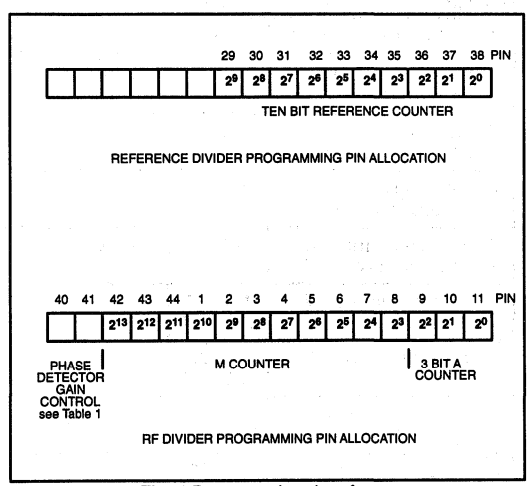


Fig. 4 Programming data format

ELECTRICAL CHARACTERISTICS

Guaranteed over the full temperature and supply voltage range (unless otherwise stated)
Temperature T_{amb} for KG parts –55°C and +100 °C
Temperature T_{amb} for IG parts –40°C and +85°
Supply Voltage = 4.75V and 5.25V

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	15, 26		180	240	mA	
RF input sensitivity	13, 14	–5.0		+7.0	dBm	100MHz to 1.7GHz See Fig. 8
RF division ratio	13,14,24	56		16383		
Reference division ratio	28, 25	1		1023		
Comparison frequency	28,24,25			50	MHz	
Reference input frequency	28	10		100	MHz	Reference division ratio ≥ 2 See Note 1
Reference input voltage	28	0	+6	+10	dBm	
F_{ref}/F_{pd} output voltage high	24, 25		–0.8		Vwrt V_{CC}	330Ω to 0V
F_{ref}/F_{pd} output voltage low	24, 25		–1.4		Vwrt V_{CC}	330Ω to 0V
Lock detect output voltage	17		300	500	mV	I_{OUT} = 3mA
Charge pump current at multiplication factor =1	19,20,21	±1.4	±1.5	±1.7	mA	$V_{pin\ 20} = V_{pin\ 21}$, $I_{pin\ 19}$ = 1.6mA
Charge pump current at multiplication factor =1.5	19,20,21	±2.0	±2.3	±2.5	mA	$V_{pin\ 20} = V_{pin\ 21}$, $I_{pin\ 19}$ = 1.6mA
Charge pump current at multiplication factor = 2.5	19,20,21	±3.4	±3.8	±4.6	mA	$V_{pin\ 20} = V_{pin\ 21}$, $I_{pin\ 19}$ = 1.6mA
Charge pump current at multiplication factor = 4.0	19,20,21	±5.4	±6.1	±6.5	mA	$V_{pin\ 20} = V_{pin\ 21}$, $I_{pin\ 19}$ = 1.6mA
Input bus high logic level	1–11,22 23,29–44	3.5			V	
Input bus low logic level	1–11,22, 23,29–44			1	V	
Input bus current source	1–11,22, 23,29–44	–200			µA	V_{IN} = 0V
Input bus current sink	1–11,22, 23,29–44			10	µA	$V_{IN} = V_{CC}$
Up down current matching	20			±2	%	$V_{pin\ 20} = V_{pin\ 21}$, $I_{pin\ 19}$ = 1.6mA
Charge pump reference voltage	21			V_{CC} – 0.5	V	$I_{pin\ 19}$ = 1.6mA current multiplication factor = 1
Charge pump reference voltage	21	V_{CC}–1.6			V	$I_{pin\ 19}$ = 1.6mA current multiplication factor = 4
R_{set} current	19	0.5		2	mA	See Note 2
R_{set} Voltage	19		1.6		V	$I_{pin\ 19}$ = 1.6 mA

Notes: 1. Lower reference frequencies may be used if slew rates are maintained.
2. Pin 19 current x multiplication factor must be less than 5mA if charge pump accuracy is to be maintained..

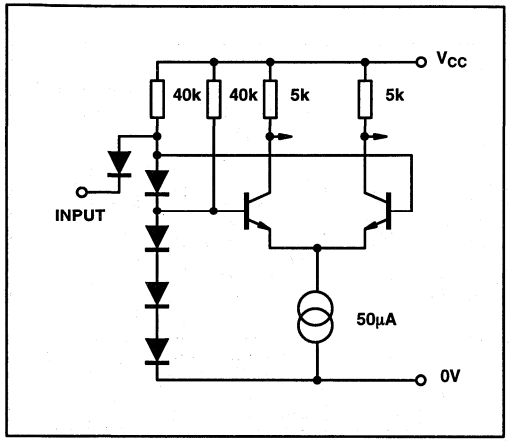


Fig. 5a RF and reference divider programming bits, F_{pd}/F_{ref} enable, control direction and phase detector gain control inputs

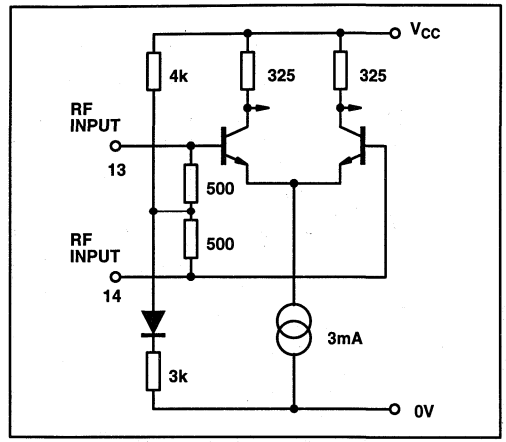


Fig. 5b RF inputs

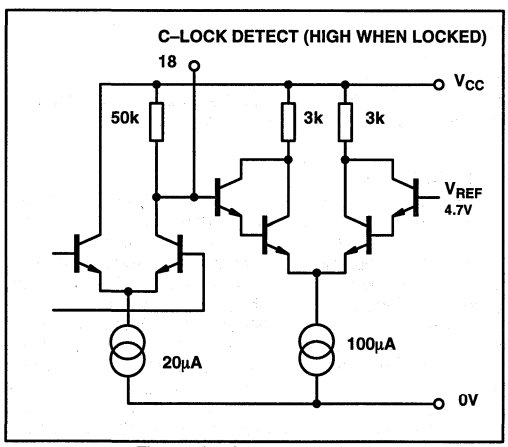


Fig. 5c Lock detect decouple

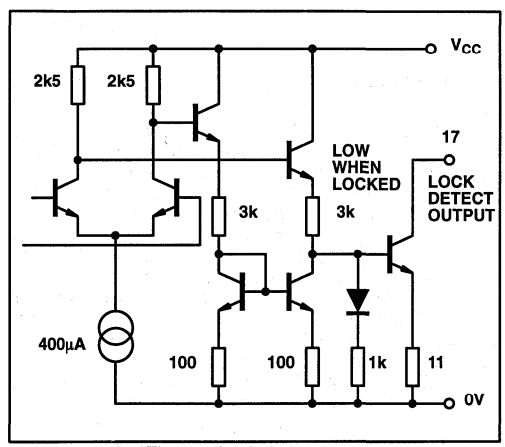


Fig. 5d Lock detect output

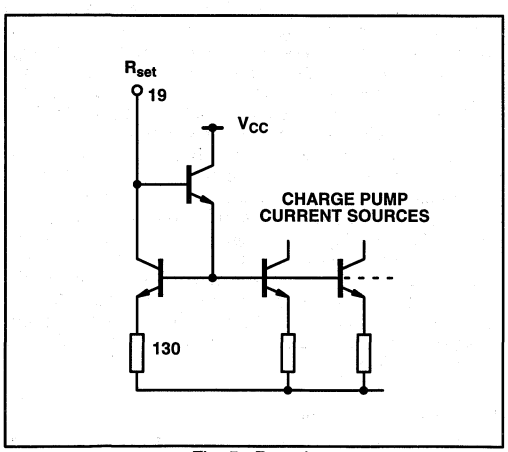


Fig. 5e R_{set} pin.

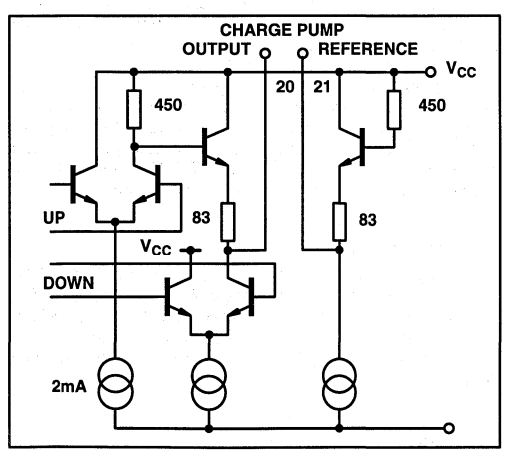


Fig. 5f Charge pump circuit

Fig. 5 Interface circuit diagrams

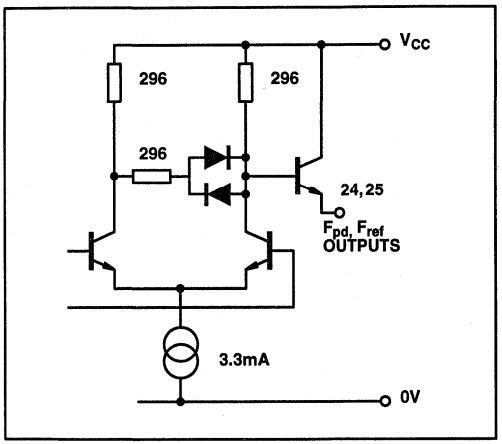


Fig. 5g F_{pd} and F_{ref} outputs

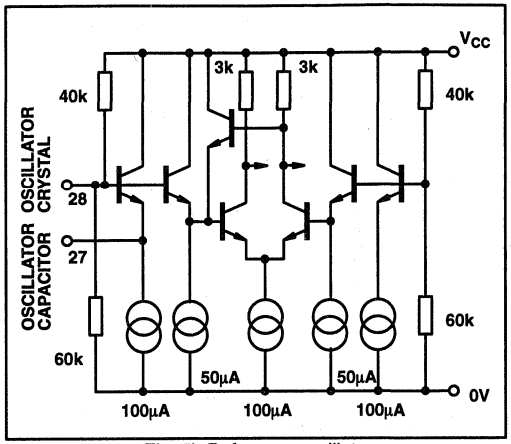


Fig. 5h Reference oscillator

Fig. 5 Interface circuit diagrams (cont)

APPLICATIONS

RF layout

The SP8855D can operate with input frequencies up to 1.7GHz but to obtain optimum performance, good RF layout practices should be used. A suitable layout technique is to use double sided printed board with through plated holes. Wherever possible the top surface on which the SP8855D is mounted should be left as a continuous sheet of copper to form a low impedance earth plane. The ground pins 12 and 16 should be connected directly to the earth plane. Pins such as V_{CC} and the unused RF input should be decoupled with chip capacitors mounted as close to the device pin as possible with a direct connection to the earth plane, suitable values are 10nF for the power supplies and 1nF for the RF input pin. A larger decoupling capacitor mounted as close as possible to pin 26 should be used to prevent modulation of V_{CC} by the charge pump pulses. The R_{set} resistor should also be mounted close to the R_{set} pin to prevent noise pickup, and the capacitor connected from the charge pump output should be a chip component with short connections to the SP8855D.

When the reference is derived from a crystal connected to pins 27 and 28 as shown in Fig. 3 the oscillator components are best mounted close to the SP8855D.

All signals such as the programming inputs, RF in, reference in and the connections to the op–amp are best taken through the pc board adjacent to the SP8855D with through plated holes allowing connections to remote points without fragmenting the earth plane. The GEC Plessey evaluation board shown in Fig.6 uses this layout technique.

Programming inputs

The input pins are designed to be compatible with TTL or CMOS logic with a switching threshold set at about 2.4V by three forward biased base emitter diodes. The inputs will be taken high by an internal pull up resistor if left open circuit but for best noise immunity it is better to connect unused inputs directly to V_{CC} or ground.

RF inputs

The prescaler has a differential input amplifer to improve input sensitivity. Generally the input drive will be single ended and the RF signal should be AC coupled to either of the inputs using a chip capacitor. The remaining input should be decoupled to ground, again using a chip capacitor. The inputs can be driven differentially but the input circuit should not provide a DC path between inputs or to ground.

Lock detect circuit

The lock detect circuit uses the up and down correction pulses from the phase detector to determine whether the loop is in or out of lock. When the loop is locked, both up and down pulses are very narrow compared to the reference frequency, but the pulse width in the out of lock condition continuously varies, depending on the phase difference between the outputs of the reference and RF counters. The logical AND of the up and down pulses is used to switch a 20mA current sink to pin 18 and a 50k resistor provides a load to V_{CC}. The circuit is shown in Fig. 5c. When lock is established, the narrow pulses from the phase detector ensure that the current source is off for the majority of the time and so pin 18 will be pulled high by the 50k resistor. A voltage comparator with a switching threshold at about 4.7V monitors the voltage at pin 18 and switches pin 17 low when pin 18 is more positive than the 4.7V threshold. When the loop is unlocked, the frequency difference at the counter outputs will produce a cyclic change in pulse width from the phase detector outputs with a frequency equal to the difference in frequency at the reference and RF counter outputs. A small capacitor connected to pin 18 prevents the indication of false phase lock conditions at pin 17 for momentary phase coincidence. Because of the variable width pulse nature of the signal at pin 18 the calculation of a suitable capacitor value is complex, but if an indication with a delay amounting to several times the expected lock up time is acceptable, the delay will be approximately equal to the time constant of the capacitor on pin 18 and the internal 50k resistor. If a faster indication is required, comparable with the loop lock up time, the capacitor will need to be 2–3 times smaller than the time constant calculation suggests. The time to respond to an out of lock condition is 2–3 times less than that required to indicate lock.

Charge pump circuit

The charge pump circuit converts the variable width up and down pulses from the phase detector into adjustable current pulses which can be directly connected to the loop amplifer. The magnitude of the current and therefore the phase detector gain can be modified when new frequency data is entered to

compensate for change in the VCO gain characteristic over its frequency band. The charge pump pulse current is determined by the current fed into pin 19 and is approximately equal to pin 19 current when the programmed multiplication ratio is one. The circuit diagram Fig. 5e shows the internal components on pin 19 which mirror the input current into the charge pump. The voltage at pin 19 will be approximately 1.6V above ground due to two V_{be} drops in the current mirror. this voltage will exhibit a negative temperature coefficient, causing the charge pump current to change with chip temperature by up to 10% over the full military temperature range if the current programming resistor is connected to V_{CC} as shown in the application diagram Fig. 3. In critical applications where this change in charge pump current would be too large the resistor to pin 19 could be increased in value and connected to a higher supply to reduce the effect of V_{be} variation on the current level. A suitable resistor connected to a 30V supply would reduce the variation in pin 19 current due to temperature to less than 1.5%. Alternatively a stable current source could be used to set pin 19 current.

The charge pump output on pin 20 will only produce symmetrical up and down currents if the voltage is equal to that on the voltage reference pin 21. In order to ensure that this voltage relationship is maintained, an operational amplifier must be used as shown in the typical application Fig. 3. Using this configuration pin 20 voltage will be forced to be equal to that on pin 21 since the operational amplifier differential input voltage will be no more than a few millivolts (the input offset voltage of the amplifier). When the synthesiser is first switched on or when a frequency outside the VCO range is programmed the amplifier output will limit, allowing pin 20 voltage to differ from that on pin 21. As soon as an achievable frequency value is programmed and the amplifier output starts to slew the correct voltage relationship between pin 20 and 21 will be restored. Because of the importance of voltage equality between the charge pump reference and output pins, a resistor should never be connected in series with the operational amplifier inverting input and pin 20 as is the case with a phase detector giving voltage outputs. Any current drawn from the charge pump reference pin should be limited to the few micro amps input current of a typical operational amplifier. A resistor between the charge pump reference and the non inverting input could be added to provide isolation but the value should not be so high that more than a few millivolts drop are produced by the amplifier input current.

When selecting a suitable amplifer for the loop filter, a number of parameters are important; input offset voltage in most designs is only a few milivolts and an offset of 5mV will produce a mismatch in the up and down currents of about 4% with the charge pump multiplication factor set at 1. The mismatch in up down currents caused by input offset voltage will be reduced in proportion to the charge pump multiplication factor in use. If the linearity of the phase detector about the normal phase locked operating point is critical, the input offset voltage of most amplifiers can be adjusted to near zero by means of a potentiometer.

The charge pump reference voltage on pin 21 is about 1.3V below the positive supply and will change with temperature and with the programmed charge pump multiplication factor. In many cases it is convenient to operate the amplifier with the negative power supply pin connected to 0V as this removes the need for an additional power supply. The amplifier selected must have a common mode range to within 3.4V (minimum charge pump reference voltage) of the negative supply pin to operate correctly without a negative supply. Most popular amplifiers can be operated from a 30V positive supply to give a wide VCO voltage drive range and have adequate common mode range to operate with inputs at +3.4V with respect to the negative supply. Input bias and offset current levels to most operational amplifiers are unlikely to be high enough to significantly affect the accuracy of the charge pump circuit currents but the bias current can be important in reducing reference side bands and local oscillator drift during frequency changes. When the loop is locked, the charge pump produces only very narrow pulses of sufficient width to make up for any charge lost from the loop filter components during the reference cycle. The charge lost will be due to leakage from the charge pump output pin and to the amplifier input bias current, the latter usually being more significant. The result of the lost charge is a sawtooth ripple on the VCO control line which frequency modulates the phase locked oscillator at the reference frequency and its harmonics.

It is possible to disable the charge pump by taking pin 39 low. In this case any leakage current will cause the oscillator to drift off frequency. This feature may be useful where having acheived lock an external phase detector of the user's choice can be employed to suit a specific application.

The necessity to maintain the charge pump output voltage at the same voltage as the reference pin has already been mentioned. This is important because the design of the positive current source has no voltage compliance and any departure from the reference voltage will introduce an error in the positive current source. The operational amplifier will maintain the DC charge pump voltage very close to the reference but the current from the charge pump is a series of pulses at the reference frequency. When the loop is locked the output pulses are very short in duration, the only current necessary being that required to restore and charge lost during the reference period. The virtual earth mechanism which maintains the charge pump output at the reference voltage depends on the amplifier having significant gain, but the narrow pulses from the charge pump are so short that the amplifier output will be unable to respond, allowing the input voltage to change and the pulse magnitude to be effectively reduced, introducing a non linearity in the phase detector characteristic at the phase locked point.

The capacitor shown connected from the charge pump output pin to ground on the typical application diagram Fig. 3 is intended to decouple the output at high frequencies, preventing voltage changes at the amplifier input which can not be corrected by the feedback response. The capacitor should be a high frequency type mounted close to the charge pump pin with short connection to the earth plane as the frequency content of the charge pump pulses extends to very high frequencies. A suitable value for this component is very difficult to calculate as its value depends on many factors including the bandwidth of the amplifier used in the loop filter and how critical the application is in terms of phase detector linearity. A value between 50pF and 5nF will suit most applications and the size of capacitor can be increased well beyond that necessary to restore linearity of the phase detector without ill effect. Many less critical applications will operate satisfactorily without this capacitor.

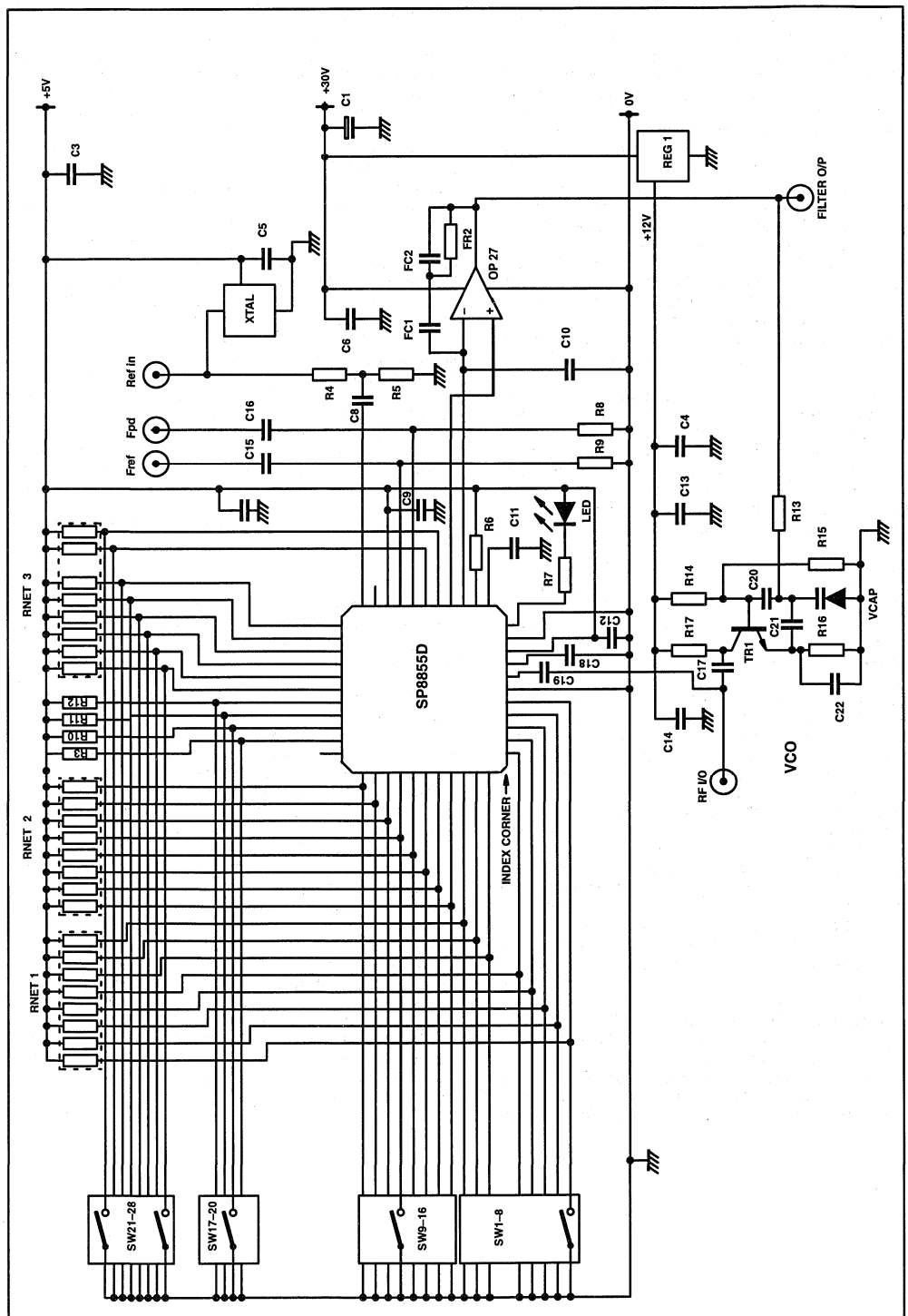


Fig. 6 Application board schematic

F_{pd} and F_{ref} outputs

These outputs provide access to the outputs from the RF and reference dividers and are provided for monitoring purposes during product development or test, and for connection of an external phase detector if required. the output circuit is of ECL type, the circuit diagram being shown in Fig.5g. The outputs can be enabled or disabled under software control by the address 0 control word but are best left in the disabled state when not required as the fast edge speeds on the output can increase the level of reference sidebands on the synthesised oscillator.

The emitter follower outputs have no internal pull down resistor to save current and if the outputs are required an external pull down resistor should be fitted.The value should be kept as high as possible to reduce supply current, about 2.2k being suitable for monitoring with a high impedance oscilloscope probe or for driving an AC coupled 50ohm load. A minimum value for the pull down resistor is 330ohms. When the F_{pd} and F_{ref} outputs are disabled the output level will be at the logic low level of about 3.5V so that the additional supply current due to the load resistors will be present even when the outputs are disabled.

Reference input

The reference input circuit functions as an input amplifier or crystal oscillator. When an external reference signal is used this is simply AC coupled to pin 28, the base of the input emitter follower. When a low phase noise synthesiser is required the reference signal is critical since any noise present here will be multiplied by the loop. To obtain the lowest possible phase noise from the SP8855D it is best to use the highest possible reference input frequency and to divide this down internally to obtain the required frequency at the phase detector. The amplitude of the reference input is also important, and a level close to the maximum will give the lowest noise. When the use of a low reference input frequency say 4–10MHz is essential some advantage may be gained by using a limiting amplifier such as a CMOS gate to square up the reference input.

In cases where a suitable reference signal is not available, it may be more convenient to use the input buffer as a crystal oscillator in this case the emitter follower input transistor is connected as a colpitts oscillator with the crystal connected from the base to ground and with the feedback necessary for oscillation provided by a capacitor tap at the emitter. The arrangement is shown inset in Fig. 3.

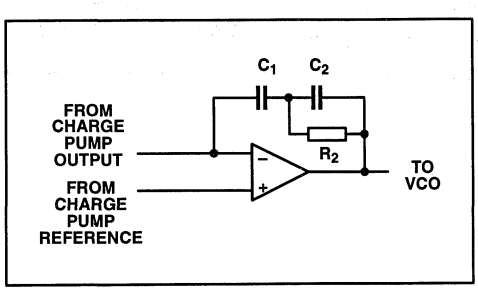


Fig. 7 Third order loop filter circuit diagram

Loop Filter Design

Generally the third order filter configuration shown in Fig.7 gives better results than the more commonly used second order because the reference sidebands are reduced. Three equations are required to determine values for the three constants where;

$$\tau_1 = C_1$$
$$\tau_2 = R_2 (C_1 + C_2)$$
$$\tau_3 = C_2 R_2$$

The equations are;

1 $$\tau_1 = \frac{K_\phi K_0}{N\omega_n^2}\left[\frac{1+\omega_n^2\tau_2^2}{1+\omega_n^2\tau_3^2}\right]^{1/2}$$

2 $$\tau_2 = \frac{1}{\omega_n^2\tau_3}$$

3 $$\tau_3 = \frac{-\tan\Phi_0 + \frac{1}{\cos\Phi_0}}{\omega_n}$$

Where;

- K_ϕ is the phase detector gain factor in mA/radian
- K_0 is the VCO gain factor in radian/second/Volt
- N is the total division ratio from VCO to reference frequency
- ω_n is the natural loop bandwidth
- Φ_0 is the phase margin normally set to 45°

Since the phase detector is linear over a range of 2π radian, K_ϕ can be calculated from

K_ϕ = Phase comparator current setting/2π mA/radian

These values can now be substituted in equation 1 to obtain a value for C_1 and equation 2 and 3 used to determine values for C_2 and R_2

EXAMPLE

Calculate values for a loop with the following parameters

Frequency to be synthesised:	1000MHz
Reference frequency	10MHz
Division ratio	1000MHz/10MHz = 100
ω_n natural loop frequency	100kHz
K_0 VCO gain factor	2π x 10MHz/Volt
Φ_0 phase margin	45°
Phase comparator current	6.3mA

The phase detector gain factor K_ϕ
= 6.3mA /2π = 1mA/radian

From equation 3:

$$\tau_3 = \frac{-\tan 45° + \frac{1}{\cos 45°}}{100\text{kHz} \times 2\pi} = \frac{0.4142}{628319}$$

$$\tau_3 = 659 \times 10^{-9}$$

From equation 2:

$$\tau_2 = \frac{1}{(100\text{kHz} \times 2\pi)^2 \times 659 \times 10^{-9}}$$

$$\tau_2 = 3.844 \times 10^{-6}$$

Using these values in equation 1:

$$\tau_1 = \frac{1 \times 10^{-3} \times 2\pi \times 10\text{MHz/V}}{100 \times (2\pi \times 100\text{kHz})^2}\ [A]^{1/2}$$

Where A is :

$$\frac{1 + \omega_n^2 \tau_2^2}{1 + \omega_n^2 \tau_3^2} = \frac{1 + (2\pi \times 100\text{kHz})^2 \times (3.844 \times 10^{-6})^2}{1 + (2\pi \times 100\text{kHz})^2 \times (659 \times 10^{-9})^2}$$

$$\tau_1 = \frac{62832}{39.48 \times 10^{12}} \left[\frac{6.833}{1.1714}\right]^{1/2}$$

$$\tau_1 = 1.59 \times 10^{-9} \times 2.415$$

$$\tau_1 = 3.84 \times 10^{-9}$$

Now $\tau_1 = C_1 \therefore C_1 = 3.84\text{nF}$

$\tau_2 = R_2 (C_1 + C_2)$

$\tau_3 = C_2 R_2$

Substituting for C_2

$$\tau_2 = R_2\left[C_1 + \frac{\tau_3}{R_2}\right] \quad \therefore \tau_2 = R_2 C_1 + \tau_3$$

$$\therefore R_2 = \frac{\tau_2 - \tau_3}{C_1} = \frac{3.844 \times 10^{-6} - 659 \times 10^{-9}}{9.61 \times 10^{-9}}$$

$R_2 = 829.4\Omega$

$$\tau_3 = C_2 R_2 \therefore C_2 = \frac{\tau_3}{R_2} = \frac{659 \times 10^{-9}}{829.4}$$

$C_2 = 0.794\text{nF}$

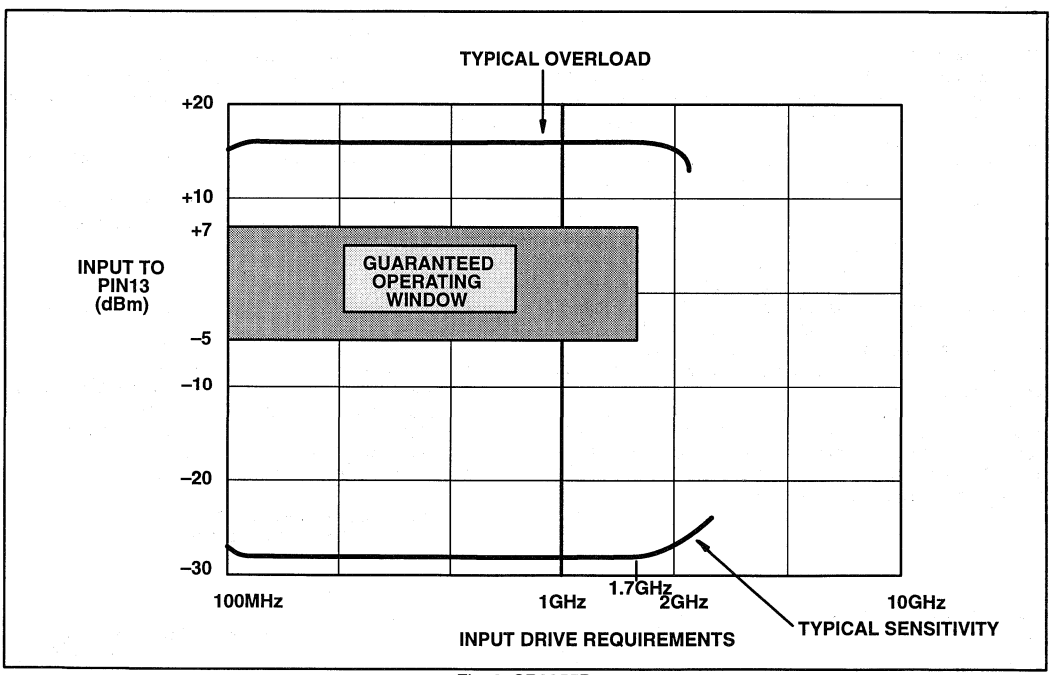
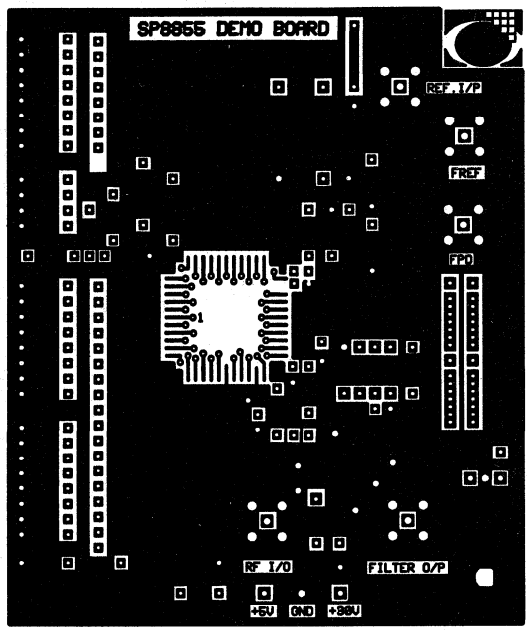


Fig. 8 SP8855D

TRACK LAYOUT (topside)



TRACK LAYOUT (underside)

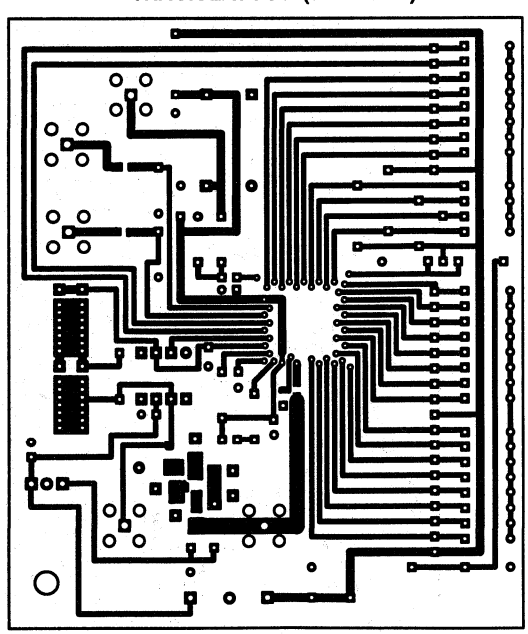


Fig. 9 P.C.B. layout

COMPONENT LAYOUT (topside)

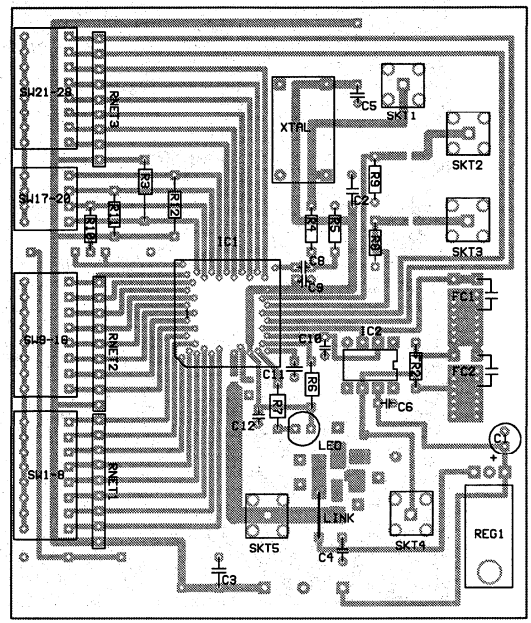


Fig.10 component layout.

COMPONENT LAYOUT (underside)

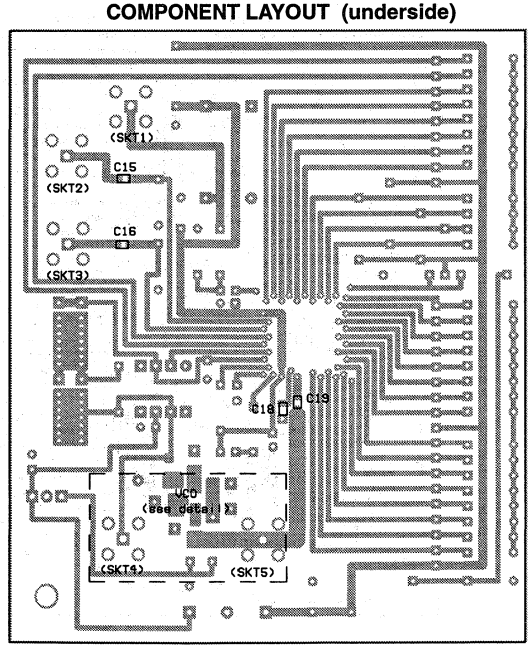


Fig.11 component layout.

Component List.

C1	47µF	electrolytic
C2	10µF	tant
C3	1µF	tant
C4	1µF	tant
C5	100nF	ceramic
C6	100nF	ceramic
C7	N/U	
C8	10nF	ceramic
C9	10nF	ceramic
C10	10nF	ceramic
C11	100pF	ceramic
C12	10nF	ceramic
C13	10nF	chip
C14	10nF	chip
C15	10nF	chip
C16	10nF	chip
C17	1nF	chip
C18	1nF	chip
C19	1nF	chip
C20	1.5pF	chip
C21	1.5pF	chip
C22	1.5pF	chip

R1	N/U	
R2	N/U	
R3	10K	
R4	2K2	
R5	2K2	
R6	2K2	
R7	1K	
R8	1K	
R9	1K	
R10	10K	
R11	10K	
R12	10K	
R13	47K	chip
R14	10K	chip
R15	1K8	chip
R16	180R	chip
R17	50R	chip
RNET1	10K	
RNET2	10K	
RNET3	10K	

Note R13 to R17 are mounted on the underside of the board

Note C13 to C22 are mounted on the underside of the board.

IC1	SP8855D
IC2	OP–27G
REG1	L7812CP
TR1	AT–41486
VARICAP	BB405B
LED	5mm round

XTAL	40MHz crystal (optional)
SW1 to SW28	SPDT d.i.l toggle switches
SKT1 to SKT5	SMA pcb mount sockets
FC1, FC2 & FR2	are application dependant

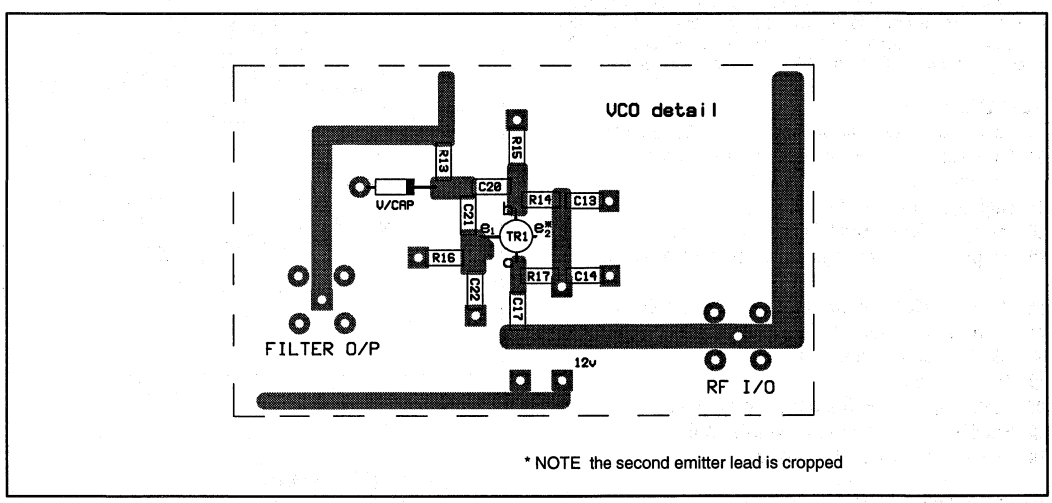


Fig. 12 VCO detail

SP8858

1.5GHz PROFESSIONAL SYNTHESISER

The SP8858 is a single chip synthesiser intended for PLL signal synthesis applications up to 1.5GHz and includes a dual modulus prescaler, programmable A, M and R dividers, digital phase detector, charge pump and lock detect circuits.

The SP8858 is a development of the SP8853 synthesiser with reduced noise floor, increased dynamic range above 1GHz and an improved, high gain, phase detector design that eliminates the dead–band. The improvements are at the expense of an increase in power consumption.

The low prescaler modulus, programmable to either 16/17 or 8/9, together with the 15 bit M counter and 13 bit reference counter make this device ideal for a diverse range of high performance applications.

The nominal phase detector gain is set by an external resistor and the gain can be varied over a 4:1 range when the device is programmed. The dividers, the phase detector sense, the prescaler modulus and the data buffer control logic are also programmable using the three wire serial interface. An alternative 22 bit control word for the A/M dividers and phase detector gain can be stored so allowing fast frequency hopping and bandwidth switching by simply toggling the logic level on pin 13 (F1/F2). In addition, the A counter of the "active" buffer can be programmed with only 6 bits allowing fast hopping to adjacent channels.

A simple exclusive–or lock detect circuit is also provided, the sensitivity of which is determined by an external capacitor.

This part is specified to 1.5GHz at +125°C in the DG package and to 1.3GHz at +125°C in the HC package.

FEATURES

- Low phase noise floor typically <–150dBc/Hz
- Operation to 1.5GHz over full operataing temperature
- High input sensitivity
- Improved linear digital phase detector
- Programmable charge pump current: 10μA to 2mA
- On–chip 16/17 or 8/9 dual modulus prescaler
- Three wire serial data interface
- 13 bit reference counter
- 15 bit M counter
- Stores an alternative programming word
- Facility to programme A counter only
- Power saving standby mode

ABSOLUTE MAXIMUM RATINGS

Supply voltage	–0.3V to 7V
Storage temperature	–65°C to +150°C
Operating temperature	–55°C to 125°C
Prescaler input voltage	2.5V p–p

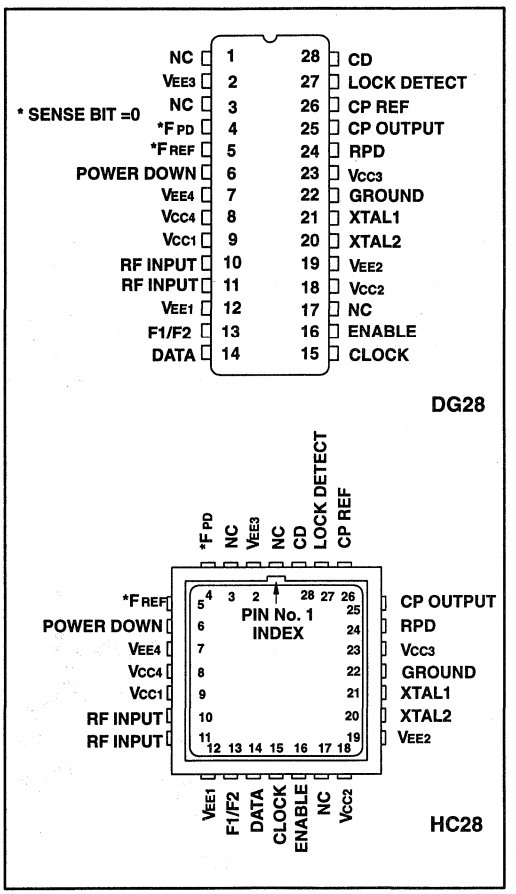


Fig. 1 pin connections – top view

ORDERING INFORMATION

SP8858 IG DGAS (–40 to +85°C)
SP8858 IG HCAR (–40 to +85°C)
SP8858 MG DGAS (–55 to +125°C)
SP8858 MG HCAR (–55 to +125°C)

PIN DESCRIPTION	
Pin 4 (F_{pd}*)	M divider output pulses F_{pd} = RF input frequency (pins 10 and 11) / (M.N + A)
Pin 5 (F_{ref}*)	R divider output pulses F_{ref} = Reference input frequency (pin 20) / R
	* These pins are reversed when the SENSE bit is set to 1 (see Data Entry and Control description)
Pin 6 (POWER DOWN)	With this pin held high the device is in the power saving standby mode. The serial interface shift register and data buffers remain active at all times so that the device can still be programmed in this mode.
Pins 10 and 11 (RF INPUT)	Balanced inputs to the RF preamplifier. For single ended operation the signal is AC coupled into pin 11 with pin 10 decoupled to ground or vice–versa.
Pin 13 (F1/F2)	The logic level on this input determines which of the two words stored in the internal buffers is used to reload the A and M dividers at the end of the count cycle. With F1/F2 high the F1 buffer is selected.
Pin 14 (DATA)	Serial data on this line is clocked into a shift register under control of clock and enable.
Pin 15 (CLOCK)	Clocks the data into the shift register. Maximum clock frequency is 1MHz.
Pin 16 (ENABLE)	Logic high on this pin allows data to be clocked into the shift register and the subsequent falling edge loads the buffer chosen by the LSBs of the programmed word. The clock input is ignored when enable is low.
PIN 20 (XTAL2)	This pin is the input to a buffer amplifier if an external reference signal is provided. Alternatively, the amplifier provides the active element for a reference oscillator if a quartz crystal is connected at this point (see Applications)
PIN 21 (XTAL1)	Leave open circuit if an external reference is used or connect load capacitors for the chosen crystal (see Applications)
Pin 24 (RPD)	An external resistor connected between this pin and V_{CC} sets the Charge Pump output current. A multiplication factor can also be programmed into the device (see table 1)
PIN 25 (CP output)	The phase detector output is a single–ended charge pump sourcing or sinking current to the inverting input of an external loop filter
PIN 26 (CP Ref)	Connected to the non–inverting input of the loop filter to set the dc bias
PIN 27 (Lock Detect)	A current sink into this pin is enabled when the lock detect circuit indicates lock. Used to give external indication of phase lock
PIN 28 (Cd)	A capacitor connected to this point determines the lock detect integrator time constant and can be used to vary the sensitivity of the phase lock indicator

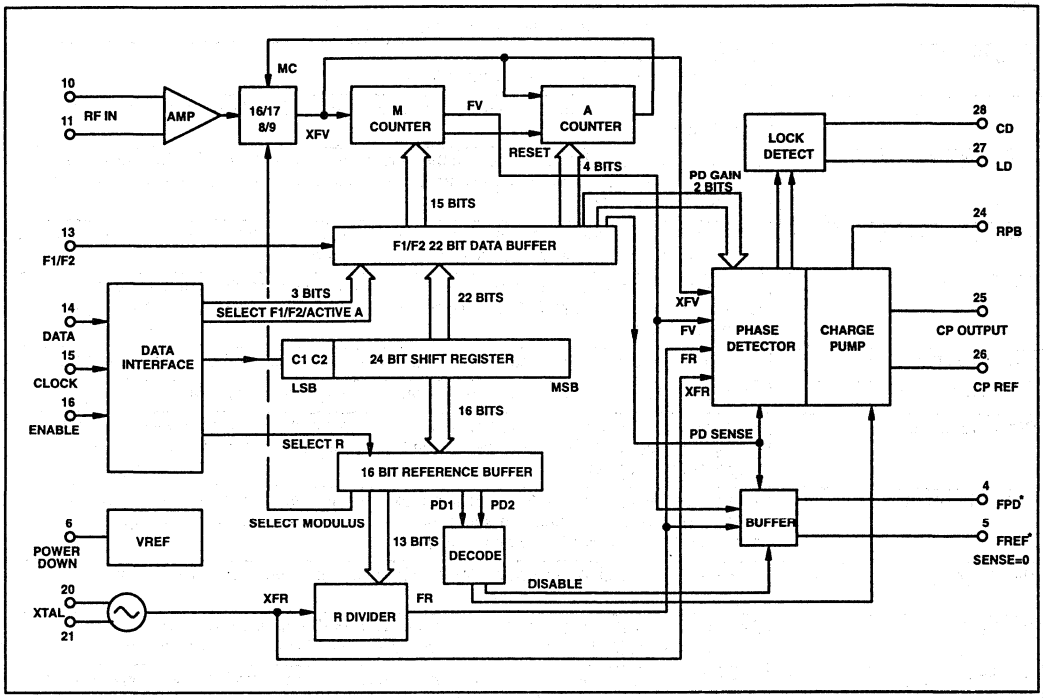


Fig. 2 SP8858 block diagram

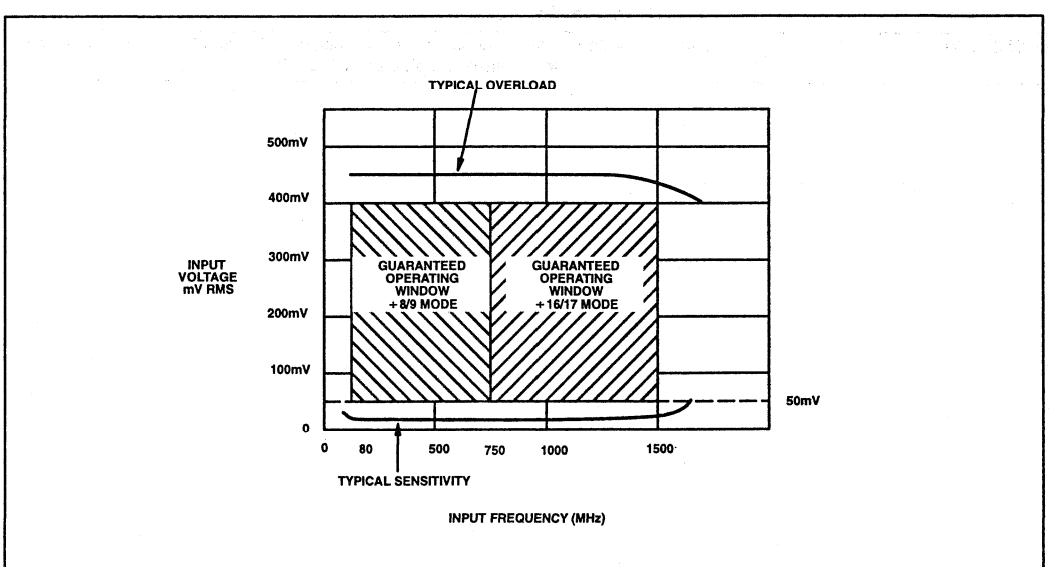


Fig. 3a typical input characteristics and input drive requirements (DG package)

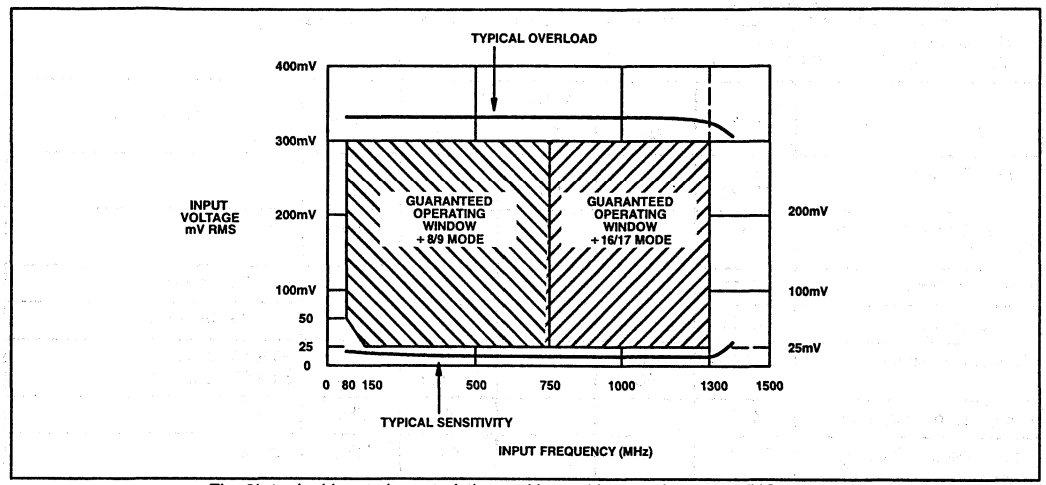


Fig. 3b typical input characteristics and input drive requirements (HC package)

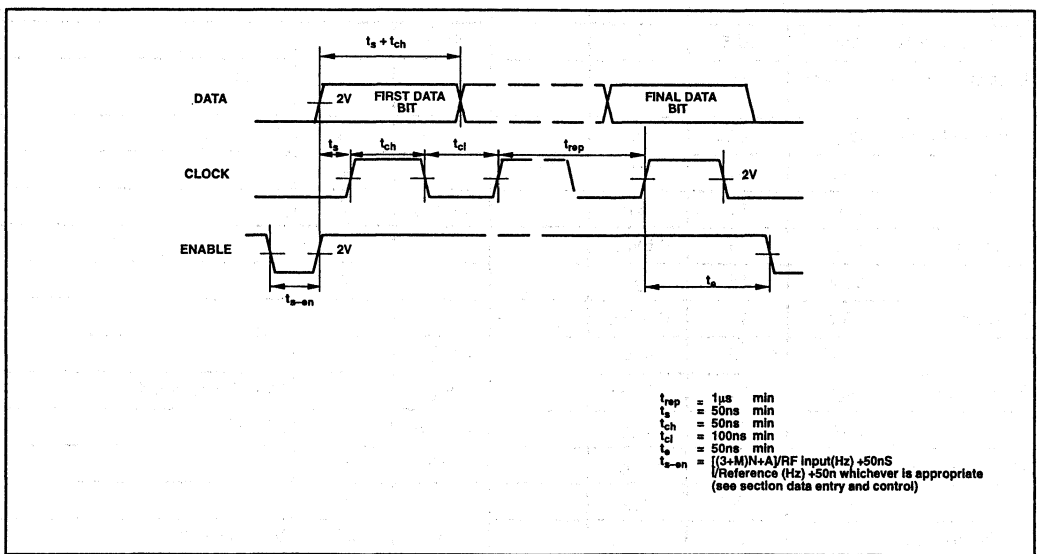


Fig. 4 Data and clock timing requirements

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated).
Supply voltage V_{CC}+4.75 to +5.25V
Temperature T_{amb} = −55°C to +125°C

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply Current	8, 9 18, 23		100		mA	
Supply Current in Power Down Mode	8		45		mA	
Input Sensitivity	10, 11					See Fig. 4a and b.
Input overload	10, 11					See Fig. 4a and b
RF Input Division Ratio	10, 11, 4	240 56		524287 262143		With 16/17 selected With 8/9 selected
Comparison Frequency	4, 5			5	MHz	
Reference Oscillator Input Frequency	20, 21	4		40	MHz	See note 1
External Reference Input Voltage	20	10		500	mVrms	
Reference Division Ratio	20.5	1		8191		
Data Clock Repetition Rate t_{rep}	15			1	µs	See Fig. 4
Minimum Set up Time t_s	14, 15	50			ns	See Fig. 4
Data Input High	14	$0.6V_{CC}$		V_{CC}	V	
Low	14	V_{EE}		$0.3V_{CC}$	V	
Clock Input High	15	$0.6V_{CC}$			V	
Low	15	V_{EE}		$0.3V_{CC}$	V	
Data Enable High	16	$0.6V_{CC}$		V_{CC}	V	
Low	16	V_{EE}		$0.3V_{CC}$	V	
F1/F2 Input High	13	$0.6V_{CC}$		V_{cc}	V	F1 buffer selected
Low	13	V_{EE}		$0.3V_{CC}$	V	F2 buffer selected
Power Down Input High	6	$0.6V_{CC}$		$0.9V_{CC}$	V	
Low	6	V_{EE}		$0.3V_{CC}$	V	
F1/F2 Input Current	13			5	µA	V Pin 13=5.0V
Power Down Input Current	6			5	µA	V Pin 6=4.5V
RPD External Resistance	24	7		330	KOhms	
Lock Detect Output Voltage "in lock"	27			1	V	I pin 27<3mA
F_{pd} and F_{ref} Output Voltage Swing			0.9		V	V_{CC}=5V. External pull down may be required
Lock Detect Time Constant Resistor	27		50K		Ohms	

Note 1: The reference frequency range when using a crystal oscillator is 4–20MHz

DESCRIPTION

Prescaler and Dividers

The block diagram of a dual modulus divider arrangement is shown in Fig. 5. The N/N+1 prescaler, together with the A and M dividers, divide the RF input frequency down to the comparison frequency at the phase detector input. The comparison frequency sets the resolution of a single loop synthesiser; when A is incremented (or decremented) by one, the loop output frequency automatically increments (or decrements) by the comparison frequency. When the dividers are reset, at the end of the each count cycle, the modulus of the prescaler is set to N+1 and the input frequency to the A and M dividers is then RFinput/(N+1) Hz. The output of the A counter controls the prescaler modulus, which is set to N when A reaches its programmed value. The M divider continues to count at the rate RFinput/N until it reaches its programmed value at which point the dividers are reset and the count cycle starts again. The division ratio of this arrangement is therefore

$$A.(N+1) + (M-A).N = M.N + A$$

It is evident that for this arrangement to work M must always be programmed greater than or equal to A and A must be able to count to N–1. These restrictions set a minimum count of N^2-N; below this value some division ratios will not be available.

The SP8858 prescaler can be set to 8/9 or 16/17 mode by setting the appropriate bit of the reference word. The A divider is a 4bit counter, whilst the M divider is a 15bit counter. The minimum division ratio, with the 8/9 prescaler, is $8^2-8 = 56$, whilst the maximum division ratio, with the 16/17 prescaler, is 16. $(2^{15}-1) + (2^4-1) = 524287$.

If the 8/9 prescaler is used the MSB of the A counter must be programmed to 0.

Reference Source and Divider

The reference source in the SP8858 is obtained from an on chip oscillator, stabilised by an external quartz crystal. The oscillator circuit will also function as a buffer amplifier if an external reference is preferred. In the latter case the signal, should be ac coupled into pin 20.(See Applications)

The reference oscillator drives a divider stage, the output of which is the reference signal to the phase comparator. The PLL controls the input voltage to an external VCO so that the divided VCO signal is phased locked to this reference signal. The dynamics of the control loop are determined by the external loop filter.

The 13bit reference divider is fully programmable and can be set to any ratio between 1 and 8191. The programmed word is stored in the internal reference buffer.

Phase Comparator and Charge Pump

The digital phase detector is sensitive to frequency and phase errors. The basic circuit for a conventional digital phase/frequency detector is based on two D type flip flops. Initially the flip flops are reset, each one is then set by the respective pulses of the divider outputs. When both flip flops have been set they are immediately reset. In this way the output of one flip flop is a pulse whose width is proportional to phase difference, whilst the second flip flop is a narrow pulse determined by the time to reset. The phase detector outputs drive a charge pump amplifier. One output controls a constant current source, the other an identical current sink connected to the same node (CP output pin 25). The SP8858 phase/frequency detector has been modified and improved to provide a linear characteristic, thus eliminating deadband effects.

The phase detector gain is determined by the output current from the charge pump ($\pm$Iout A). An external transimpedance amplifier is required to provide the voltage drive to the VCO. This requirement is usually performed by the loop filter operational amplifier which is designed to provide a type II third order control loop (see Applications).

The nominal charge pump output current is set by an external resistor connected between pin 24 and the supply rail. This current can be multiplied by up to four times by programming bits G1 and G2 as shown in Table 1. The maximum charge pump output current is $\pm$ 2mA.

Ipin 24=(V_{CC}–1.5)/RPD.

Iout=G.Ipin 24

Gain = Iout /2π A/rad.

G2	G1	Multiplier G
0	0	1
1	0	1.5
0	1	2.5
1	1	4

Table 1

Data Entry and Control

The SP8858 is programmed using the serial data interface. Data is entered into the chip on the DATA pin and clocked into the internal shift register by the positive going edge of the CLOCK signal with the Enable pin held high. Whilst the ENABLE pin is high, changes to the shift register will not affect the current count cycle. On the falling edge of ENABLE the data held in the shift register is transferred to one of the three buffers (F1, F2 or reference). Fig. 4 shows the timing requirements for these three signals.

The 2 LSBs of the 24 bit shift register, C1 and C2, determine which of the three buffers is loaded with the data held in the remaining 22bits as shown in Table 2.

C2	C1	Buffer Loaded
0	0	F1
1	0	F2
0	1	Active A*
1	1	Reference

Table 2

* Only the A divider of the active buffer is changed

If the F1 buffer (C2=0, C1=0) is selected the 22MSBs of the shift register are transferred to it. 19bits of the buffer provide the data for the A and M dividers. The three remaining bits control the charge pump current multiplication factor as shown in Table 1 and the sense of the phase detector. The F2 buffer performs the same function so that an alternative divider word and/or phase detector gain can be stored.

When the sense bit is set to 1 the inputs and clocks to the phase detector flip flops are reversed. The bit should be set to 1 for a VCO with a positive frequency vs voltage characteristic. The sense bit also swops the outputs F_{ref} and F_{pd} on pins 4 and 5. Fig. 1 shows the pin out for sense = 0.

The active buffer, i.e. the one that is currently used to update the dividers, is selected at pin 13 (F1/F2). An high on this pin selects F1. The F2 word can be updated whilst F1 is controlling the dividers without disrupting the loop (and vice versa). This facility can be used to reduce synthesiser switching time by preparing the non–active buffer prior to the instant of switching and can also be used to modify the open loop gain.

To ensure reliable data is loaded into the dividers the internal control circuits ensure that the buffer data can only be updated if the remaining M count is greater than 3. Given this restriction, the maximum time taken to update the buffer after

the negative going ENABLE transition (or after F1/F2 has been toggled) is:

Max. buffer update time (Sec) = ((3+M) N+A)/RF input (Hz) +50nS

Time taken to reprogramme the shift register is determined by the clock rate and the number of bits required:

Programming time (F1 or F2) = $24.t_{rep} + t_s + t_e$ (see Fig. 4).

If the reference buffer is selected (C2=1,C1=1) only the 16LSBs of the shift register are used. 13bits provide the data for the Reference divider. Two bits, PD1 and PD2, control the charge pump and the divider output buffer as shown in table 3:

PD2	PD1	
0	0	F_{ref} and F_{pd} outputs off, charge pump on
0	1	F_{ref} and F_{pd} outputs on, charge pump on
1	0	F_{ref} and F_{pd} outputs on, charge pump off
1	1	F_{ref} and F_{pd} outputs on, charge pump disabled by lock detect

Table 3

The remaining bit of the Reference word is used to select the prescaler modulus. A 1 in this position selects the 8/9 mode. Note that when the 8/9 mode is selected the A divider only requires 3bits – the 4th bit must be set to 0.

To ensure reliable data is loaded into the dividers the internal control circuits ensure that the buffer data can only be updated if the remaining R count is greater than 1. Given this restriction, the maximum time taken to update the buffer after the negative going ENABLE transition (or after F1/F2 has been toggled) is:

Max. buffer update time(Sec) = $1/F_{ref}$+50nS

Only 16bits are required to programme the reference buffer, therefore programming time (Reference)=$16.t_{rep}+t_s+t_e$ (see fig. 4)

If the Active A mode is programmed (C2=0. C1=1) only the 4 A divider bits of the active buffer are updated at the end of the M count. The M divider data, multiplication factor and phase detector sense remain unchanged.

This can be used to frequency hop to an adjacent channel with the programming time reduced to :

Programming time (Active A)=$6.t_{rep}+t_s+t_e$

The programming details discussed above are summarised in Fig. 6.

Lock Detect

A simple EXCLUSIVE OR phase detector together with an integrator and comparator are used to indicate phase lock.

A capacitor on pin 28 sets the integrator time constant and hence the sensitivity of the lock detect function. The comparator controls a current sink connected to pin 27 which can be used together with an external LED or resistor to indicate phase lock.

The lock detect can also be used to disable the charge pump by programming PD1 and PD2 of the reference word (Table 3).

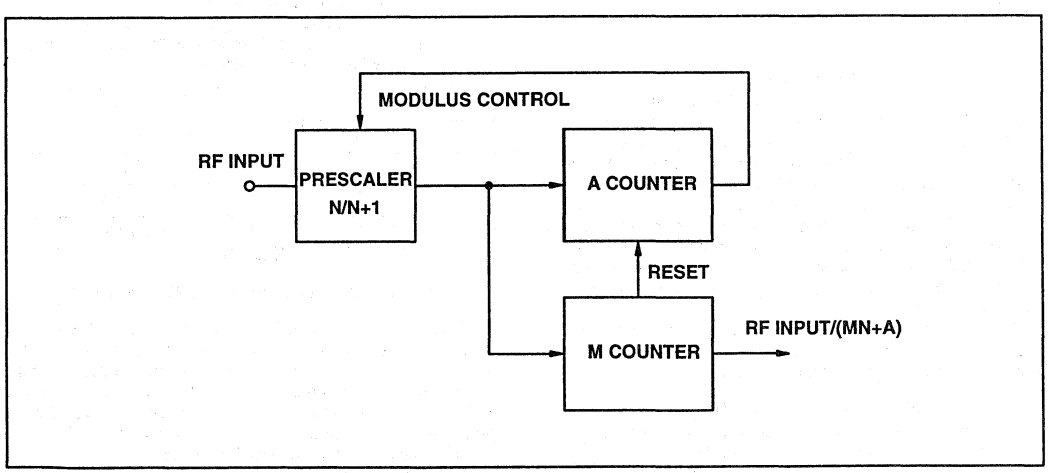


Fig. 5

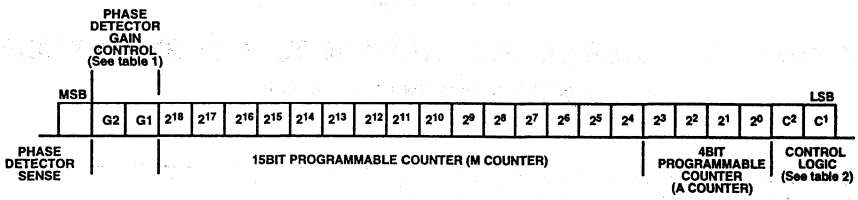


Fig. 6 (a) F1 or F2 word bit allocation with 16/17 selected

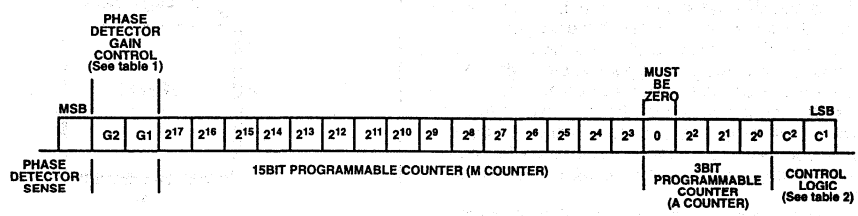


Fig. 6 (b) F1 or F2 word bit allocation with 8/9 selected

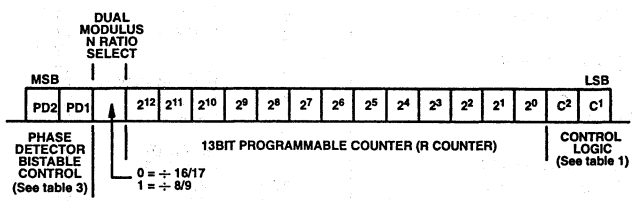


Fig. 6 (c) reference word bit allocation

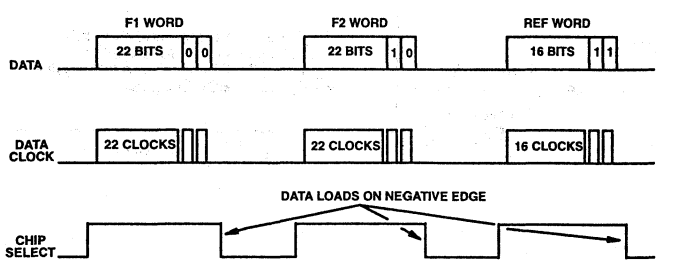


Fig. 6 (d) typical data load sequence

Fig. 6 Data format diagrams

SP8861

1.3GHz LOW POWER SINGLE–CHIP FREQUENCY SYNTHESISER

(Supersedes September 1990 Edition)

The SP8861 is a low power single chip synthesiser intended for professional radio applications, and contains all the elements (apart from the loop amplifier) to fabricate a PLL frequency synthesis loop.

The device is serially programmable by a three wire data highway and contains three independent buffers to store one reference divider word and two local oscillator divider words. A digital comparator, with two charge pumps, programmable in phase gain are provided to improve lock up performance. the preset tandem operation of the charge pumps can be overwritten or the comparison frequencies switched to output ports under control of the divider word. The dual modulus ratio and so operating range is also programmable through the same word.

A power down mode is incorporated as a battery economy feature.

FEATURES

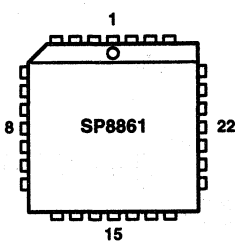
- Improved Digital Phase Detector to Eliminate "Dead Band" Effects
- Low Operating Power, Typically 175mW
- 1.3GHz Operating Frequency
- Complete Phase Locked Loop
- high Input Sensitivity
- Programmed through Three Wire Data Bus
- Wide Range of Reference Division Ratios
- Local Storage for Two Frequency Words giving Rapid Frequency Toggling
- Programmable Phase Detection Gain
- Power Down Mode
- ESD Protection on all pins.

ABSOLUTE MAXIMUM RATINGS

Supply voltage	0.3V to 7V
Storage temperature	–55°C to +150°C
Operating temperatue	–40°C to+85°C
Prescaler input voltage	2.5V p–p

ORDERING INFORMATION

SP8861/NA/HP



Pin	Description	Pin	Description
1	IC	15	CLOCK
2	$V_{EE}3$	16	ENABLE
3	PD1 OUTPUT	17	NC
4	*F_{pd}	18	$V_{CC}2$
5	*F_{ref}	19	$V_{EE}2$
6	POWER DOWN	20	XTAL 2
7	$V_{EE}4$	21	XTAL 1
8	$V_{CC}4$	22	EARTH
9	$V_{CC}1$	23	$V_{CC}3$
10	RF INPUT	24	RPD
11	RF INPUT	25	PD2 OUTPUT
12	$V_{EE}1$	26	NC
13	F1/F2	27	LOCK DETECT
14	DATA	28	Cd

*** F_{pd} and F_{ref} outputs are reversed by the phase detector sense bit in the programming word. Diagram above is correct when sense bit is low.**

$V_{CC}1$, $V_{EE}1$ – Preamp and Prescaler
$V_{CC}2$, $V_{EE}2$ – Oscillator Supplies
$V_{CC}3$, $V_{EE}3$ – Charge Pump 2 Supplies
$V_{CC}4$, $V_{EE}4$ – ECL Supplies

Fig. 1 Pin connections – top view

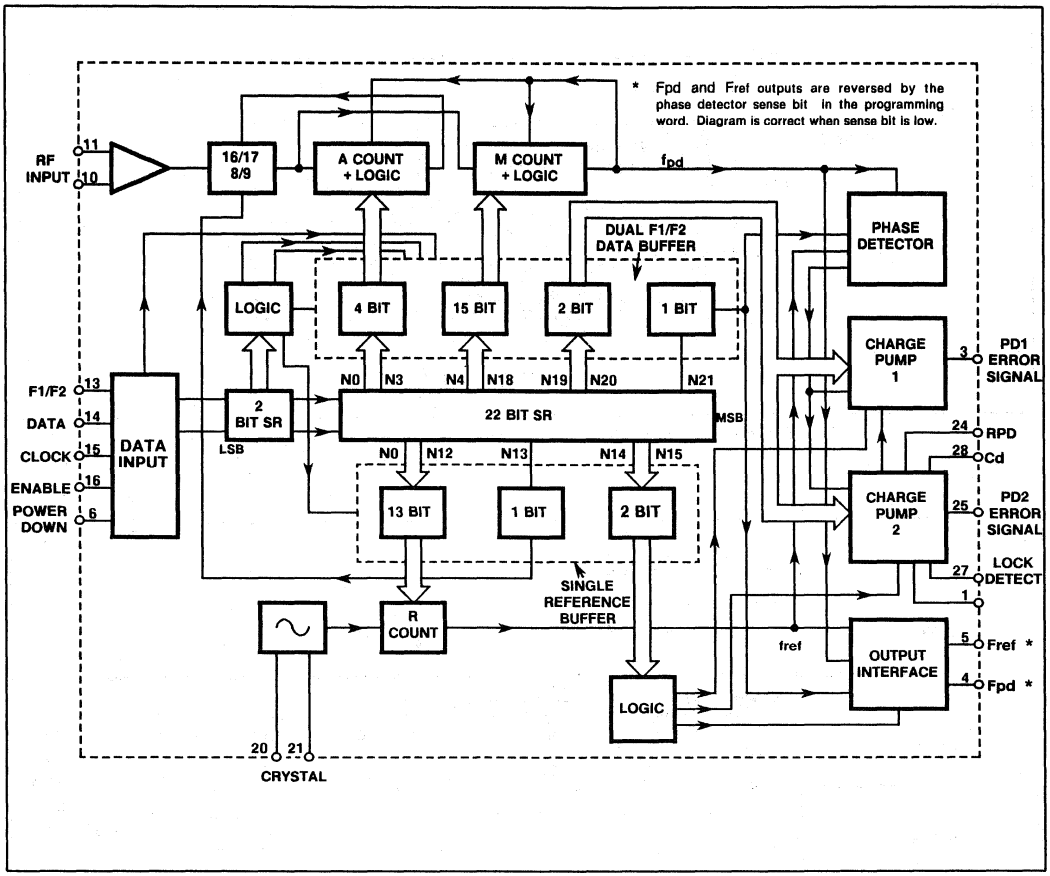


Fig. 2 SP8861 block diagram

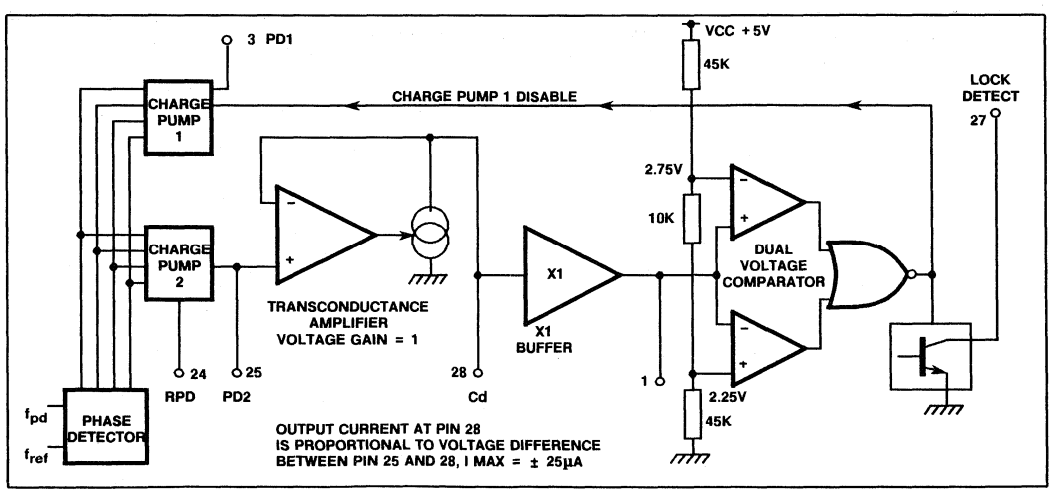


Fig. 3 Detailed Block Diagram of Lock Detect Circuit

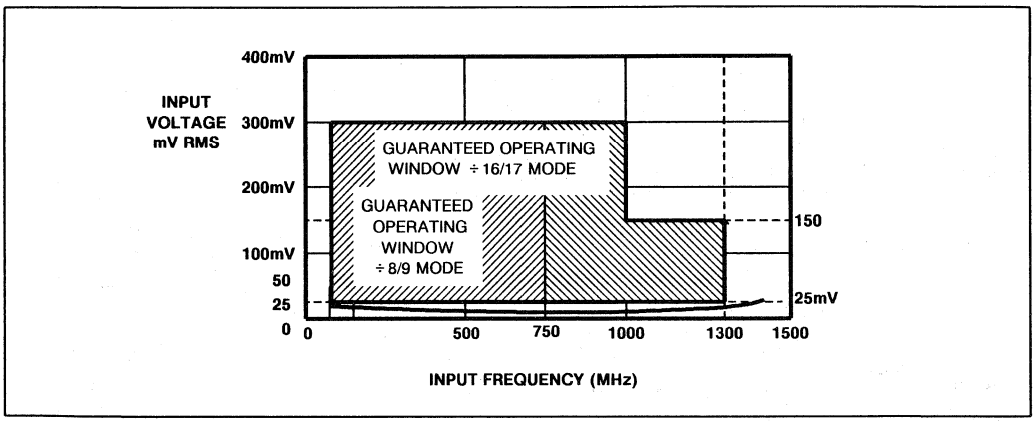


Fig. 4 Typical input characteristics and input drive requirements

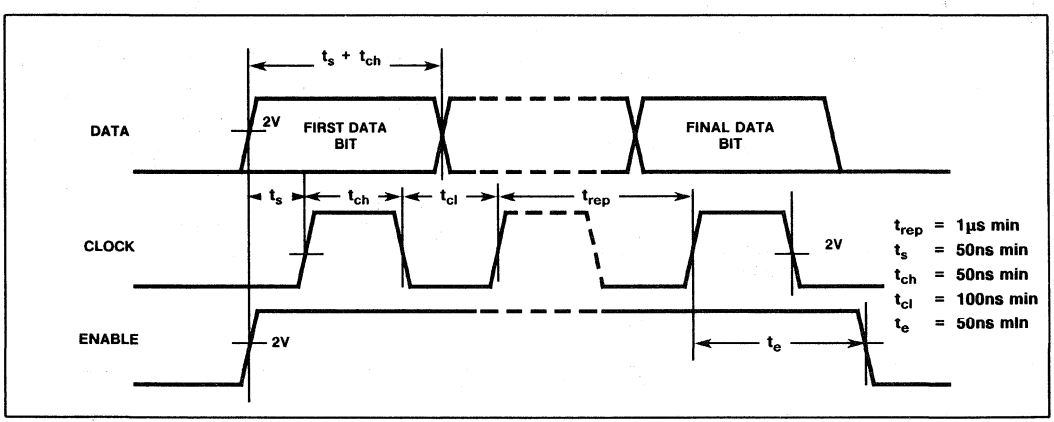


Fig. 5 Data and clock timing requirements

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
Supply Voltage V_{CC} +4.75 to + 5.25V
Temperature T_{amb} = 25°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ	Max.		
Supply Current	8,9					
	18,23		33	40	mA	
Supply Current in Power Down Mode	8		4.5	6	mA	
Input Sensitivity	10,11					See Figure 4a and b
Input Overload	10,11					See Figure 4a and b
RF Input Division Ratio	10,11,4	256		524287		With 16/17 selected
		56		262143		With 8/9 selected
Comparison Frequency	4,5			5	MHz	
Reference Oscillator Input Frequency	20,21	4		20	MHz	
External Reference Input Voltage	20	10		500	mVrms	
Reference Division Ratio	20,5	1		8191		
Data Clock Repetition Rate t_{rep}	15			1	µs	See Figure 5
Minimum Set up Time t_s	14,15	50			ns	See Figure 5
Data Input High	14	0.6Vcc		Vcc	V	
Low	14	Vee		0.3Vcc	V	
Clock Input High	15	0.6Vcc		Vcc	V	
Low	15	Vee		0.3Vcc	V	
Data Enable High	16	0.6Vcc		Vcc	V	
Low	16	Vee		0.3Vcc	V	
F1/F2 Input High	13	0.6Vcc		Vcc	V	F1 buffer selected
Low	13	Vee		0.3Vcc	V	F2 buffer selected
Power Down Input High	6	0.6Vcc		0.9Vcc	V	
Low	6	Vee		0.3Vcc	V	
F1/F2 Input Current	13			5	µA	V Pin 13 = 5.0V
Power Down Input Current	6			5	µA	v Pin 6 = 4.5V
RPD External Resistance	24	68		330	KΩ	
Lock Detect Output Voltage "in lock"	27			1	V	I pin 27 = 1mA
Lock Detect Switching Voltage High	25	2.7			V	Vcc = 5V
Low	25			2.3	V	Vcc = 5V
Fpd and Fref Output Voltage Swing			0.9		V	Vcc = 5V. External pull down may be required

DESCRIPTION

Prescaler and A M counter

The programmable divider chain is of A M counter construction and therefore contains a dual modulus front end prescaler, an A counter which controls the dual modulus ratio and an M counter which performs the bulk multi-modulus division. A programmable divider of this construction has a division ratio of MN + A and a minimum integer steppable division ratio of N(N-1).

In the SP8861 the dual modulus front end prescaler is a dual N ratio device capable of being statically switched between 16/17 and 8/9 ratios. The controlling A counter is of four bit design enabling a maximum count sequence of 15, (2^4-1) which begins with the start of the M counter sequence and stops when it has counted by the preloaded number of cycles. Whilst the A counter is counting the dual modulus prescaler is held in the N + 1 mode, then relaxes back to the N mode at the completion of the sequence. The M counter is a 15-bit asynchronous divider which counts with a ratio set by a control word. In both A and M counters the controlling data from the F1/F2 buffer is loaded in sequence with every M count cycle. The N ratio of the dual modulus prescaler is selected by a one bit word in the reference divider buffer and, when a ratio of 8/9 is selected the A counter requires only three programming bits, having an impact on the frequency bit allocation as described in the data entry section.

Reference source and divider

The reference source in the SP8861 is obtained from an on board oscillator, frequency controlled by an external crystal. The oscillator can also function as a buffer amplifier allowing the use of an external reference source. In this mode the source is simply AC coupled into the oscillator transistor base on pin 20.

The oscillator output is coupled to a programmable reference divider whose output is the reference for the phase detector. The reference divider is a fully programmable 13-bit asynchronous design and can be set to any division ratio between 1 and 8191. The actual division ratio is controlled by a data word stored in the internal reference buffer.

Phase comparator

The SP8861 is provided with a digital phase comparator feeding two charge pump circuits. Charge pump 1 has preset currents programmable as shown in table 1. Charge pump 2 has a current level set by an external resistor: the current is multiplied by a factor determined by the F1 or F2 word (see table 1).

A lock detect circuit is connected to the output of charge pump 2. When the voltage level at pin 25 is between approximately 2.25 and 2.75 volts, pin 27 will be low and charge pump 1 disabled depending on the PD1 and PD2 programming bits as shown in table 4.

The output signals from the reference and M counters are available on pins 4 and 5 when programmed by the reference programming word: the various options are shown in table 4. An external phase detector may be connected to pins 4 and 5 and may be used independently or in conjunction with the on chip detector.

To allow for control direction changes introduced by the design of the control loop, a programming bit in the F1/F2 programming word interchanges the inputs to the on chip phase detector and reverses the functions on pins 4 and 5.

F1 OR F2 WORD G2	G1	CHARGE PUMP 1 CURRENT	CHARGE PUMP 2 MULTIPLIER
0	0	50µA	1
1	0	75µA	1.5
0	1	125µA	2.5
1	1	200µA	4

Table 1 Charge pump currents

Note: ***Charge pump 2** is pin 24 current × multiplication factor.* I pin 24 = $\frac{VCC-1.5V}{RPD}$

Data entry and storage

The data section of the SP8853 consists of a data input interface, an internal data shift register and three internal data buffers.

Data is entered to the data input interface by a three wire data highway with data, clock and chip enable inputs. The input interface then routes this data to a 24-bit shift register with bus connections to three data buffers. Data entered via the serial bus is transfered to the appropriate data buffer on the negative transition of the chip enable input according to the two final data bits as shown in Table 3. The MSB of the data is entered first.

The dual F1/F2 buffer can receive two 22-bit words and controls the programmable divider A and M counters using 19-bits, the phase detector gain with two bits and the phase detector sense with one bit. A fourth input from the synthesiser control system selects the active buffer.

OUTPUT FOR RF PHASE LAG	
Sense Bit	Pins 3 and 25
0	Current source
1	Current sink

Table 2

The third buffer contains only 16 bits, 13 being used to set the reference counter division ratio, and 2 to control the phase comparator enable logic. The remaining bit sets the dual modulus prescaler N ratio.

2 Bit S.R. Contents	Buffer Loaded
00	F1
10	F2
01	Active A *
11	Reference

Table 3

** Transfer of A counter bits into buffer controlling the programmable counter*

The data words may be entered in any individual multiple sequence and the shift register can be updated whilst the data buffers retain control of the synthesiser with the previously loaded data. This enables four unique data words to be stored in the device, with three in the data buffers and a fourth in the shift register, whilst the chip is enabled. F1 word may also be updated whilst F2 is controlling the programmable divider and vice versa.

The dual F1/F2 buffer enables the device to be toggled between two frequencies using the F1/F2 select input at a rate determined by the comparasion frequency

and also enables random frequency hopping at a rate determined by a byte load period, since the loop can be locked to F1 whilst F2 is updated by entering new data via the shift register. The F1/F2 input is high to select F1.

An F1 or F2 update cycle will consist of a byte containing 24 bits, whereas the reference byte will contain 18 bits. The device requires 3 bytes, each with a chip select sequence, totalling 66 bits to fully program.

When the dual modulus counter (A count) is set to ÷8/9, the data required to set the counter is reduced by one bit, leaving an unused bit in the 22-bit F1/F2 buffer. this bit must always be set to zero when ÷8/9 mode is required. Various programming sequences are shown in Fig. 7

The data entry and storage registers are always powered up, making it possible to enter data when the device is in the powered down state.

PD2	PD1	
0	0	Fref and Fpd outputs off, charge pump 1 and 2 on
0	1	Fref and Fpd outputs on, charge pump 1 off. Charge pump 2 on
1	0	Fref and Fpd outputs off, charge pump 1 disabled by lock detect. Charge pump 2 on
1	1	Fref and Fpd outputs on, charge pump 1 disabled by lock detect. Charge pump 2 on

Table 4

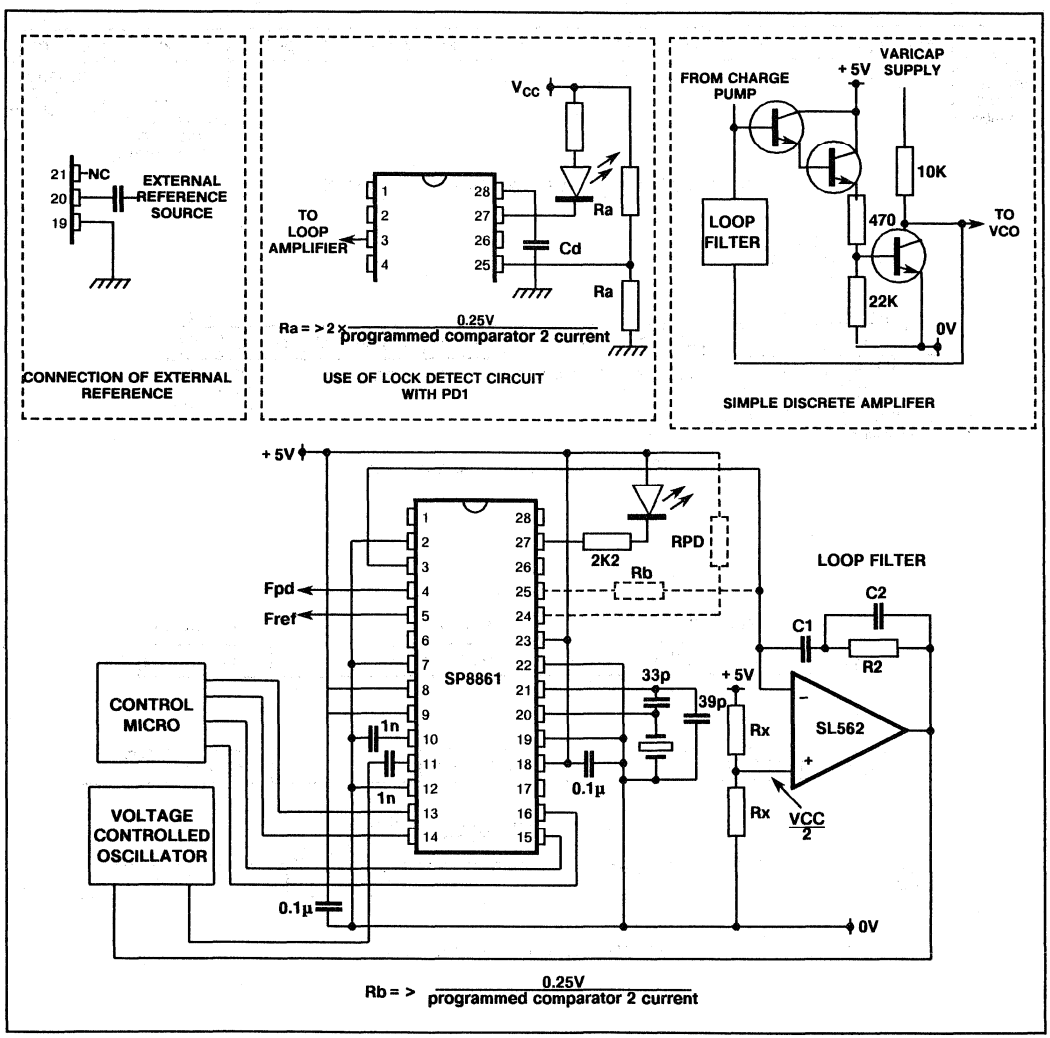


Fig. 6 Typical application diagram

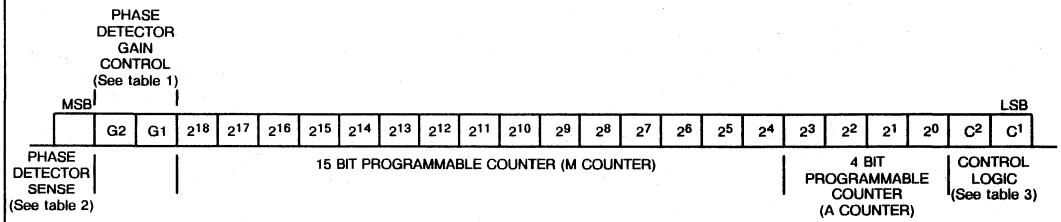


FIG.7(a) F1 or F2 word, bit allocation with 16/17 selected

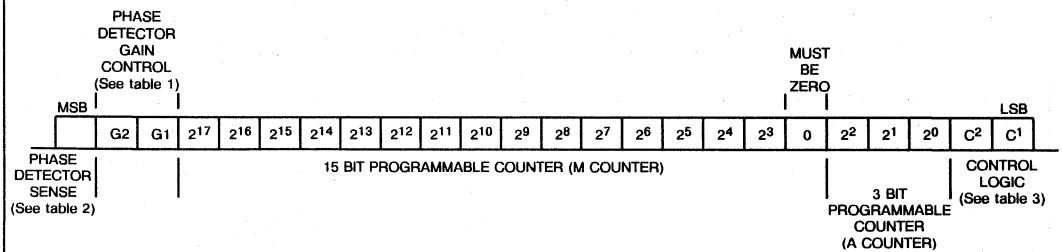


FIG.7(b) F1 or F2 word, bit allocation with 8/9 selected

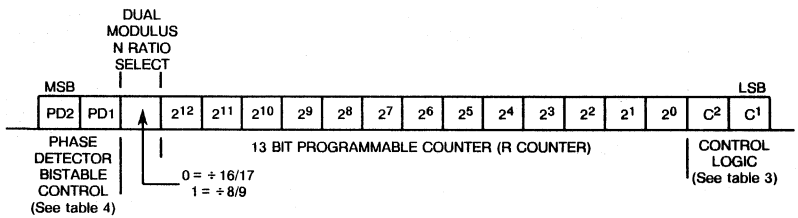


FIG.7(c) reference word bit allocation

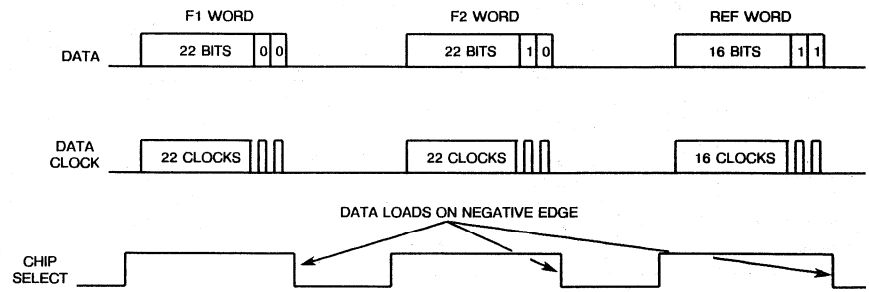


Fig.7(d) Typical data load sequence

Fig. 7 Data format diagrams

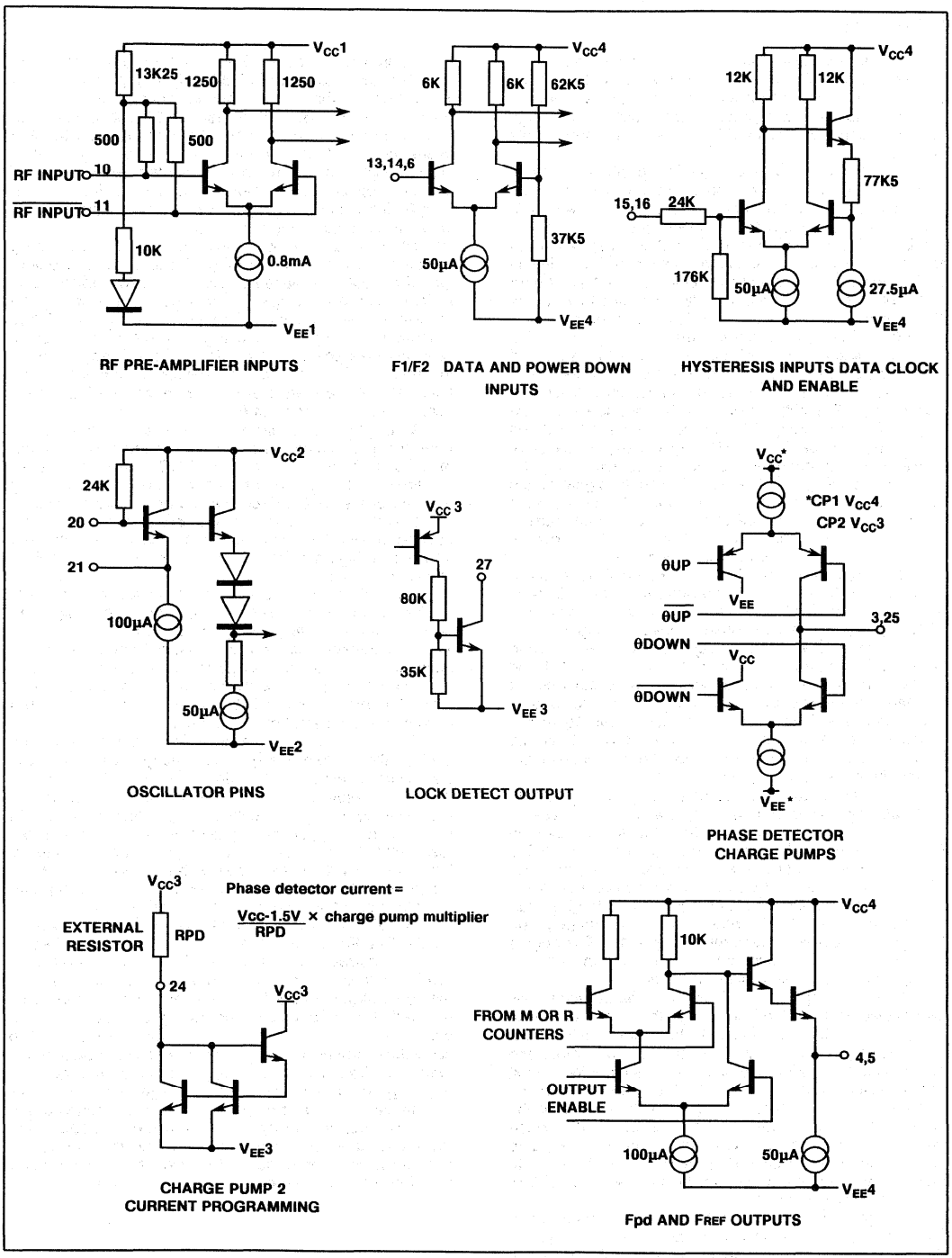


Fig. 8 Input and output interface diagrams

APPLICATIONS

A basic application using a single phase comparator is shown in Fig. 6. The SP8861 is a 1.5 GHz part, so good RF design techniques should be employed, including the use of a ground plane and suitable high frequency capacitors at the RF input and for power supply decoupling.

The RF input should be coupled to either pin 10 or 11, and the other pin decoupled to ground. The reference oscillator is of conventional Colpitts type with two capacitors required to provide a low impedance tap for the feedback signal to the transistor emitter. Typical values are shown in figure 6, although these may be varied to suit the loading requirements of particular crystals. Where a suitable reference signal already exists or where a very stable source is required, it is possible to apply an external reference as shown inset in Fig. 6. The amplitude should be kept below 0.5V RMS to avoid forward biasing the transistor collector base junction.

In some systems, it is useful to have an indication of phase lock. The output from pin 27 goes low when the output of charge pump 2 is between 2.25 and 2.75V and can be used to operate an LED to give visual indication of phase lock. Alternatively a pull-up resistor may be connected to V_{CC} and the output used to signal to the control microprocessor that the loop is locked thus speeding up system operation. The output current available from pin 27 is limited to 1.5mA. If this current is exceeded the logic low level will be uncertain.

The circuit diagram shown in figure 6 is a basic application with minimum component count which is nevertheless perfectly adequate for many applications. Charge pump 1 on pin 3 is used to drive the loop amplifier which provides the control voltage for the local oscillator. When charge pump 1 is used in this mode, the PD1 and PD2 bits in the reference programming word must be set to enable charge pump 1 continuously. This application could also use charge pump 2 output on pin 25 or if a higher phase comparator gain is required, pins 3 and 25 could be connected in parallel to use the combined output current from both charge pumps.

The lock detect circuit can be programmed to automatically disable charge pump 1 as shown in Table 4. This feature can be used to reduce the system lock up time by connecting the charge pump outputs in parallel to the loop amplifier with a resistor, (shown dotted) in series with charge pump 2. This connection allows a relatively high current to be used from charge pump 1 to give short lock up time, and a low current to be set on charge pump 2 giving low reference frequency sidebands. The degree of lock up time improvement depends on the ratio of charge pump 1 to charge pump 2 currents.

When the loop is out of lock, both charge pumps will be enabled and will feed current to the loop amplifier to bring the oscillator to phase lock. The current from charge pump 2 will produce a voltage drop across the series resistor allowing operation of the lock detect circuit and enabling charge pump 1. The resistor must be chosen to give a voltage drop greater than 0.25V at the current level programmed for charge pump 2. When phase lock is achieved, there will be no charge pump current and therefore the voltage at pin 25 will be equal to that on the virtual earth point of the loop amplifier (2.5V), disabling charge pump 1.

Charge pump 1 should not be left open circuit when enabled as this prevents correct operation of the phase detector. The output on pin 3 should be biased to half supply with a pair of 4.7kΩ resistors connected between supplies.

When charge pump 2 is used to drive the loop amplifier, the lock detect circuit will only give an out of lock indication when large frequency changes are made or when a frequency outside the range of the local oscillator is programmed. At other times the loop amplifier input is maintained at 2.5V by the action of the loop filter components. Again a resistor connected between pin 25 and the loop amplifier, producing a voltage drop greater than 0.25V at the charge pump current programmed will allow sensitive out of lock detection.

When phase lock detection is required using comparator 1 only (see inset Fig.6) charge pump 2 output (pin 25) should be biased to 2.5V using two equal value resistors across the supply. The values should be chosen to give a voltage change greater than 0.25V at the programmed comparator 2 charge pump current. A small capacitor connected from pin 28 to ground may be used to reduce chatter at the lock detect output. (see inset figure 6) A detailed block diagram showing the lock detect circuitry is shown in Fig 3.

An amplifier is required to convert the current pulses from the phase comparator into a voltage of suitable magnitude to drive the chosen VCO. The choice of amplifier must be determined by the voltage swing required at the VCO to achieve the necessary frequency range, and in most cases an operational amplifier will be used to provide the essential characteristics of high input impedance, high gain and low output impedance required in this application.

Although it is expected that an operational amplifier will be used in most cases, a simple discrete design can be used and a suitable design is shown inset in Fig. 6. This arrangement can be particularly useful when the minimum VCO control voltage must be close to ground and where negative supplies are inconvenient. This form of amplifier is not suitable for use with charge pump 2 when the lock detect circuit is required.

When an operational amplifier is used in the inverting configuration shown in Fig. 6, the charge pump output is connected directly to the virtual earth point and will therefore operate at a voltage similar to that set on the non-inverting input. Normaly this operating point should be set at half supply using a potentiometer of two equal resistors, but if necessary this voltage can be set up to 1V higher or lower than half supply without detrimental effect. When the lock detect function is required on charge pump 2, the non inverting input must be at half supply.

The digital phase comparator and charge pump used on the SP8861 produces bi-directional current pulses in order to correct errors between the reference and VCO divider outputs. Once synchronisation is achieved, in theory no further output from the charge pump should be required, but in practice, due to leakage currents and particularly the input current of the amplifier, the capacitors forming the loop filter around the amplifier will gradually discharge, modifying the VCO voltage and requiring further outputs from the charge pump to restore the charge. The effect of this continuous correction of the local oscillator frequency, is to frequency modulate the VCO and thus produce sidebands at the reference frequency. In order to reduce this effect to a minimum, an amplifier with low input bias current is essential.

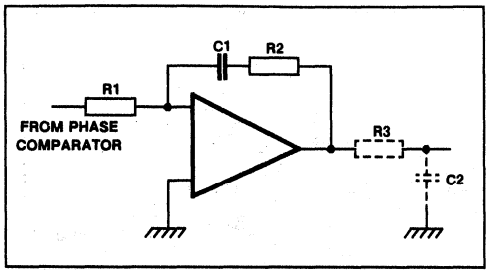


Fig. 9 Standard Form of Second Order Loop Filter

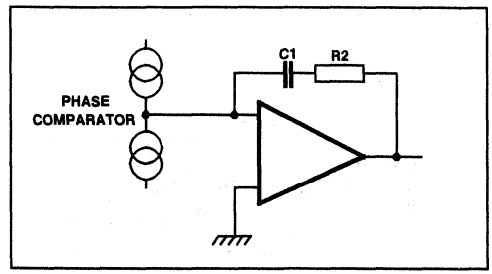


Fig.10 Modified Second Order Loop Filter

Loop calculations

Many frequency synthesiser designs use a second order loop with a loop filter of the form shown in figure 9.

In practice an additional RC time constant (shown dotted in Fig. 9) is often added to reduce noise from the amplifier. In addition any feedthrough capacitor or local decoupling at the VCO will be added to the value of C2. These additional components in fact form a third order loop, and if the values are chosen correctly, the additional filtering provided can considerably reduce the level of reference frequency sidebands and noise without adversly affecting the loop settling time. The calculation of values for both forms of loop is shown below.

Second Order Loop.

For this filter two equations are required to determine the time constants τ_1 and τ_2 where:

$$\tau_1 = C_1 R_1$$
$$\tau_2 = C_1 R_2$$

The equations are:

$$\tau_1 = \frac{K_\theta K_0}{\omega_n^2 N} \quad \ldots (1)$$

$$\tau_2 = \frac{2\zeta}{\omega_n} \quad \ldots (2)$$

where:

K_θ is the phase detector gain factor in V/Radian
K_0 is the VCO gain factor in radians second /Volt
N is the division ratio from VCO to reference frequency
ω_n is the natural loop bandwidth
ζ is the damping factor: normaly 0.7071

The SP8853 phase comparator is a current source rather than a conventional voltage source and has a gain factor specified in µA/radian. Since the equations deal with a filter where R_1 is feeding the virtual earth point of an operational amplifier from a voltage source, R_1 is setting the input current to the filter which is similar to the circuit shown in Fig. 10 where a current source phase comparator is connected directly to the virtual earth point of the operational amplifier.

The equivalent voltage gain of the phase comparator can be calculated by assuming a value for R_1 and calculating a gain in volts/radian which would produce the set current.

The digital phase comparator used in the SP8861 is linear over a range of 2π radians and therefore the phase comparator gain is given by:

$$\frac{\text{phase comparator current setting µA/Radian.}}{2\pi}$$

The phase comparator gain in V/radian is therefore:

$$\frac{50\,\mu A}{2\pi} \times 1K \text{ ohm}$$

assuming a value of 1K for R_1 and 50µA for the phase comparator current setting, these values can now be inserted in equation 1 to obtain values for C_1 and equation 2 used to determine a value for R_2.

Example:

Calculate values for a second order loop with the following parameters.

Frequency to be synthesised	800Mhz
Reference frequency	100KHz
Division ratio N	$\frac{800MHz}{100KHz}$ = 8000
Natural loop frequency ω_n	500Hz
VCO gain factor K_0	2π x 10MHz/Volt
Damping factor ζ	0.7071
Phase comparator current setting	50µA

Assuming R_1 is 1kΩ then the equivalent phase comparator gain K_θ in V/radian $= \frac{50\mu A}{2\pi} \times 1000$

$$K_\theta = 0.00796 \text{V/radian.}$$

From equation 1 $$\tau_1 \frac{0.00796 \times 2 \times \pi \times 10MHz}{(2 \times \pi \times 500)^2 \times 8000}$$

$$\tau_1 = 6.334 \times 10^{-6}$$

From equation 2 $$\tau_2 = \frac{2 \times 0.7071}{2 \times \pi \times 500}$$

$$\tau_2 = 4.50 \times 10^{-4}$$

Now $$\tau_1 = C_1 R_1 \quad \therefore C_1 = \frac{6.334 \times 10^{-6}}{1k\Omega}$$

1K is chosen value for R_1

$$C_1 = 6.33nF$$

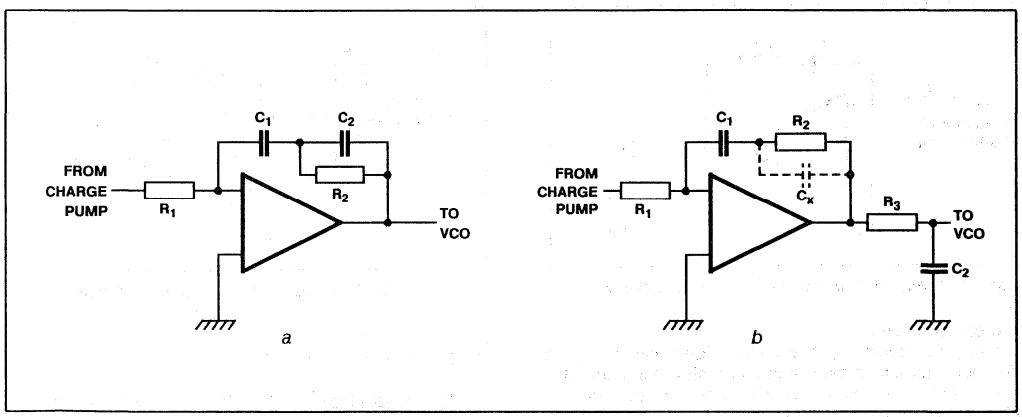


Fig. 11 Third Order Loop Filter

$$\tau_2 = C_1 R_2 \therefore \frac{4.50\times10^{-4}}{6.33\times10^{-9}} = R_2$$

$$R_2 = 71000\Omega$$

Third Order Loop

The third order loop filter is normally shown as in Fig. 11. Fig. 11b shows the circuit redrawn to use an RC time constant after the amplifier, allowing any feedthrough capacitance on the VCO line to be included in the loop calculations. Where the modified form in Fig. 11b is used it is advantageous to connect a small capacitor Cx of typically 100pF (shown dotted), across the amplifier to reduce sidebands caused by the amplifier being forced into non linear operation by the phase comparator pulses.

Three equations are required to determine the time constants, τ_1, τ_2 and τ_3 where :

for Fig. 11a
$$\tau_1 = C_1 R_1$$
$$\tau_2 = R_2 (C_1 + C_2)$$
$$\tau_3 = C_2 R_2$$

and for Fig. 11b
$$\tau_1 = C_1 R_1$$
$$\tau_2 = C_1 R_2$$
$$\tau_3 = C_2 R_3$$

The equations are:

$$\tau_1 = \frac{K_\theta K_0}{N\omega_n^2}\left[\frac{1+\omega_n^2\tau_2^2}{1+\omega_n^2\tau_3^2}\right]^{\frac{1}{2}} \quad \ldots(3)$$

$$\tau_2 = \frac{1}{\omega_n^2\tau_3} \quad \ldots(4)$$

$$\tau_3 = \frac{-\tan\phi_0 + \frac{1}{\cos\phi_0}}{\omega_n} \quad \ldots(5)$$

K_θ is the phase detector gain factor in V/Radian
K_0 is the VCO gain factor in radians second/Volt
N is the total division ratio from VCO to reference frequency
ω_n is the natural loop bandwidth
ϕ_0 is the Phase margin normaly set to 45°

As in the second order filter example a value for R1 can be assumed and an equivalent gain K_θ in V/radian calculated from:

$$\frac{\text{phase comparator current setting } \mu\text{A/radian}}{2\pi} \times 1\text{K}$$

Where 1K ohm is the assumed value for R_1

These values can now be substituted in equation (3) to obtain a value for C_1 and equations (4) and (5) used to determine values for C_2 and R_2.

EXAMPLE

Calculate values for a loop with the following parameters.

Frequency to be synthesised:	800MHz
Reference frequency	100KHz
Division ratio	$\frac{800\text{MHz}}{100\text{KHz}} = 8000$
ω_n natural loop frequency	500Hz
K_0 VCO gain factor	2π x 10MHz/Volt
ϕ_0 phase margin	45°
Phase comparator current	50μA

assuming R_1 is 1K Ohm, then the equivalent phase comparator gain K_θ in V/radian is:

$$\frac{50\mu\text{A}}{2\pi} \times 1000 = 0.00796 \text{ V/Radian}$$

From equation 3:

$$\tau_3 = \frac{-\tan 45° + \frac{1}{\cos 45°}}{500\text{Hz} \times 2\pi} = \frac{0.4142}{3141.6}$$

$$\tau_3 = 1.318 \times 10^{-4}$$

From equation 2:

$$\tau_2 = \frac{1}{(500 \times 2 \times \pi)^2 \times 1.318 \times 10^{-4}}$$

$$\tau_2 = 7.687 \times 10^{-4}$$

Using these values in equation 1:

$$\tau_1 = \frac{7.96 \times 10^{-3} \times 2 \times \pi \times 10\text{MHz/V}}{8000 \times (2\pi \times 500)^2} \left[A\right]^{\frac{1}{2}}$$

Where A is:

$$\frac{1+\omega_n^2 \tau_2^2}{1+\omega_n^2 \tau_3^2} = \frac{1+(2\pi\times500)^2\times(7.687\times10^{-4})^2}{1+(2\pi\times500)^2\times(1.318\times10^{-4})^2}$$

$$\tau_1 = \frac{500141.6}{7.896 \times 10^{10}} \left[\frac{6.832}{1.1714}\right]^{\frac{1}{2}}$$

$$\tau_1 = 6.334 \times 10^{-6} \times 2.415$$

$$\tau_1 = 1.53 \times 10^{-5}$$

now $\tau_1 = C_1 R_1$

$$\therefore C_1 = \frac{1.53 \times 10^{-5}}{1k\Omega} \quad (R_1 \text{ is chosen as } 1k\Omega)$$

$$C_1 = 0.0153\mu F$$

for figure 11a $\tau_2 = R_2 (C_1 + C_2)$

for figure 11a $\tau_3 = C_2 R_2$

substituting for C_2

$$\tau_2 = R_2\left[C_1 + \frac{\tau_3}{R_2}\right] \quad \therefore \tau_2 = R_2 C_1 + \tau_3$$

$$\therefore R_2 = \frac{\tau_2 - \tau_3}{C_1} = \frac{7.687 \times 10^{-4} - 1.318 \times 10^{-4}}{0.0153 \times 10^{-6}}$$

$$R_2 = 41627\Omega$$

$$\tau_3 = C_2 R_2 \quad \therefore C_2 = \frac{\tau_3}{R_2} = \frac{1.318 \times 10^{-4}}{41627}$$

$$C_2 = 3.17nF$$

for figure 11b $\tau_1 = C_1 R_1 \quad \therefore C_1 = \frac{1.53\times10^{-5}}{1k}$

$$C_1 = 0.0153\mu F$$

$$\tau_2 = C_1 R_2 \quad \therefore R_2 = \frac{7.687 \times 10^{-4}}{1.53 \times 10^{-8}}$$

$$R_2 = 50.242k\Omega$$

$$\tau_3 = C_2 R_3$$

Since both values are independent of the other components, either C2 or R3 can be chosen and the other calculated.

assume $R_3 = 1k\Omega \quad \therefore C_2 = \frac{1.318\times10^{-4}}{1000}$

$$C_2 = 1.318 \times 10\text{-}7$$

$$C_2 = 0.1318\mu F$$

Section 3
Frequency Dividers

MIL-STD-883 Class B

Many of the integrated circuits detailed in this section are available screened in conformance with MIL-STD-883 Class B and are identified in their ordering codes by the letters **AC** immediately following the device type number. Separate data sheets for these circuits are available from your local GEC Plessey Semiconductors Sales Office.

GEC PLESSEY
SEMICONDUCTORS

SP8400

VERY LOW PHASE NOISE SYNTHESISER DIVIDER

The SP8400 is a very low phase noise programmable divider which is based on a divide by 8/9 dual modulus prescaler and a 12 stage control counter. This gives a minimum division ratio of 56 (64 for fractional – N synthesis applications), and a maximum division ratio of 4103. Special circuit techniques have been used to reduce the phase noise considerably below that produced by standard dividers.The data inputs are CMOS or TTL compatible.

The SP8400 is packaged in a 28 pin plastic SO package.

FEATURES

- Very low Phase Noise (Typically –156dBc/Hz at 1kHz offset)
- Supply Voltage 5V

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	6.5V
Output Current	20mA
Storage Temperature Range	–55°C to +125°C
Maximum Clock Input Voltage	2.5V p–p

ORDERING INFORMATION

SP8400 KG MPES(Commercial Grade)

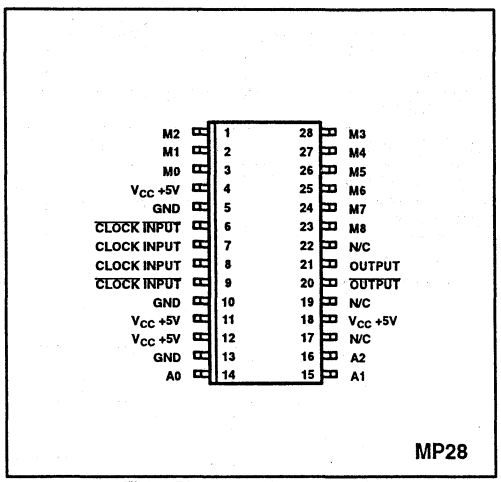


Fig. 1 Pin connections – top view

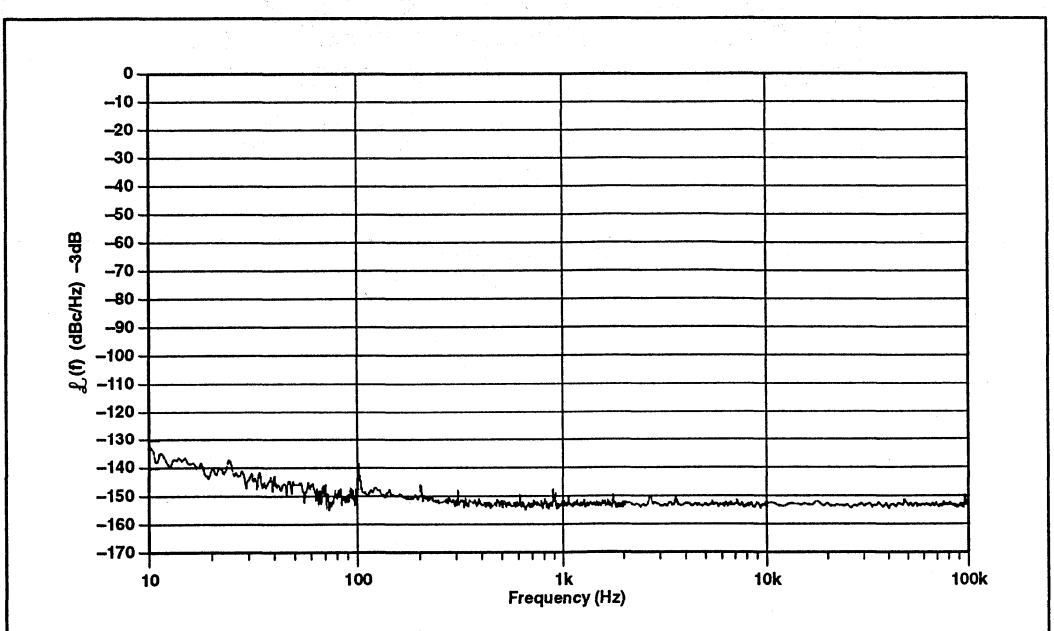


Fig. 2. Typical single sideband phase noise measured at 300MHz

ELECTRICAL CHARACTERISTICS

Guaranteed over: Supply Voltage V_{CC} = +4.75V to +5.25V Temperature T_{amb} = −10°C to +75°C
Tested at +4.75V and +5.25V at T_{amb} = +25°C

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	4,11,12, 18	122	137	152	mA	Outputs loaded with 330R See Fig.4
Output voltage swing	20,21	320	410		mV	p–p @ 1.5GHz input ÷ 71 mode See Fig. 4
Input sensitivity 200MHz to 1.5GHz	7,8			140 (–4)	mV dBm	RMS Sine wave into 50 Ohms (dBm equivalent) See Fig. 3
DATA INPUTS						
Logic high voltage		2.2			V	
Logic low voltage				0.8	V	
Input current				180	µA	5V Data input voltage

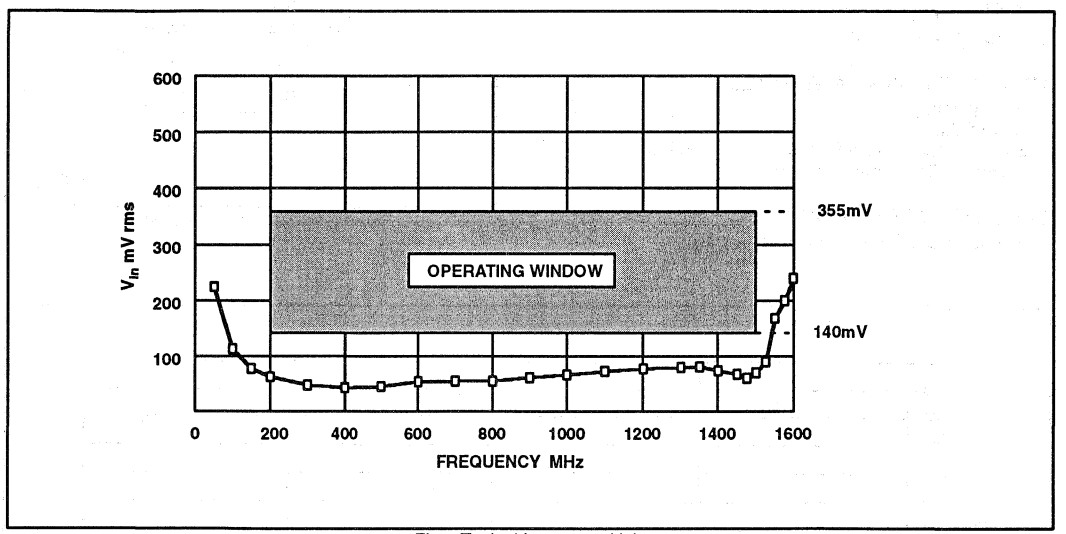


Fig.3 Typical input sensitivity

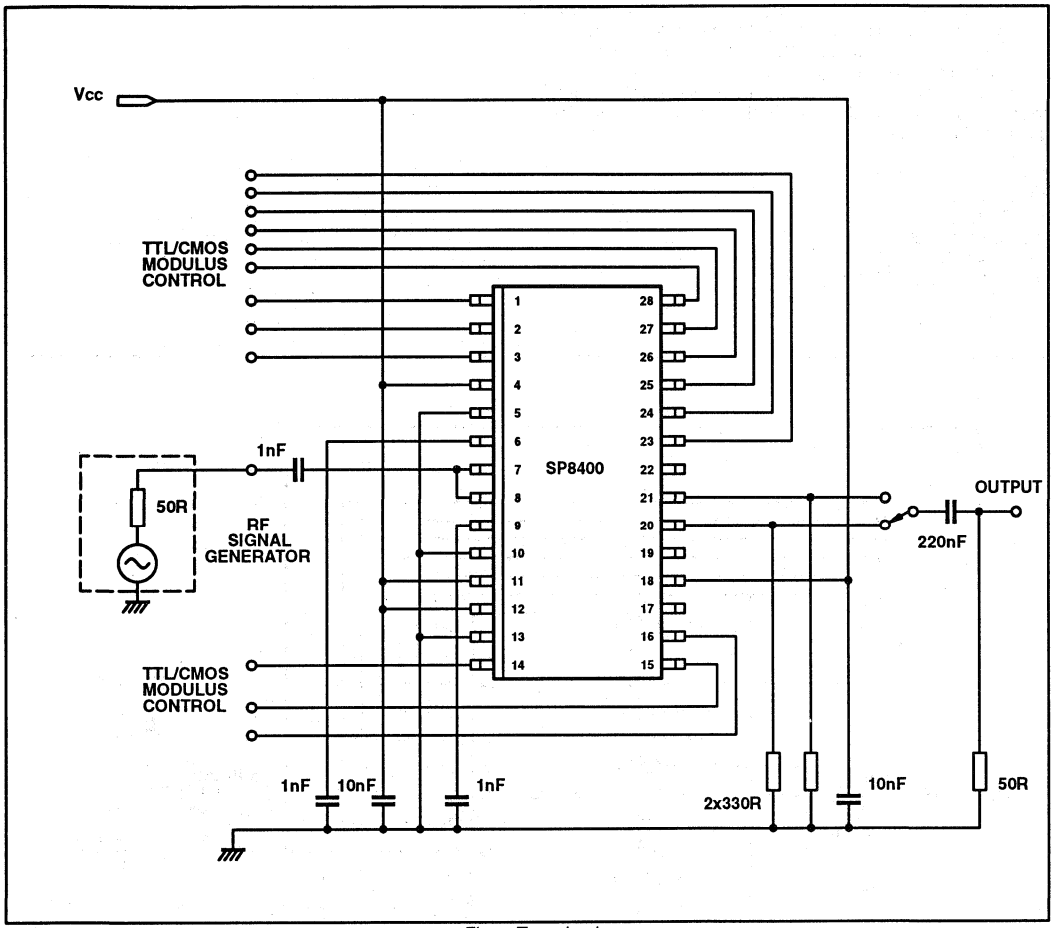


Fig. 4 Test circuit

APPLICATIONS INFORMATION

Circuit description, synthesiser divider

The divider is based on a divide by 8/9 modulus prescaler, and a 12 stage control counter. This gives minimum fractional – N division ratio of 64 (56 for general division), and a maximum division ratio of 4103. The inputs to the control counter are TTL/CMOS compatible. There is a fixed offset of 8 between the number on the data lines and the actual division ratio.

The output is one transition only per divide cycle. This eliminates the problem of where to put the redundant edge when the divider is used in a fractional–N system, and also avoids the problem of how to define the output pulse width. This means that the overall division ratio conventionally defined in terms of the rate of edges of the same polarity is twice the selected division ratio.

Equations for division

The M and A data inputs form a 12 bit number with A0 being the least significant bit and M8 being the most significant bit.

Definition 1: Division ratio – (input frequency to output edges, positive or negative).

= Number loaded + 8

Definition 2: Division ratio – (input frequency to output frequency).

= (Number loaded + 8) x 2

Available division ratio

All division ratios of 64 to 4103 (Definition 1) will return the divider to the same internal state at the end of the count and hence these are the only divisional ratios to be used for fractional–N synthesiser application.
All division ratios of 56 to 4103 are available for general division purposes. Additional division ratios available for general division are:–

8,9
16, 17, 18
24, 25, 26, 27
32, 33, 34, 35, 36
40, 41, 42, 43, 44, 45
48, 49, 50, 51, 52, 53, 54

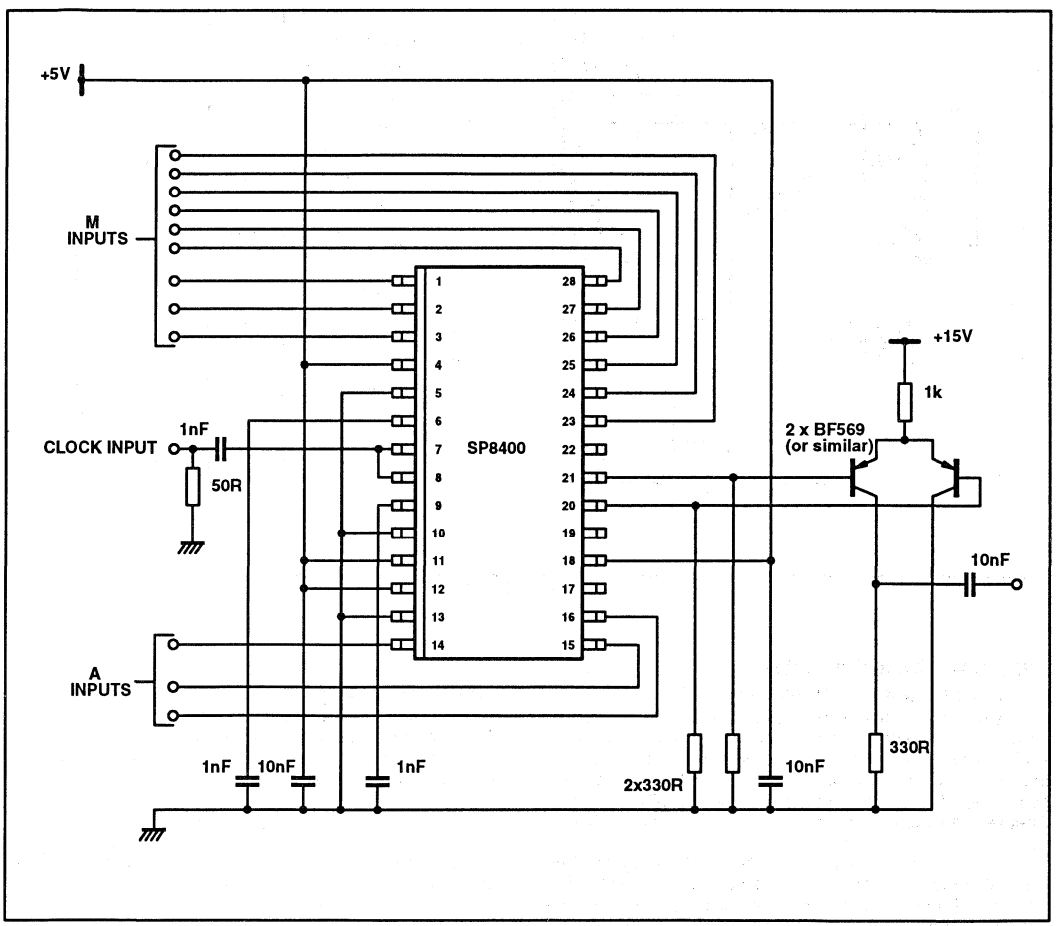


Fig. 5a Typical application combining output to increase signal and retain low phase noise

SP8401

(Supersedes February 1992 edition)

VERY LOW PHASE NOISE 300MHz ÷10/11

The SP8401 is a very low phase noise variable modulus divider. Special circuit techniques have been used to reduce the phase noise considerably below that produced by standard dividers. The modulus control input is CMOS or TTL compatable

The SP8401 is packaged in a 28 pin plastic SO package to be compatible with the SP8400 and SP8402 devices.

FEATURES

- Very low Phase Noise (Typically –160dBc/Hz at 1kHz offset)
- Supply Voltage 5V

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	6.5V
Output Current	20mA
Storage Temperature Range	–55°C to +125°C
Maximum Clock Input Voltage	2.5V p–p

ORDERING INFORMATION

SP8401 KG MPES (Commercial Grade)

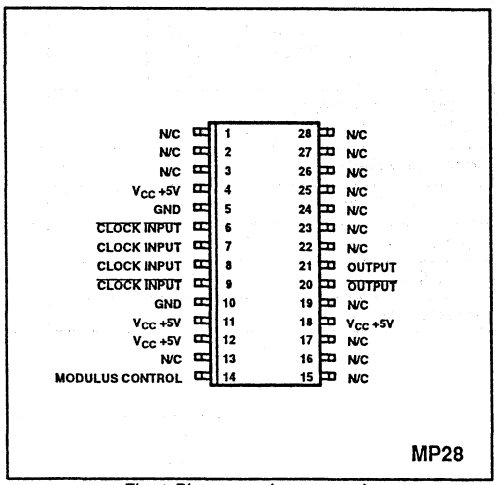


Fig. 1 Pin connections – top view

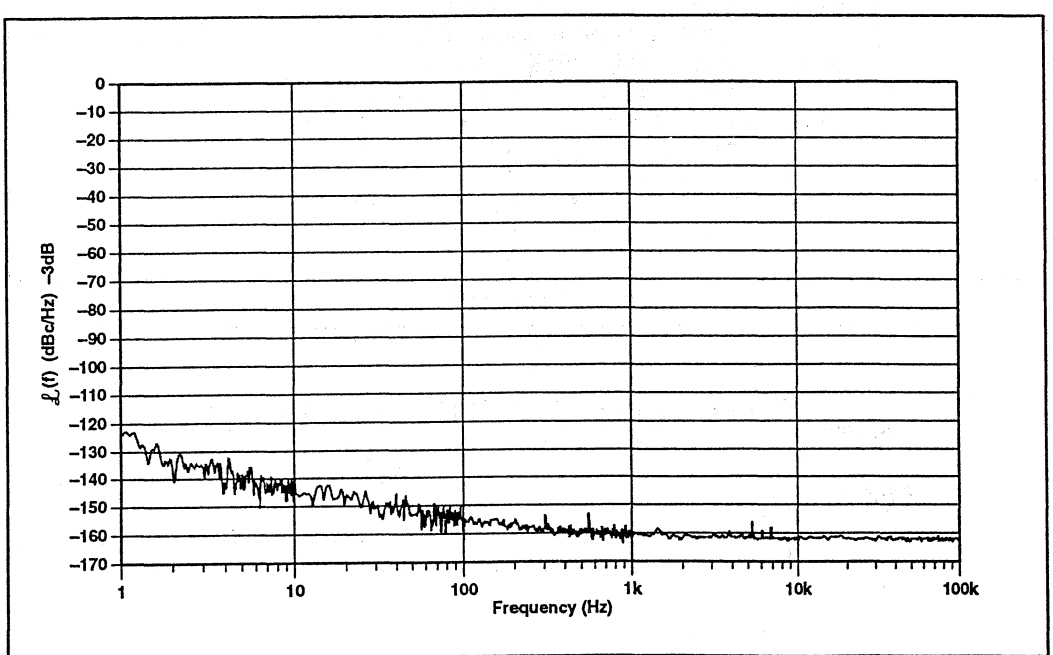


Fig. 2. Typical single sideband phase noise measured at 300MHz

ELECTRICAL CHARACTERISTICS

Guaranteed over; Supply Voltage V_{CC} = +4.75V to +5.25V, Temperature T_{amb} = −10°C to +75°C
Tested at +4.75V and +5.25V at T_{amb} = +25°C

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	4,11,12, 18	50	57	64	mA	Outputs loaded with 330R See Fig.5
Output voltage swing	20,21	340	440		mV	p–p @ 330MHz input ÷ 11 mode Outputs loaded with 330R
Input sensitivity 50MHz to 300MHz	7,8			140 (–4)	mV dBm	RMS Sine wave into 50Ω (dBm equivalent) See Fig. 3
MODULUS CONTROL INPUT						
Logic high voltage	14	2.2			V	÷10 mode
Logic low voltage	14			0.8		÷ 11 mode
Input current	14			180	µA	Modulus control input voltage 5V
Set up time t_s	14		4		ns	
Release time t_r	14		4		ns	

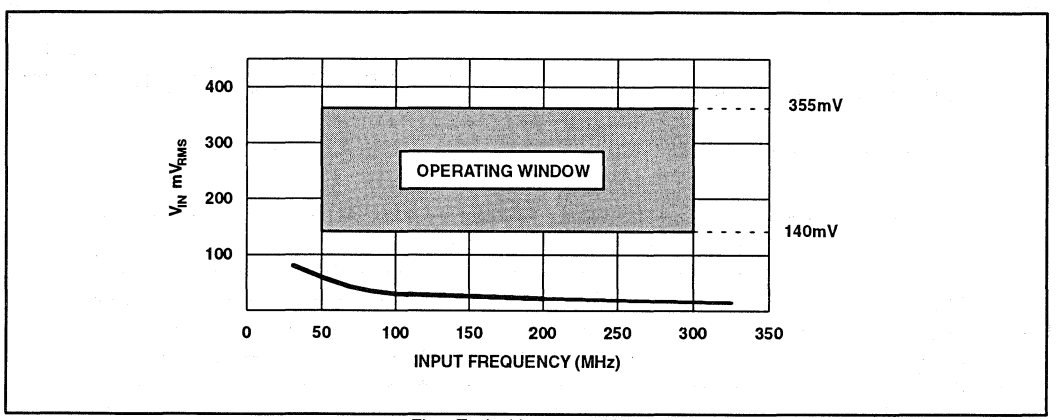


Fig.3 Typical input sensitivity

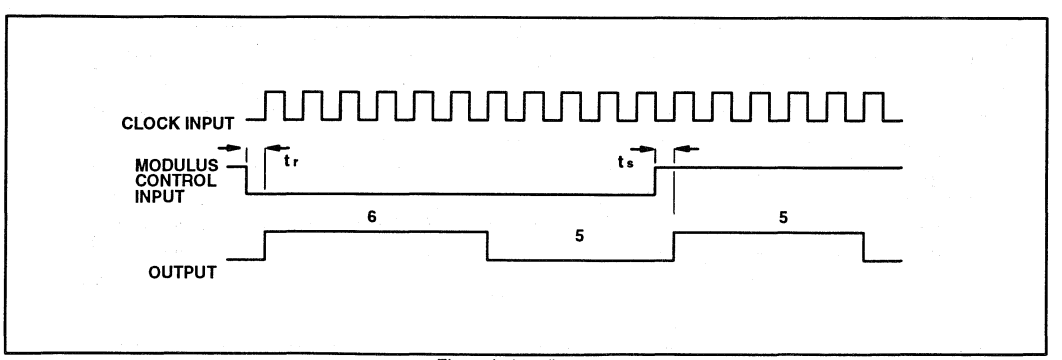


Fig.4. timing diagram

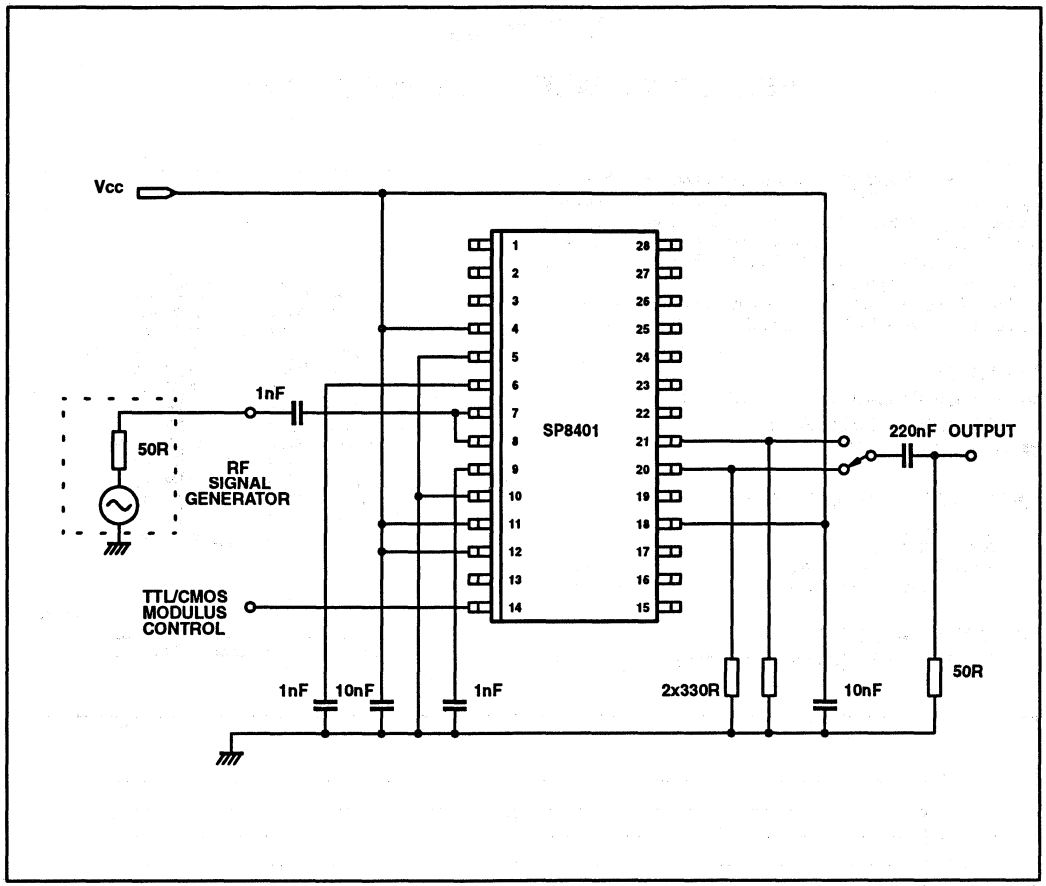


Fig. 5 Test circuit

SP8402

VERY LOW PHASE NOISE DIVIDE BY 2^N

The SP8402 is a very low phase noise divider which divides by powers of two. The S0, S1, S2 data inputs select the division ratio in the range 2^1 to 2^8. Special circuits techniques have been used to reduce the phase noise considerably below that produced by standard dividers.The data inputs are CMOS or TTL compatible.

The SP8402 is packaged in a 28 pin plastic SO package to be compatible with the SP8400 and SP8401 devices.

FEATURES

- Very low Phase Noise (Typically –155 to 160dBc/Hz at 1kHz offset)
- Supply Voltage 5V

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	6.5V
Output Current	20mA
Storage Temperature Range	–55°C to +125°C
Maximum Clock Input Voltage	2.5V p–p

ORDERING INFORMATION

SP8402 KG MPES (Commercial Grade)

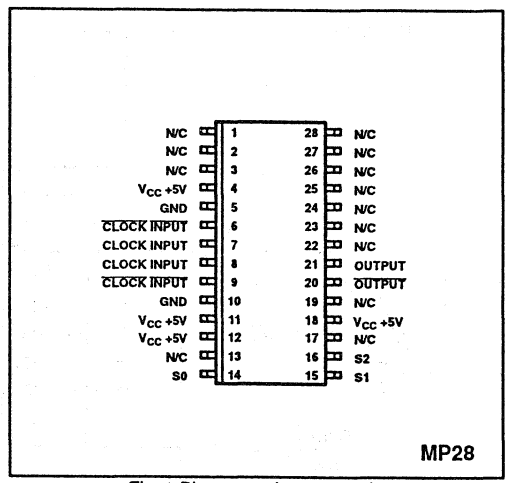


Fig. 1 Pin connections – top view

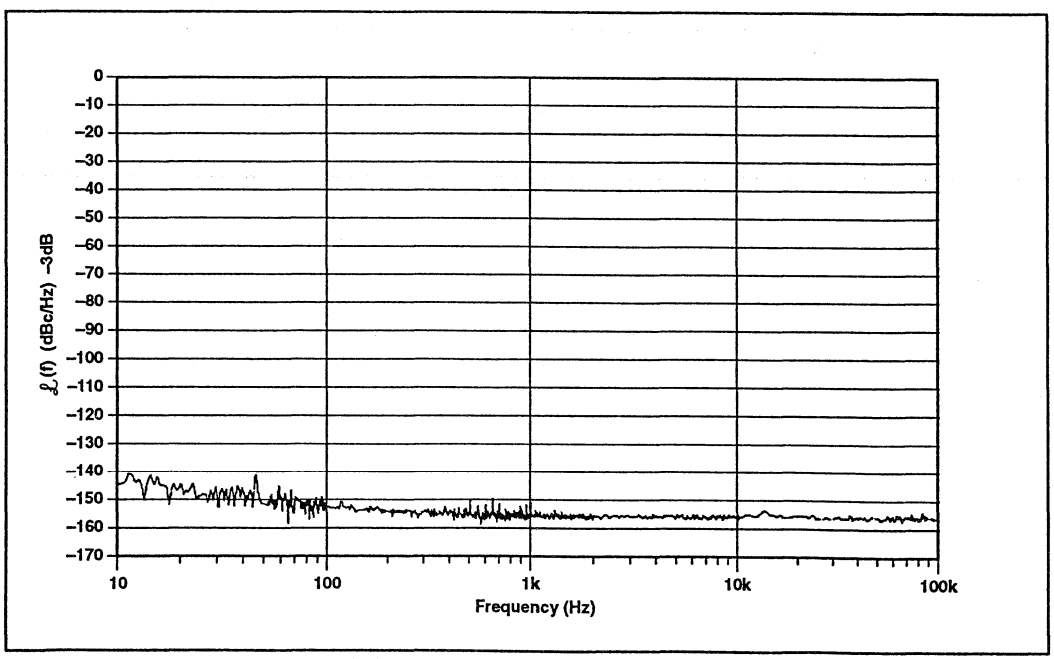


Fig. 2. Typical single sideband phase noise measured at 768MHz

ELECTRICAL CHARACTERISTICS

Guaranteed over : Supply Voltage V_{CC} = +4.75V to +5.25V Temperature T_{amb} = −10°C to +75°C
Tested at +4.75V and +5.25V at T_{amb} = +25°C

Characteristics	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	4,11,12, 18	82	92	102	mA	Outputs loaded with 330R See Fig.5
Output voltage swing	20,21	320	410		mV	p–p @ 1.4GHz input ÷ 256 mode outputs loaded with 330R See Fig. 5
Input sensitivity 200MHz to 1.4GHz	7,8			140 (–4)	mV dBm	RMS Sine wave into 50 Ohms (dBm equivalent) See Fig. 3
DATA INPUTS						
Logic high voltage		2.2			V	
Logic low voltage				0.8	V	
Input current				180	µA	5V Data input voltage

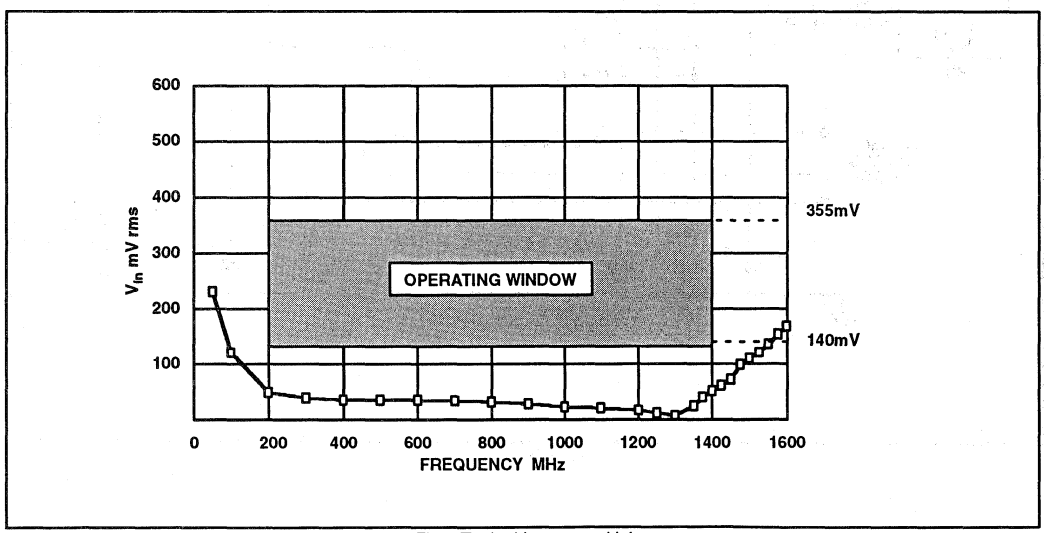


Fig.3 Typical input sensitivity

S0	S1	S2	DIVISION RATIO
L	L	L	2
H	L	L	4
L	H	L	8
H	H	L	16
L	L	H	32
H	L	H	64
L	H	H	128
H	H	H	256

Fig. 4 Truth table

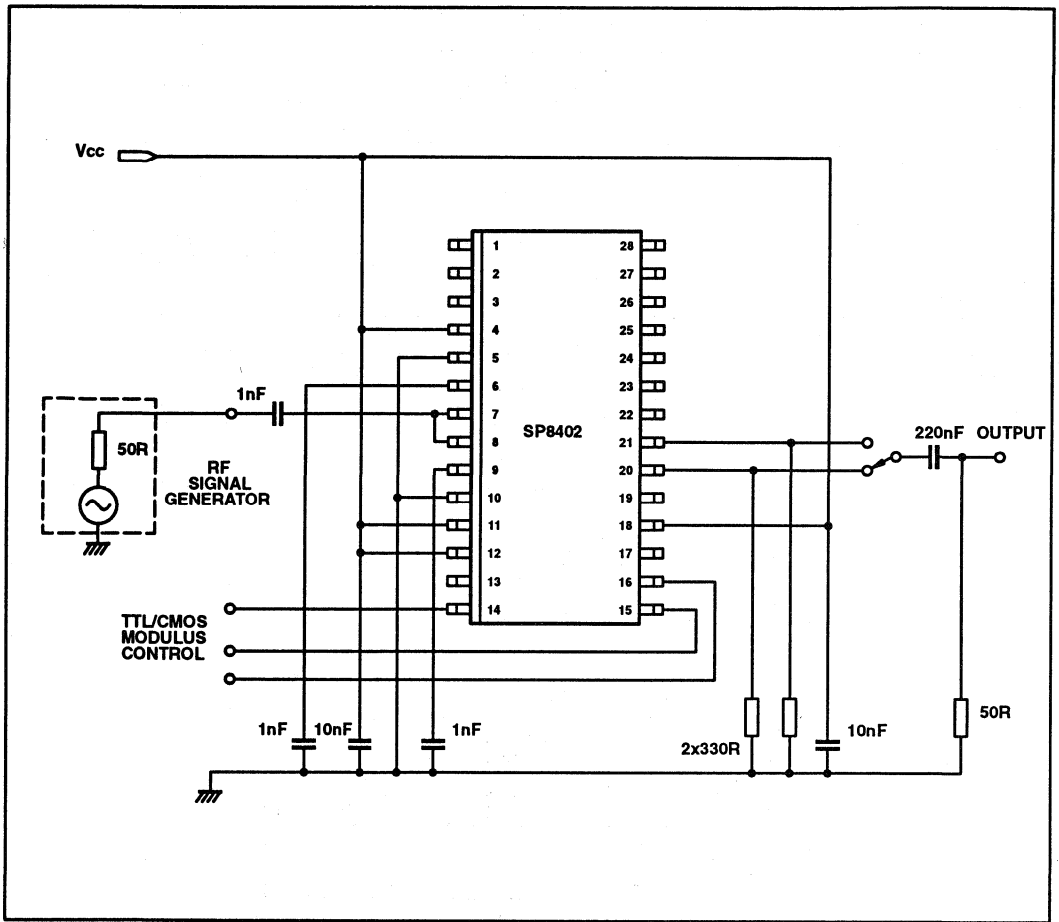


Fig. 5 Test circuit

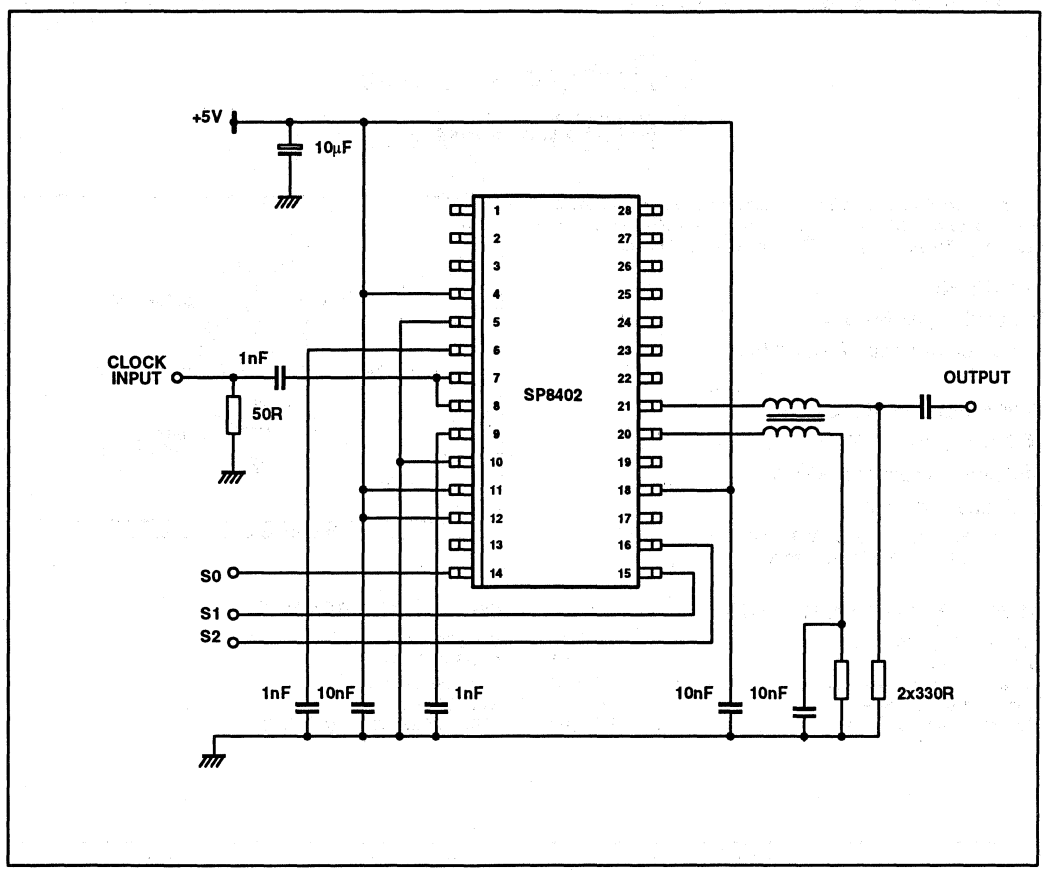


Fig. 6 Typical application – outputs combined in balun

SP8602 500MHz÷2
SP8604 300MHz÷2

The SP8602 and SP8604 are emitter coupled logic dividers which feature ECL10K compatible outputs when used with external pulldown resistors. The inputs are AC coupled.

FEATURES

- ECL Compatible Outputs
- AC-Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: −5·2V
- Power Consumption: 85mW
- Temperature Range:
  −55°C to +125°C (A Grade)
  −30°C to +70°C (B Grade)

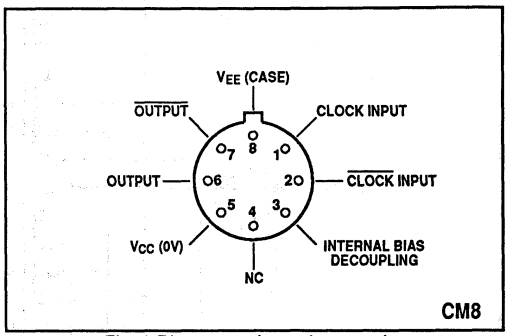


Fig. 1 Pin connections - bottom view

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{EE}	−8V
Output current	10mA
Storage temperature range	−65°C to +150°C
Max. junction temperature	+175°C
Max. clock input voltage	2·5V p-p

ORDERING INFORMATION

SP8602 A CM
SP8602 B CM
SP8604 A CM
SP8604 B CM
5962-92059 (SMD) (SP8602)

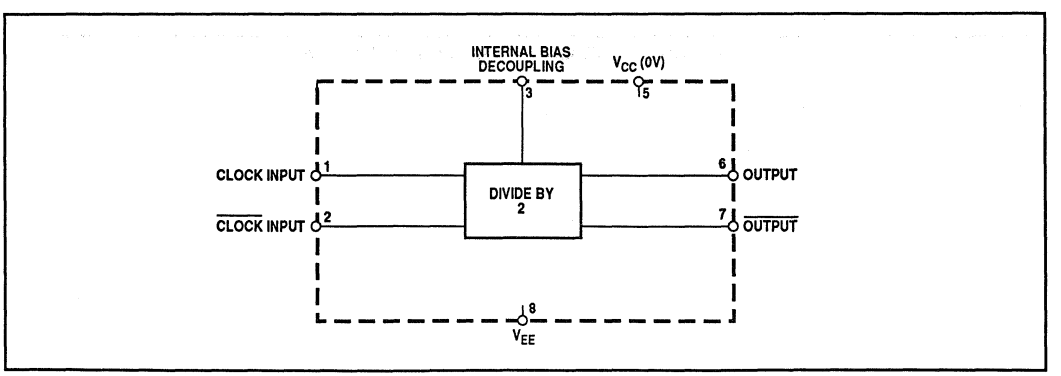


Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range
Supply voltage, V_{CC} = 0V, V_{EE} = −5·2V ± 0·25V
Temperature, T_{AMB} = −55°C to +125°C (A Grade), −30°C to +70°C (B Grade)

Characteristic	Symbol	Value		Units	Type	Conditions	Notes
		Min.	Max.				
Maximum frequency (sinewave input)	f_{MAX}	500		MHz	SP8602	Input = 400-800mV p-p	
		300		MHz	SP8604	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f_{MIN}		40	MHz	Both	Input = 400-800mV p-p	
Power supply current	I_{EE}		18	mA	Both	V_{EE} = −5·2V, outputs unloaded	
Output low voltage	V_{OL}	−1·8	−1·4	V	Both	V_{EE} = −5·2V	3
Output high voltage	V_{OH}	−0·85	−0·7	V	Both	V_{EE} = −5·2V	3
Minimum output swing	V_{OUT}	400		mV	Both	V_{EE} = −5·2V	

NOTES
1. The temperature coefficients of V_{OH} = +1·63mV/°C, and V_{OL} = +0·34mV/°C but these are not tested.
2. The test configuration for dynamic testing is shown in Fig.5.
3. Tested at 25°C only.

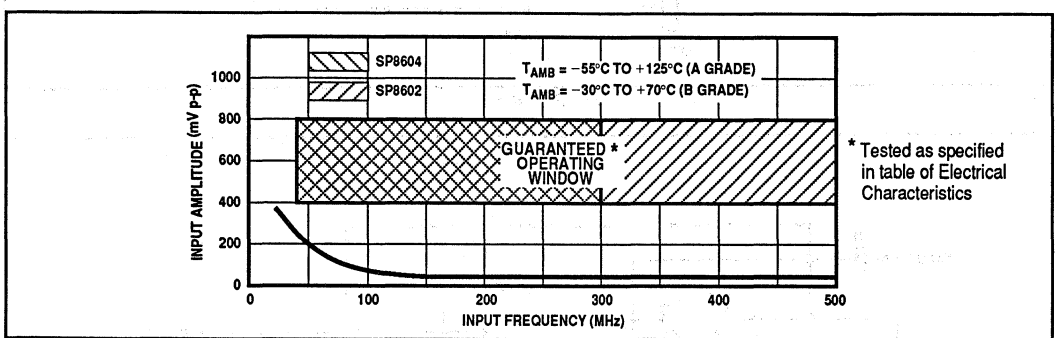


Fig. 3 Typical input characteristics of SP8602 and SP8604

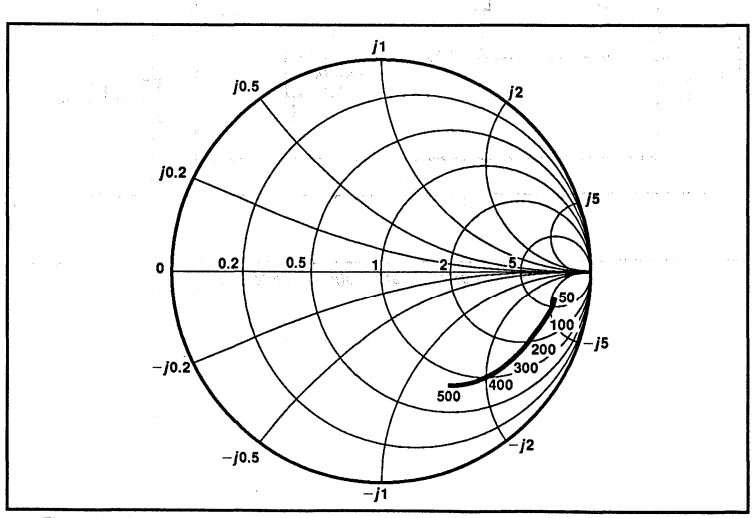


Fig. 4 Typical input impedance. Test conditions: supply voltage = −5·2V, ambient temperature = 25°C, frequencies in MHz, Impedances normalised to 50Ω

OPERATING NOTES

1. The clock inputs (pins 1 and 2) can be driven single ended or differentially and should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 3, to ground.
2. In the absence of a signal the device will self-oscillate. If this is undesirable, it may be prevented by connecting a 15kΩ resistor from the unused input to V_{EE}. This will reduce the input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/µs.
4. The outputs are compatible with ECLII. There is an internal load of 4kΩ on each output. The outputs can be interfaced to ECL10K by the addition of 1·5kΩ pulldown resistors from the outputs to V_{EE} to increase output voltage swing.
5. Input impedance is a function of frequency, See Fig. 4.
6. All components should be suitable for the frequency in use.

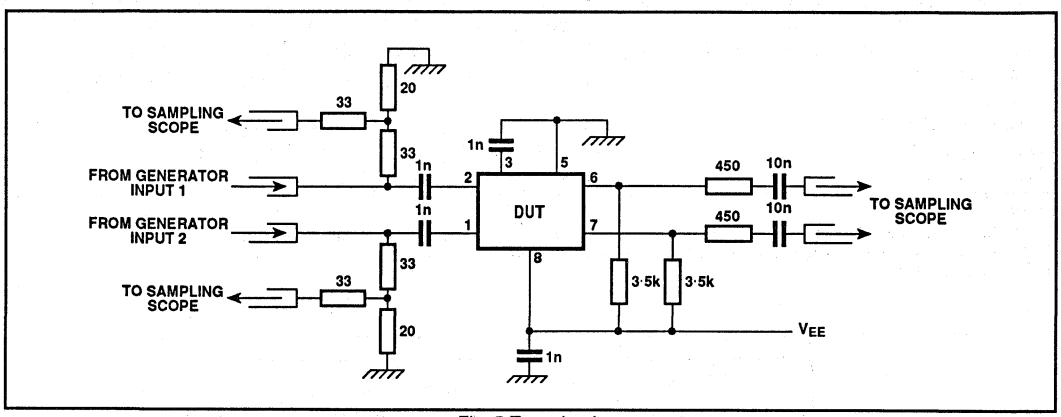


Fig. 5 Test circuit

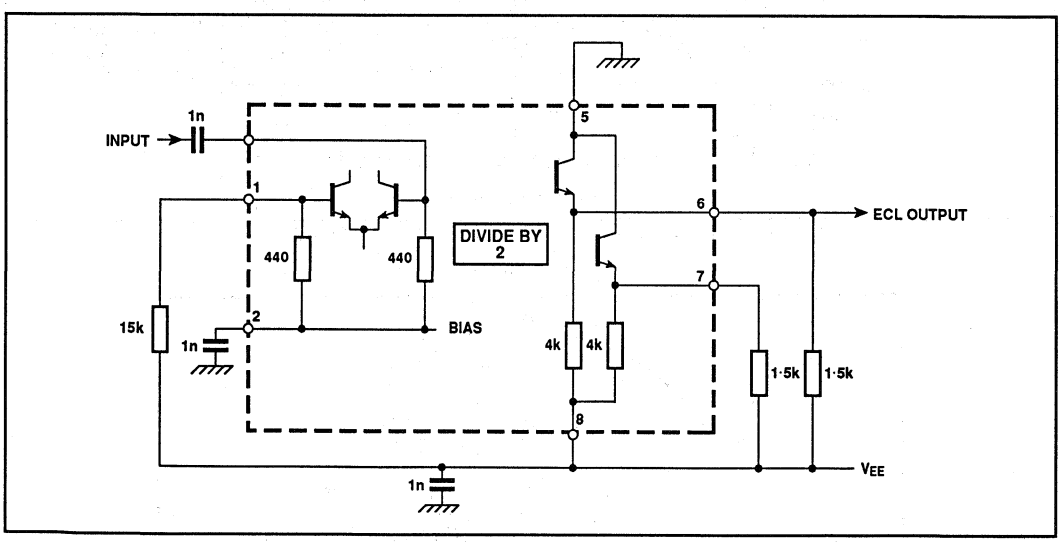


Fig. 6 Typical application showing interfacing

SP8605 1000MHz÷2
SP8606 1300MHz÷2

The SP8605 and SP8606 are emitter coupled logic dividers with ECIII compatible outputs when used with external pulldown resistors. Specified from 0°C to+70°C, these devices feature AC coupled inputs and 600mV p-p clock input sensitivity.

FEATURES

- ECL Compatible Outputs
- AC-Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: −5·2V
- Power Consumption: 320mW
- Temperature Range: 0°C to +70°C

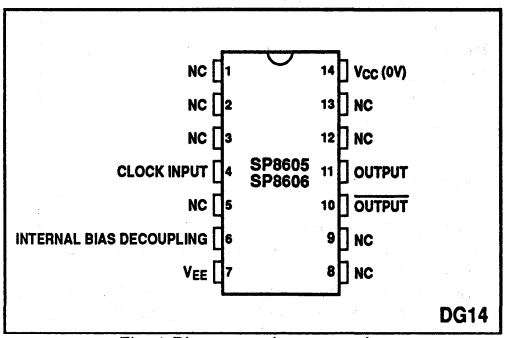


Fig. 1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{EE}	−8V
Output current	15mA
Storage temperature range	−65°C to +150°C
Max. junction temperature	+175°C
Max. clock input voltage	2·5V p-p

ORDERING INFORMATION

SP8605 B DG
SP8605 NA 1C
SP8606 B DG

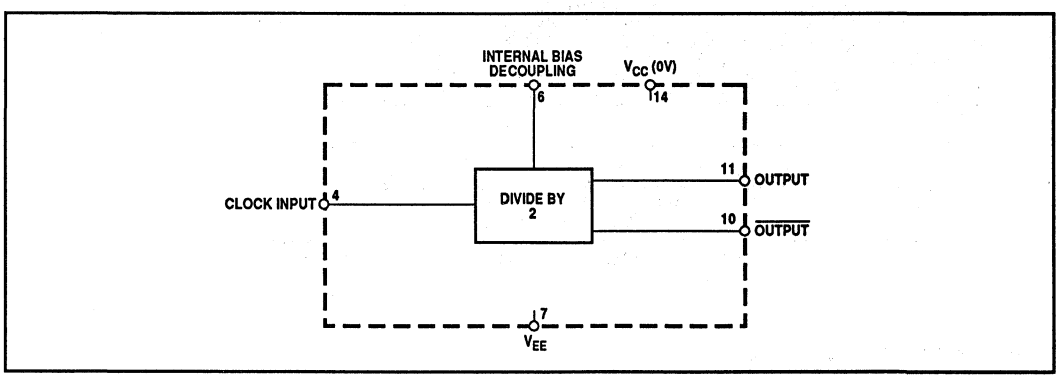


Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range
Supply voltage, V_{CC} = 0V, V_{EE} = −5·2V ± 0·25V
Temperature, T_{AMB} = 0°C to +70°C

Characteristic	Symbol	Value		Units	Type	Conditions	Notes
		Min.	Max.				
Maximum frequency (sinewave input)	f_{MAX}	1·0		GHz	SP8605B	Input = 400-1200mV p-p	5
		1·3		GHz	SP8606B	Input = 400-1200mV p-p	5
Minimum frequency (sinewave input)	f_{MIN}		150	MHz	All	Input = 600-1200mV p-p	3
Current consumption	I_{EE}		100	mA	All	V_{EE} = −5·45V, outputs unloaded	4
Output low voltage	V_{OL}	−1·92	−1·62	V	All	V_{EE} = −5·2V, R_L = 430 (25°C)	
Output high voltage	V_{OH}	−0·93	−0·75	V	All	V_{EE} = −5·2V, R_L = 430 (25°C)	
Minimum output swing	V_{OUT}	500		mV	All	V_{EE} = −5·2V, R_L = 430	4

NOTES
1. The temperature coefficients of V_{OH} = +1·2mV/°C, and V_{OL} = +0·24mV/°C but these are not tested.
2. The test configuration for dynamic testing is shown in Fig.5.
3. Tested at 25°C and +70°C only.
4. Tested at 25°C only
5. Tested at +70°C only.

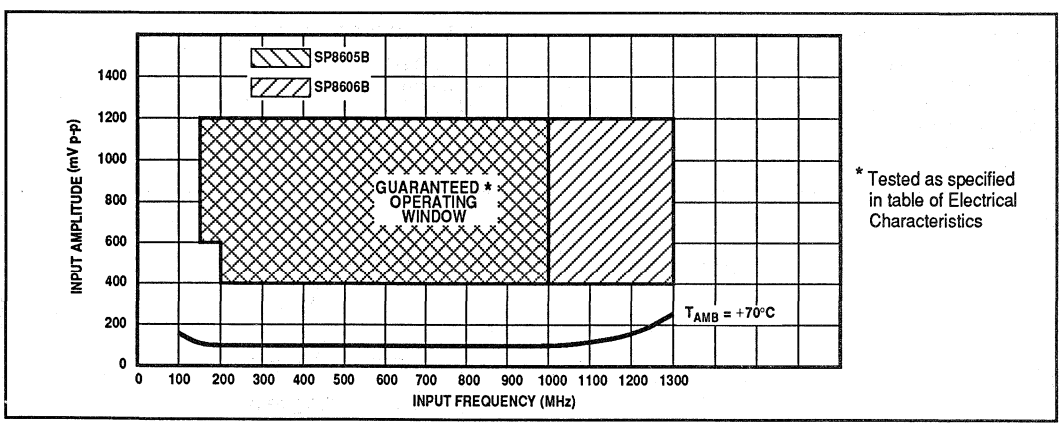


Fig. 3 Typical input characteristics of SP8605B and SP8606B

THERMAL CHARACTERISTICS

θ_{JC} approximately 30°C/W
θ_{JA} approximately 110°C/W

OPERATING NOTES

1. The clock input (pin 4) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 6, to ground.
2. In the absence of a signal the device will self-oscillate. If this is undesirable, it may be prevented by connecting a 10k resistor from the unused input to V_{EE} i.e. from pin 4 to pin 7. This will reduce the input sensitivity by approximately 100mV.
3. The circuit will operate at very low input frequencies but slew rate must be better than 200V/µs.
4. The input impedance of the SP8605/6 is a function of frequency, see Fig. 4.
5. The emitter follower outputs require external load resistors. These should not be less than 330 and a value of 430 is recommended. Interfacing to ECLIII/10K is shown in Fig. 7.
6. These devices may be used with split suopply lines and ground referenced input; a suitable configuration is shown in Fig. 6.
7. All components should be suitable for the frequency in use.

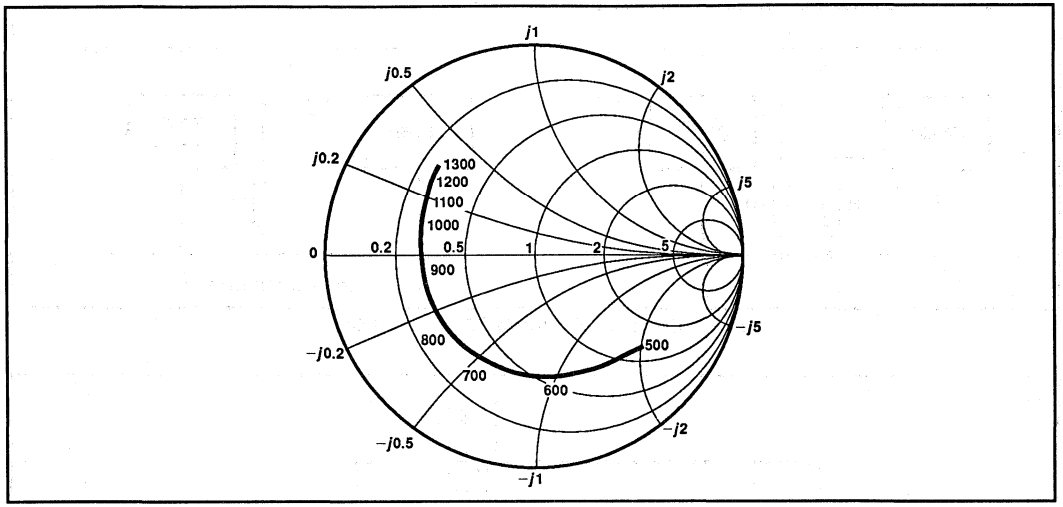


Fig. 4 Typical input impedance. Test conditions: supply voltage = −5·2V, ambient temperature = 25°C, frequencies in MHz, Impedances normalised to 50

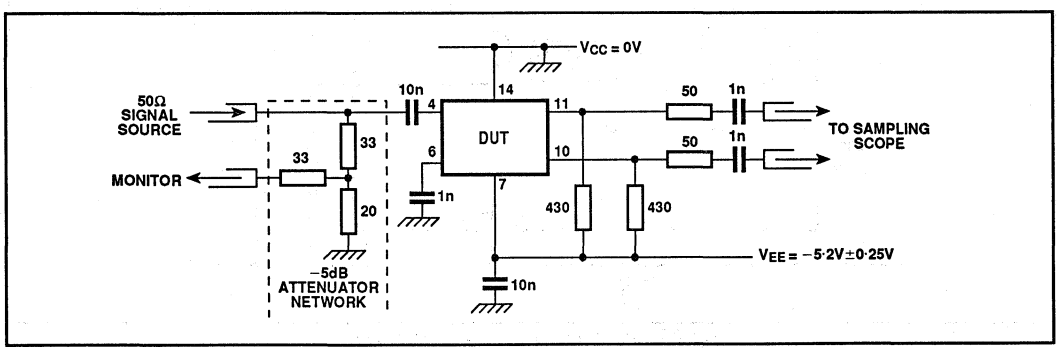


Fig. 5 Toggle frequency test circuit

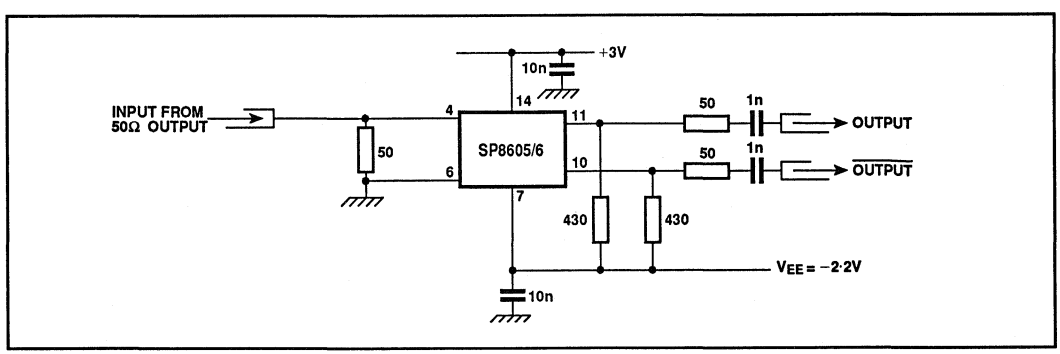


Fig. 6 Circuit for using the input signal about ground potential

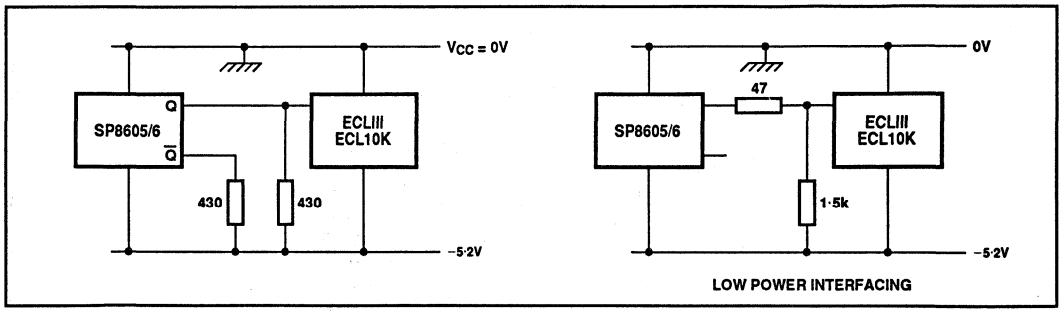


Fig. 7 Interfacing SP8605/6 to ECL10K and ECLIII

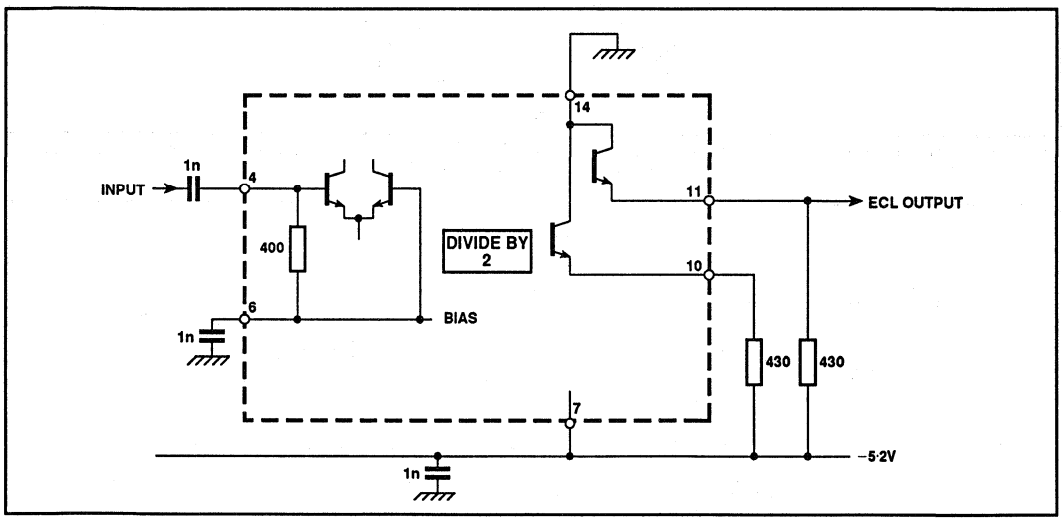


Fig. 8 Typical application showing interfacing

SP8607 600MHz÷2

The SP8607 is an emitter coupled logic divider which features ECL10K compatible outputs when used with external pulldown resistors. The inputs are AC coupled.

FEATURES

- ECL Compatible Outputs
- AC-Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: −5·2V
- Power Consumption: 80mW
- Temperature Range:
  −55°C to +125°C (A Grade)
  −30°C to +70°C (B Grade)

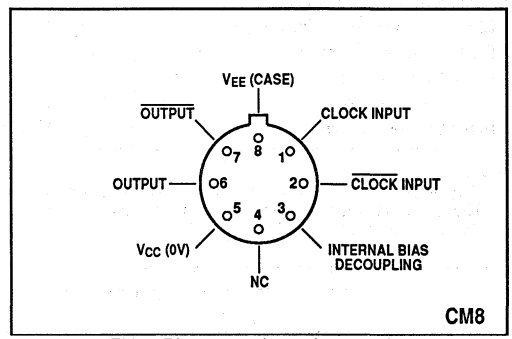


Fig. 1 Pin connections - bottom view

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{EE}	−8V
Output current	10mA
Storage temperature range	−65°C to +150°C
Max. junction temperature	+175°C
Max. clock input voltage	2·5V p-p

ORDERING INFORMATION

SP8607 A CM
SP8607 B CM
SP8607 AC CM

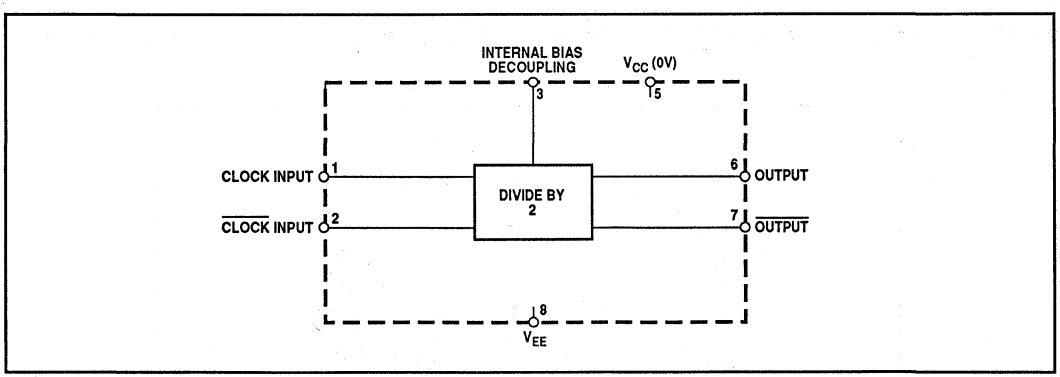


Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range
Supply voltage, V_{CC} = 0V, V_{EE} = −5·2V ± 0·25V
Temperature, T_{AMB} = −55°C to +125°C (A Grade), −30°C to +70°C (B Grade)

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{MAX}	600		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f_{MIN}		40	MHz	Input = 400-800mV p-p	
Power supply current	I_{EE}		18	mA	V_{EE} = −5·2V, outputs unloaded	
Output low voltage	V_{OL}	−1·8	−1·4	V	V_{EE} = −5·2V	3
Output high voltage	V_{OH}	−0·85	−0·7	V	V_{EE} = −5·2V	3
Minimum output swing	V_{OUT}	400		mV	V_{EE} = −5·2V	

NOTES
1. The temperature coefficients of V_{OH} = +1·63mV/°C, and V_{OL} = +0·34mV/°C but these are not tested.
2. The test configuration for dynamic testing is shown in Fig.5.
3. Tested at 25°C only.

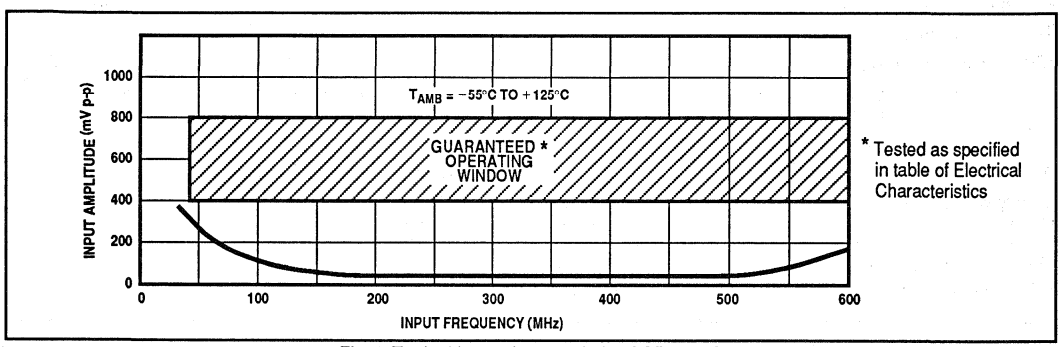


Fig. 3 Typical input characteristic of SP8607A

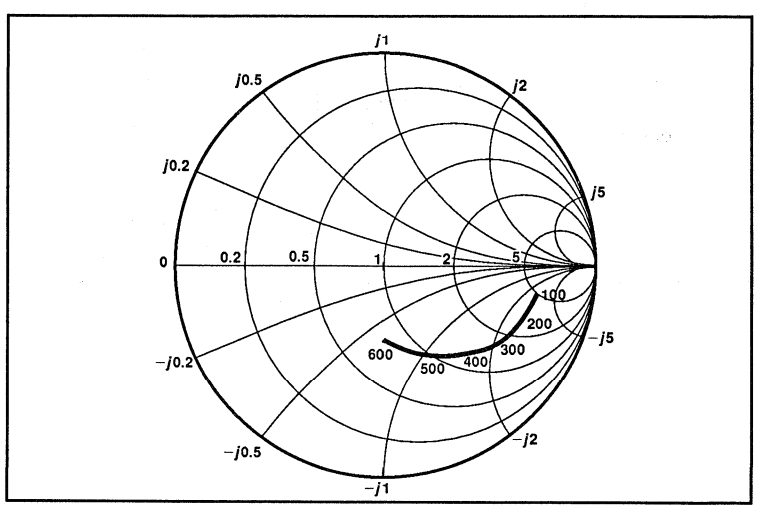


Fig. 4 Typical input impedance. Test conditions: supply voltage = −5·2V, ambient temperature = 25°C, frequencies in MHz, Impedances normalised to 50Ω

OPERATING NOTES

1. The clock inputs (pins 1 and 2) can be driven single ended or differentially and should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 3, to ground.
2. In the absence of a signal the device will self-oscillate. If this is undesirable, it may be prevented by connecting a 15kΩ resistor from the unused input to V_{EE}. This will reduce the input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/µs.
4. The outputs are compatible with ECLII. There is an internal load of 4kΩ on each output. The outputs can be interfaced to ECL10K by the addition of 1·5kΩ pulldown resistors from the outputs to V_{EE} to increase output voltage swing.
5. Input impedance is a function of frequency, See Fig. 4.
6. All components should be suitable for the frequency in use.

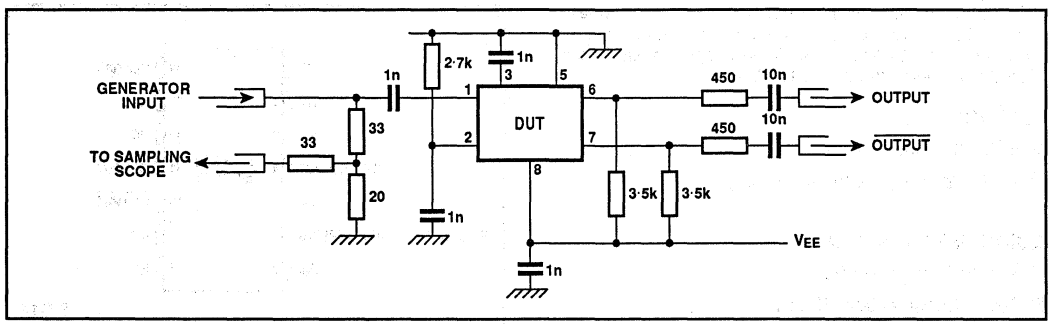


Fig. 5 Test circuit

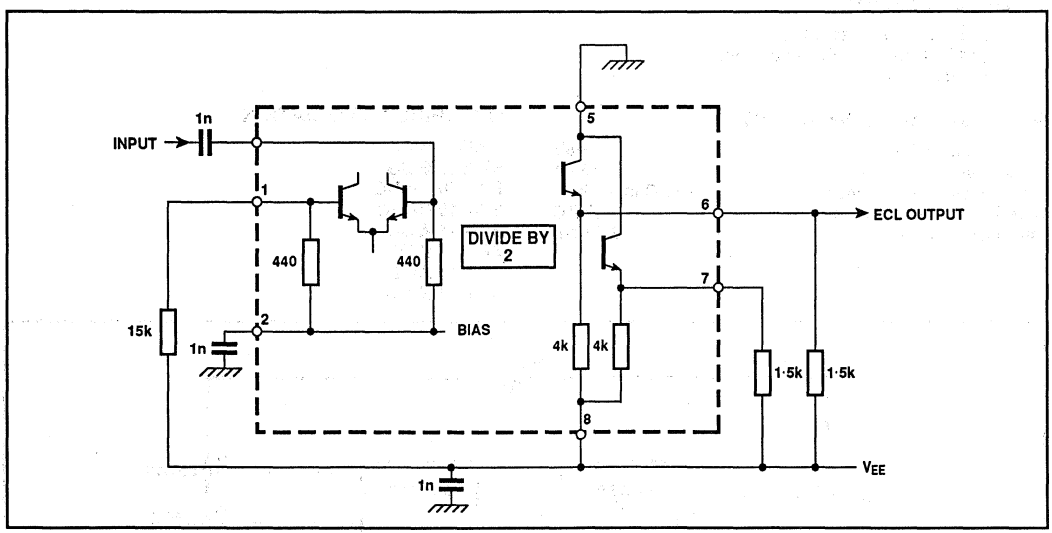


Fig. 6 Typical application showing interfacing

SP8610 1000MHz÷4
SP8611 1300/1500MHz÷4

The SP8610 and SP8611 are asynchronous ECL divide by four circuits with ECL compatible outputs which can also be used to drive 100Ω lines. They feature input sensitivities of 600mV p-p (800mV p-p above 1300MHz).

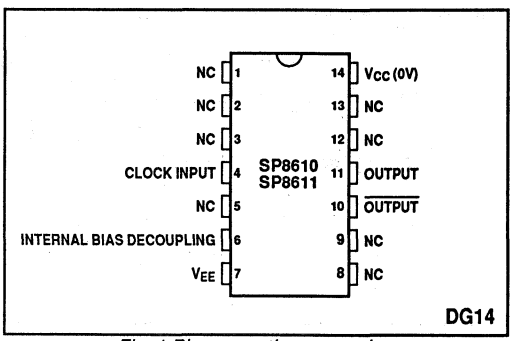


Fig. 1 Pin connections - top view

FEATURES

- ECL Compatible Outputs
- AC-Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: −5·2V
- Power Consumption: 380mW
- Max. Input Frequency: 1500MHz (SP8611B)
- Temperature Range:

  A Grade: −55°C to +110°C
  (+125°C with suitable heat sink)
  B Grade: 0°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{EE}	−8V
Output current	15mA
Storage temperature range	−65°C to +150°C
Max. junction temperature	+175°C
Max. clock input voltage	2·5V p-p

ORDERING INFORMATION

SP8610 A DG
SP8610 B DG
SP8610 AA DG
SP8610 NA 1C
SP8611 A DG
SP8611 B DG
SP8611 AA DG
SP8611 NA 1C

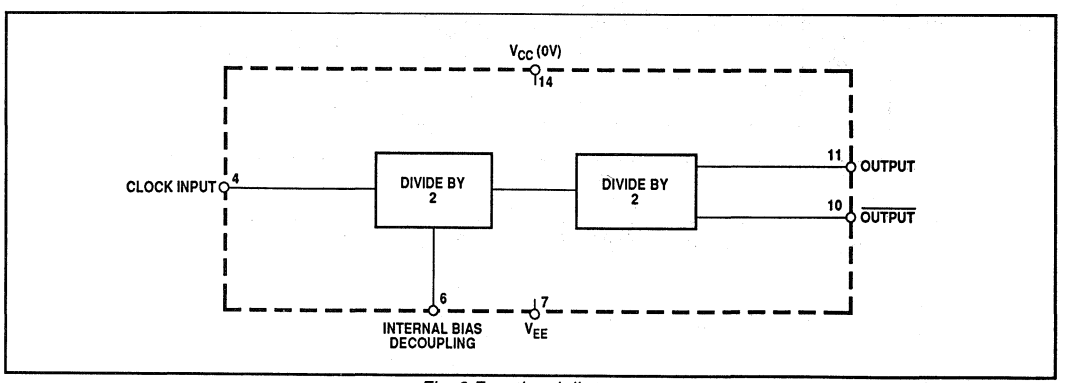


Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range
Supply voltage, V_{CC} = 0V, V_{EE} = −5·2V ± 0·25V
Temperature, T_{AMB} = −55°C to +125°C (A Grade) (Note 1), 0°C to +70°C (B Grade)

Characteristic	Symbol	Value		Units	Type	Conditions	Notes
		Min.	Max.				
Maximum frequency (sinewave input)	f_{MAX}	1·0		GHz	SP8605A,B	Input = 400-1200mV p-p	6
		1·3		GHz	SP8606A	Input = 800-1200mV p-p	6
		1·5		GHz	SP8606B	Input = 400-1200mV p-p	6
Minimum frequency (sinewave input)	f_{MIN}		150	MHz	All	Input = 600-1200mV p-p	4
Current consumption	I_{EE}		100	mA	All	V_{EE} = −5·45V, outputs unloaded	5
Output low voltage	V_{OL}	−1·92	−1·62	V	All	V_{EE} = −5·2V, R_L = 430Ω (25°C)	
Output high voltage	V_{OH}	−0·93	−0·75	V	All	V_{EE} = −5·2V, R_L = 430Ω (25°C)	
Minimum output swing	V_{OUT}	500		mV	All	V_{EE} = −5·2V, R_L = 430Ω	5

NOTES
1. The A Grade devices must be used with a heat sink to maintain chip temperature below +150°C when operating in a T_{AMB} of +125°C.
2. The temperature coefficients of V_{OH} = +1·2mV/°C, and V_{OL} = +0·24mV/°C but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.5.
4. Tested at 25°C and +125°C only (+70°C for B grade).
5. Tested at 25°C only
6. Tested at +125°C only (+70°C for B grade).

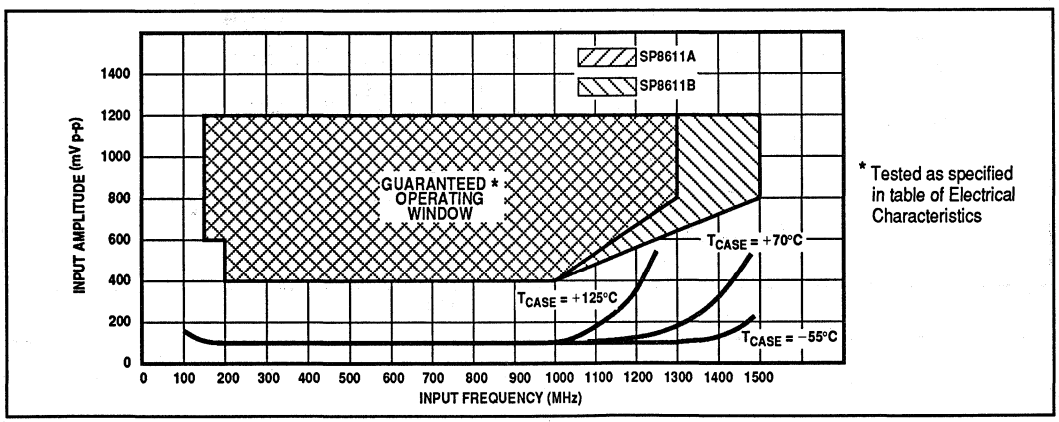


Fig. 3 Typical input characteristic of SP8611

THERMAL CHARACTERISTICS

θ_{JC} approximately 30°C/W
θ_{JA} approximately 110°C/W

OPERATING NOTES

1. The clock input (pin 4) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 6, to ground.
2. In the absence of a signal the device will self-oscillate. If this is undesirable, it may be prevented by connecting a 10kΩ resistor from the unused input to V_{EE} i.e. from pin 4 to pin 7. This will reduce the input sensitivity by approximately 100mV.
3. The circuit will operate at very low input frequencies but slew rate must be better than 200V/µs.
4. The input impedance of the SP8610/11 is a function of frequency, see Fig. 4.
5. The emitter follower outputs require external load resistors. These should not be less than 330Ω and a value of 430Ω is recommended. Interfacing to ECLIII/10K is shown in Fig. 7.
6. These devices may be used with split supply lines and ground referenced input; a suitable configuration is shown in Fig. 6.
7. All components should be suitable for the frequency in use.

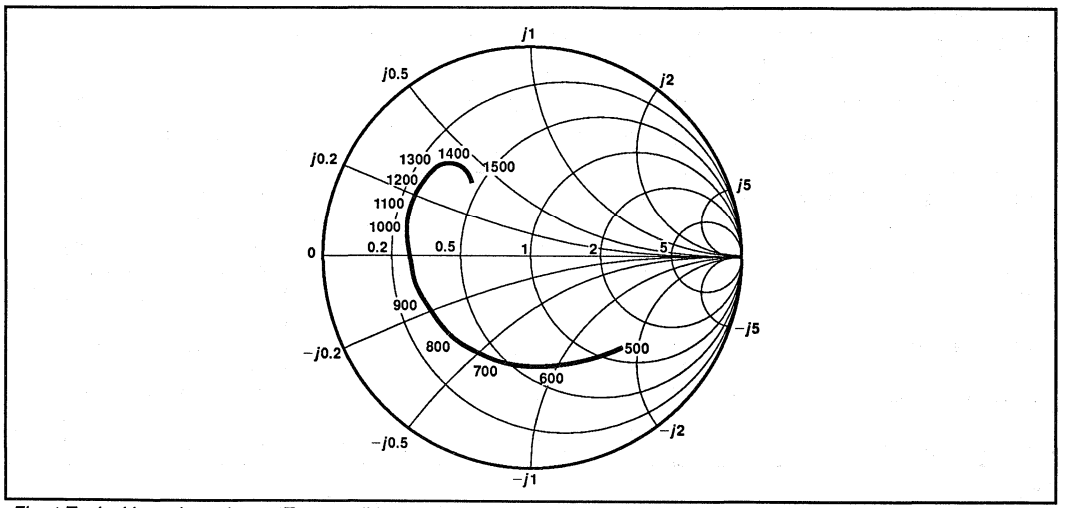


Fig. 4 Typical input impedance. Test conditions: supply voltage = −5·2V, ambient temperature = 25°C, frequencies in MHz, Impedances normalised to 50Ω

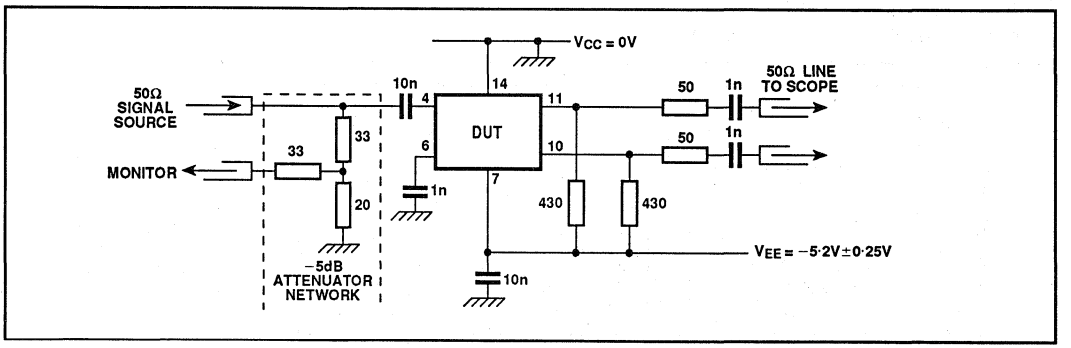


Fig. 5 Toggle frequency test circuit

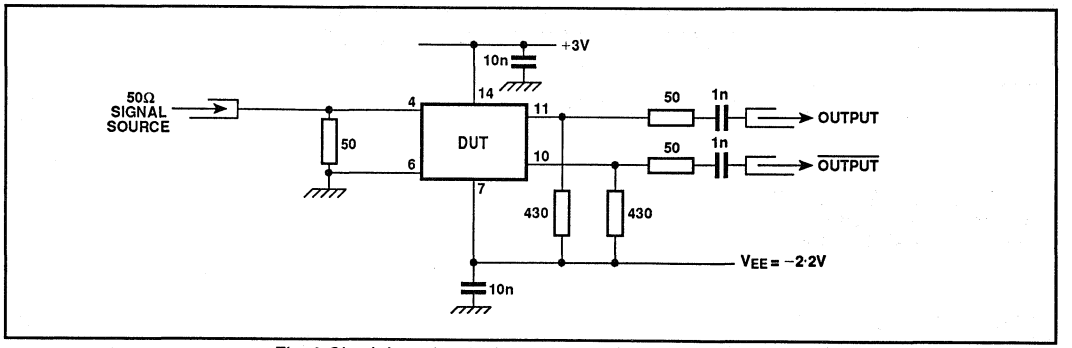


Fig. 6 Circuit for using the input signal about ground potential

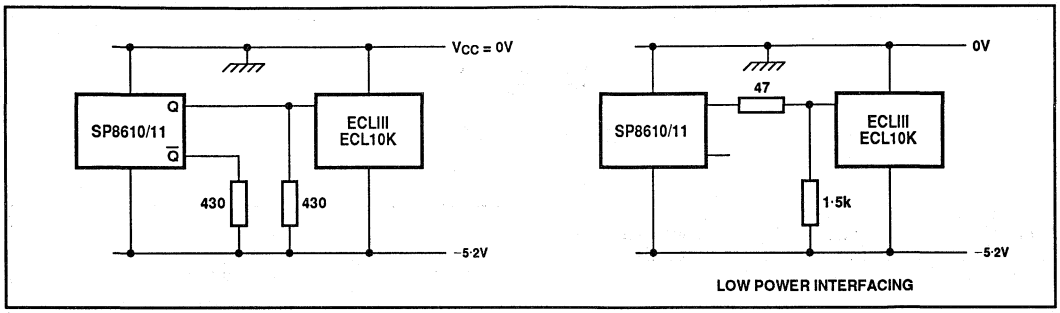


Fig. 7 Interfacing SP8610/11 to ECL10K and ECLIII

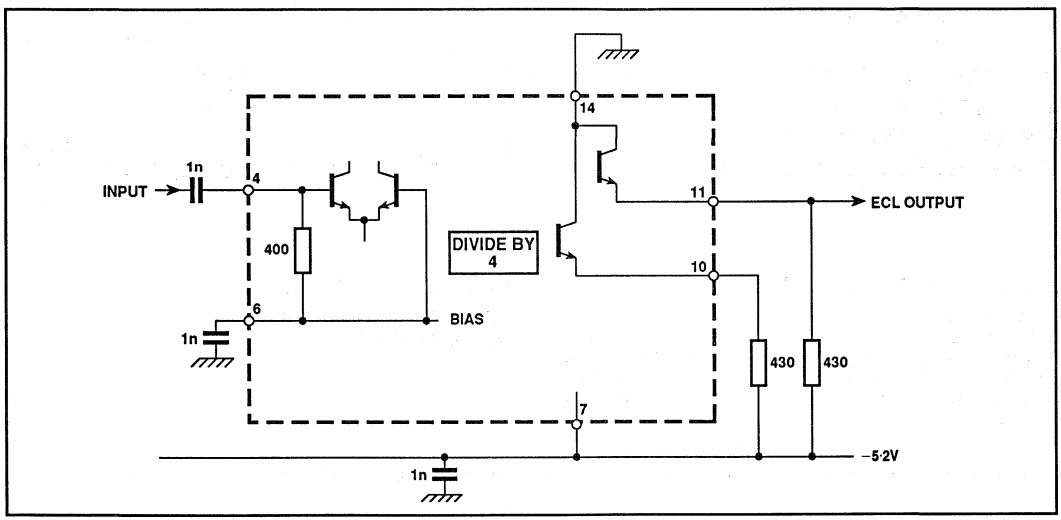


Fig. 8 Typical application showing interfacing

SP8630

600MHz÷10

The SP8630 is an asynchronous emitter coupled logic divider which provides an ECLIII/10K compatible output when used with an external pulldown resistor. It requires an AC coupled input of 600mV p-p.

FEATURES

- ECL Compatible Outputs
- AC-Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: −5·2V
- Power Consumption: 350mW
- Temperature Range: −30°C to +70°C

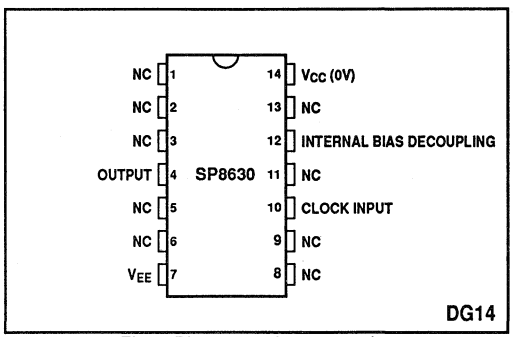


Fig. 1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{EE}	−8V
Output current	15mA
Storage temperature range	−65°C to +150°C
Max. junction temperature	+175°C
Max. clock input voltage	2·5V p-p

ORDERING INFORMATION

SP8630 B DG
5962-92003 (SMD)

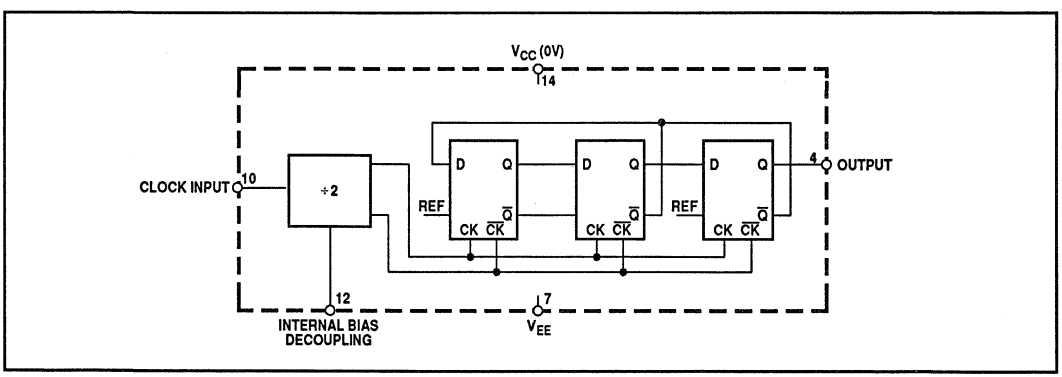


Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range
Supply voltage, V_{CC} = 0V, V_{EE} = −5·2V ± 0·25V
Temperature, T_{AMB} = −30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{MAX}	600		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f_{MIN}		40	MHz	Input = 400-800mV p-p	
Power supply current	I_{EE}		70	mA	V_{EE} = −5·2V	
Output low voltage	V_{OL}	−1·8	−1·5	V	V_{EE} = −5·2V	3
Output high voltage	V_{OH}	−0·85	−0·7	V	V_{EE} = −5·2V	3
Minimum output swing	V_{OUT}	400		mV	V_{EE} = −5·2V	

NOTES
1. The temperature coefficients of V_{OH} = +1·63mV/°C, and V_{OL} = +0·94mV/°C but these are not tested.
2. The test configuration for dynamic testing is shown in Fig.5.
3. Tested at 25°C only.

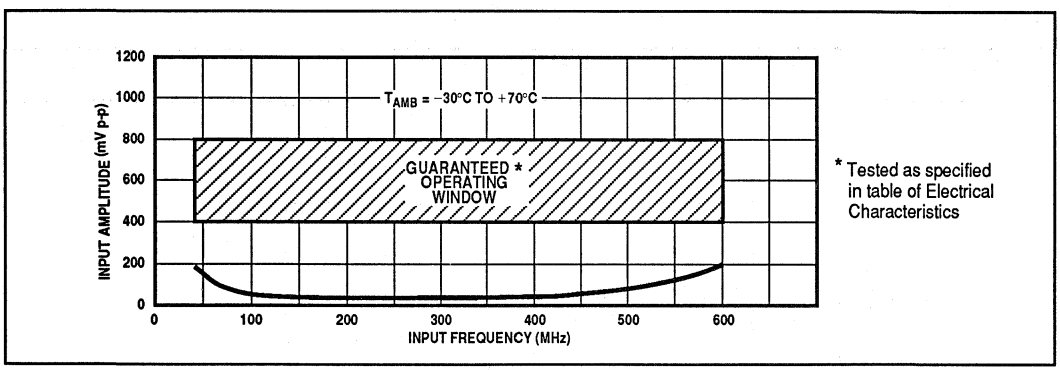


Fig. 3 Typical input characteristic

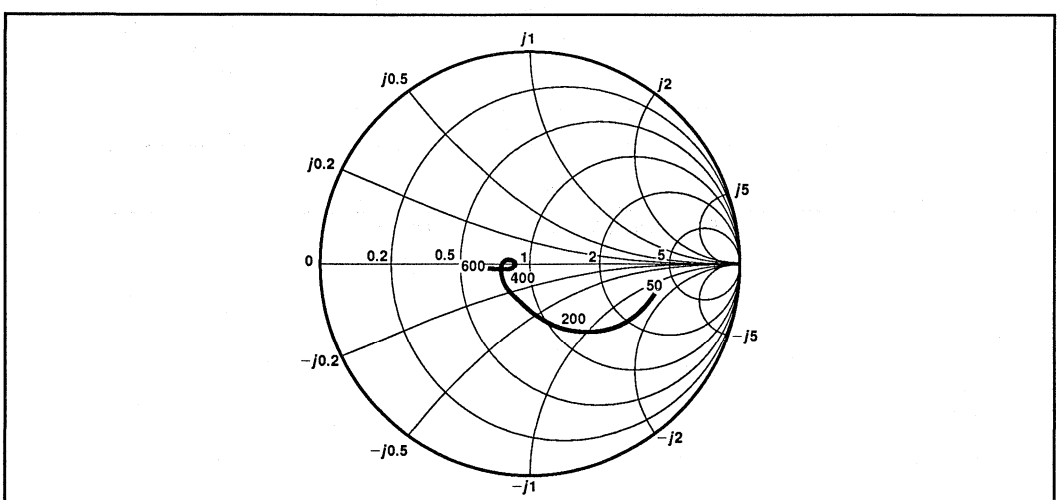


Fig. 4 Typical input impedance. Test conditions: supply voltage = −5·2V, ambient temperature = 25°C, frequencies in MHz, Impedances normalised to 50Ω

OPERATING NOTES

1. The clock input (pin 10) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 12, to ground.
2. The circuit will operate down to DC but slew rate must be better than 100V/μs.
3. The output is compatible with ECLII. There is an internal load of 3kΩ at the output. The output can be interfaced to ECLIII/10K by the addition of 1·5kΩ to the output to increase the output voltage swing.
4. Input impedance is a function of frequency, see Fig. 4.
5. All components should be suitable for the frequency in use.

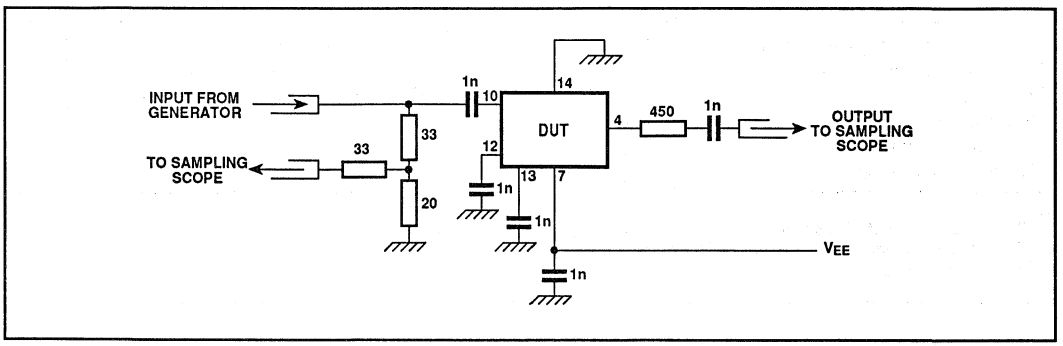


Fig. 5 Test circuit

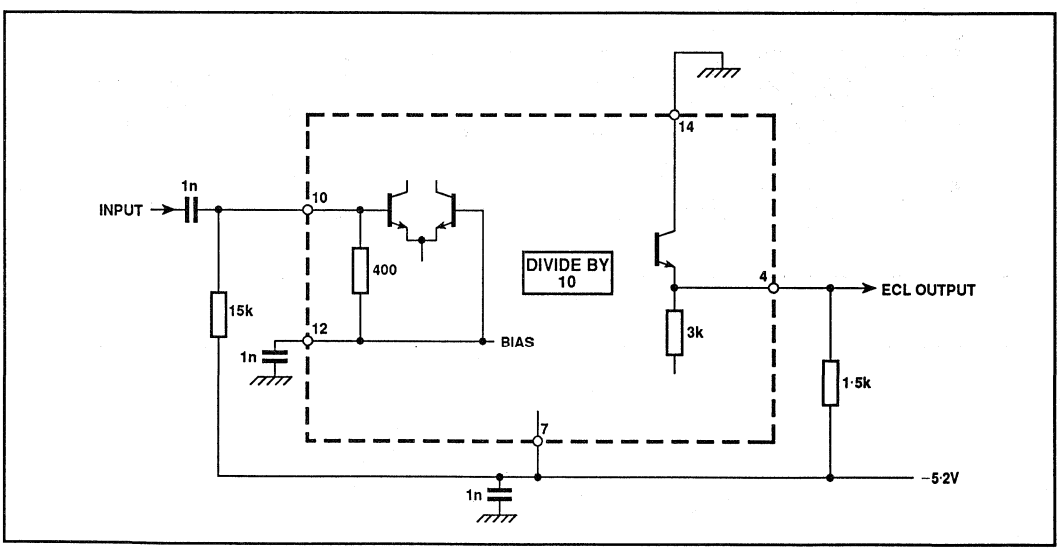


Fig. 6 Typical application showing interfacing

SP8647

250MHz÷10/11

The SP8647 is an ECL variable modulus divider, with ECL10K and TTL/CMOS compatible outputs. It divides by 10 when either of the ECL control inputs, $\overline{PE1}$ or $\overline{PE2}$, is in the high state and by 11 when both are low (or open circuit).

The two clock inputs are interchangeable and either will act as a clock inhibit when connected to an ECL high level. Normally, one input is left open circuit and the other is AC-coupled, with externally applied bias.

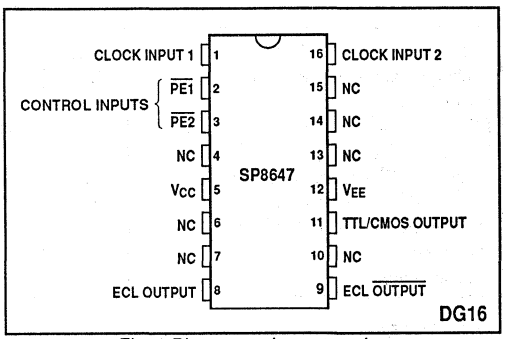


Fig. 1 Pin connections - top view

FEATURES

- ECL Compatible Inputs/Outputs
- Open Collector TTL/CMOS Output
- AC-Coupled Input (External Bias)

QUICK REFERENCE DATA

- Supply Voltage: −5·2V±0·25V (ECL), 5·0V±0·25V (TTL)
- Power Consumption: 260mW
- Temperature Range: −30°C to +70°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage, $\|V_{CC}-V_{EE}\|$	8V
Output current	20mA
Storage temperature range	−65°C to +150°C
Max. junction temperature	+175°C
Open collector voltage (pin 11)	+12V
Max. clock input voltage	2·5V p-p
Max. open collector current	15mA

ORDERING INFORMATION

SP8647 B DG
5962-90618 (SMD)

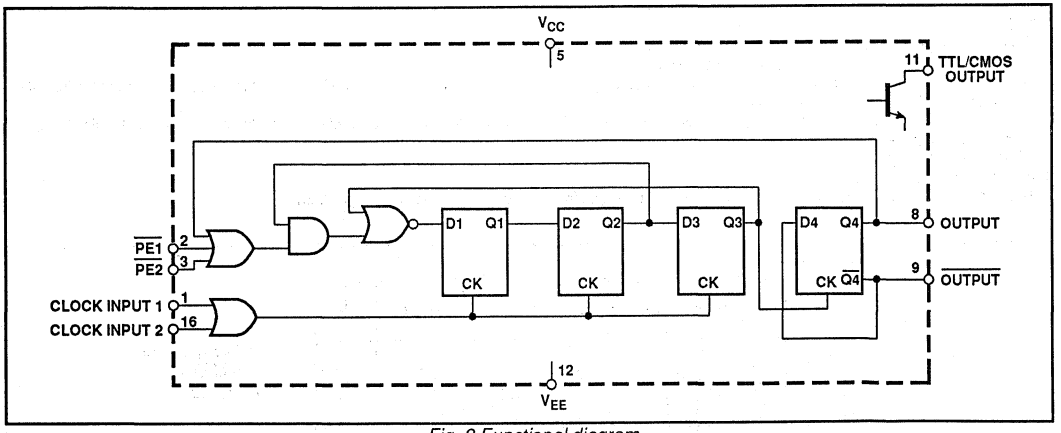


Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range

ECL OPERATION

Supply voltage, V_{CC} = 0V, V_{EE} = −5·2V ± 0·25V
Temperature, T_{AMB} = −30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{MAX}	250		MHz	Input = 400-800mV p-p	5
Minimum frequency (sinewave input)	f_{MIN}		50	MHz	Input = 400-800mV p-p	5
Power supply current	I_{EE}		65	mA	V_{EE} = −5·2V	5
ECL output high voltage	V_{OH}	−0·85	−0·7	V	V_{EE} = −5·2V (25°C)	
ECL output low voltage	V_{OL}	−1·8	−1·5	V	V_{EE} = −5·2V (25°C)	
Clock and $\overline{PE}$ input high voltage	V_{INH}	−0·93		V	V_{EE} = −5·2V (25°C)	
Clock and $\overline{PE}$ input low voltage	V_{INL}		−1·62	V	V_{EE} = −5·2V (25°C)	
Clock to ECL output delay	t_p		6	ns		6
Set-up time	t_s	2·5		ns		3, 6
Release time	t_r	3		ns		4, 6

TTL OPERATION

Supply voltage, V_{CC} = 5V ± 0·25V, V_{EE} = 0V
Temperature, T_{AMB} = −30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{MAX}	250		MHz	Input = 400-800mV p-p	5
Minimum frequency (sinewave input)	f_{MIN}		50	MHz	Input = 400-800mV p-p	5
Power supply current	I_{EE}		65	mA		5
TTL output low voltage	V_{OL}		0·5	V	V_{CC} = 5·25V, sink current = 8mA	5, 7
TTL output high voltage	V_{OH}	3·5		V	V_{CC} = 5·0V	5, 7
Clock to TTL output high delay, +ve going	t_{PLH}		15	ns		6
Clock to TTL output low delay, −ve going	t_{PHL}		15	ns		6
Set-up time	t_s	2·5		ns		3, 6
Release time	t_r	3		ns		4, 6

NOTES
1. The temperature coefficients of V_{OH} = +1·63mV/°C, V_{OL} = +0·94mV/°C and of V_{IN} = +1·22mV/°C.
2. The test configuration for dynamic testing is shown in Fig.6.
3. The set-up time t_s is defined as the minimum time that can elapse between L→H transition of control input and the next L→H clock pulse transition to ensure that the ÷10 mode is obtained.
4. The release time t_r is defined as the minimum time that can elapse between H→L transition of control input and the next L→H clock pulse transition to ensure that the ÷11 mode is obtained.
5. Tested at 25°C only.
6. Guaranteed but not tested.
7. The open collector output is not recommended for use at output frequencies above 15MHz. $C_{LOAD} \leq 5pF$.

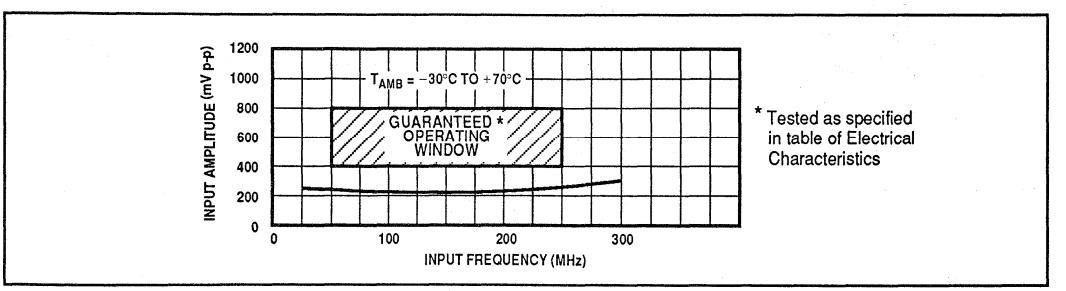
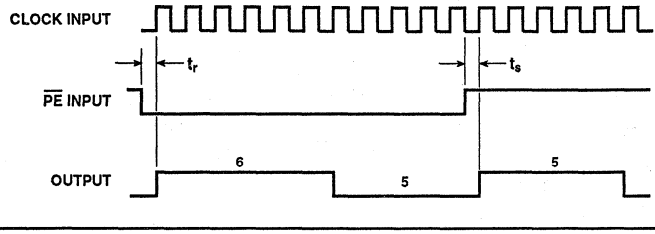


Fig. 3 Typical input characteristic



TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division ratio
L	L	11
H	L	10
L	H	10
H	H	10

Fig. 4 Timing diagram

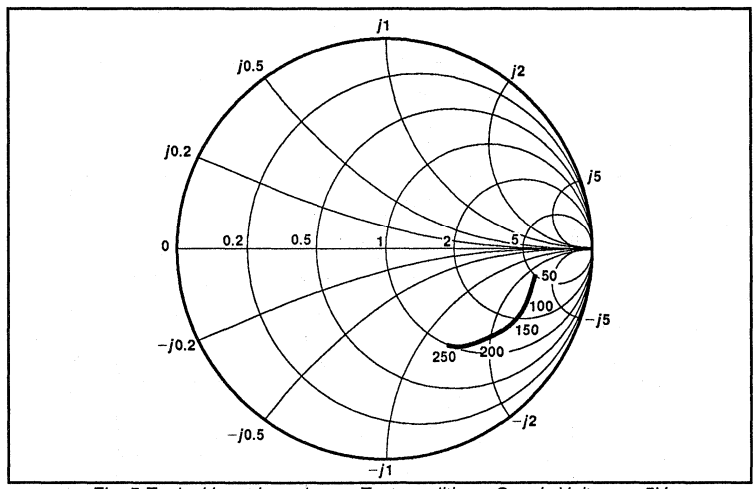


Fig. 5 Typical input impedance. Test conditions: Supply Voltage = 5V, Ambient Temperature = 25°C. Frequencies in MHz, impedances normalised to 50Ω.

OPERATING NOTES

1. The clock and control inputs are ECLIII compatible. There is an internal pulldown resistor to V_{EE} of 4·3kΩ on each input and therefore any unused input can be left open circuit. If it is desirable to capacitively couple the signal source to the clock then an external bias is required as shown in Fig. 6. The external bias voltage should be −1·3V at 25°C.
2. The outputs are compatible with ECLII but can be interfaced to ECL10K as shown in Fig.8.
3. The circuit will operate down to DC but slew rate must be better than 100V/μs.
4. Input impedance is a function of frequency. See Fig. 5.
5. The TTL/CMOS output is a free collector, with an output rise/fall time which is a function of load resistance and load capacitance. The load capacitance should therefore be kept to a minimum and the load resistance should not be too small otherwise V_{OL} will be too great. For example, TTL output current = 8mA, V_{OL} = 0·5V. For CMOS outputs, the value of load resistor should be the maximum consistent with satisfactory rise times.
6. All components should be suitable for the frequency in use.

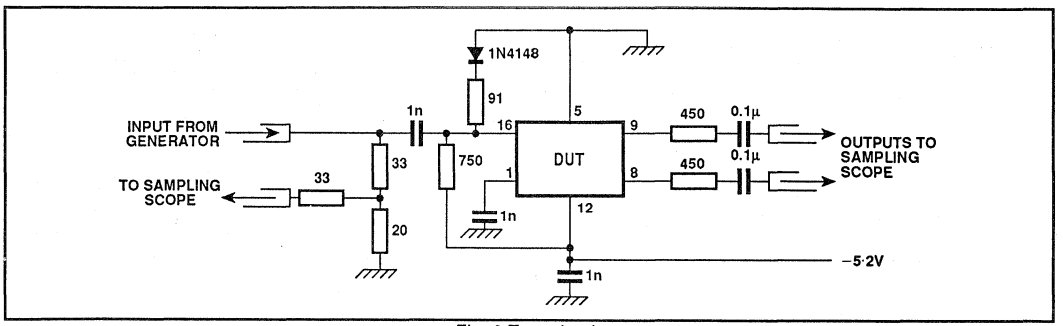


Fig. 6 Test circuit

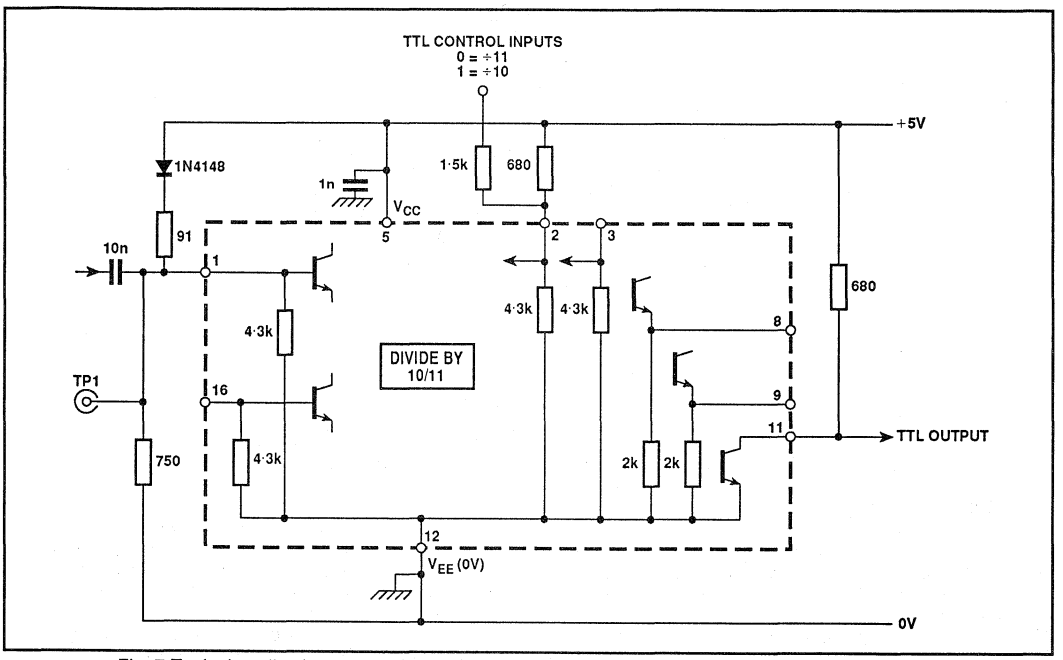


Fig. 7 Typical application showing TTL interfacing. NB: Voltage at TP1 should be +3·75V at 25°C.

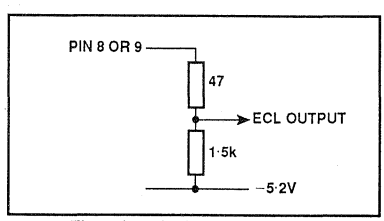


Fig. 8 Interfacing to ECL10K

SP8655A 200MHz÷32, SP8657A 200MHz÷20, SP8659B 200MHz÷16

The SP8655A, SP8657A and SP8659B are low power ECL counters with open collector output capable of driving TTL or CMOS and have internally biased inputs.

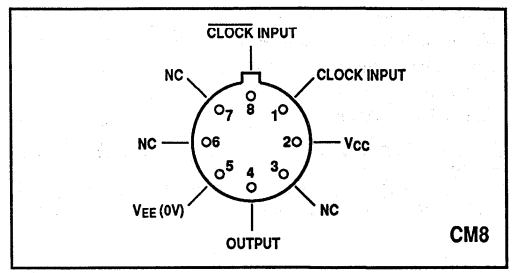


Fig. 1 Pin connections - bottom view

FEATURES

- AC Coupled Inputs
- Low Power Consumption
- CMOS/TTL Compatible Open Collector Output

QUICK REFERENCE DATA

- Supply Voltage: 5·0V
- Power Consumption: 50mW
- Temperature Range: −55°C to +125°C (SP8655A, SP8657A)
  −30°C to +70°C (SP8659B)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Open collector output voltage	12V
Storage temperature range	−65°C to +150°C
Max. junction temperature	+175°C
Max. clock input voltage	2·5V p-p
Output sink current	10mA

ORDERING INFORMATION

SP8655 A CM
SP8657 A CM
SP8659 B CM

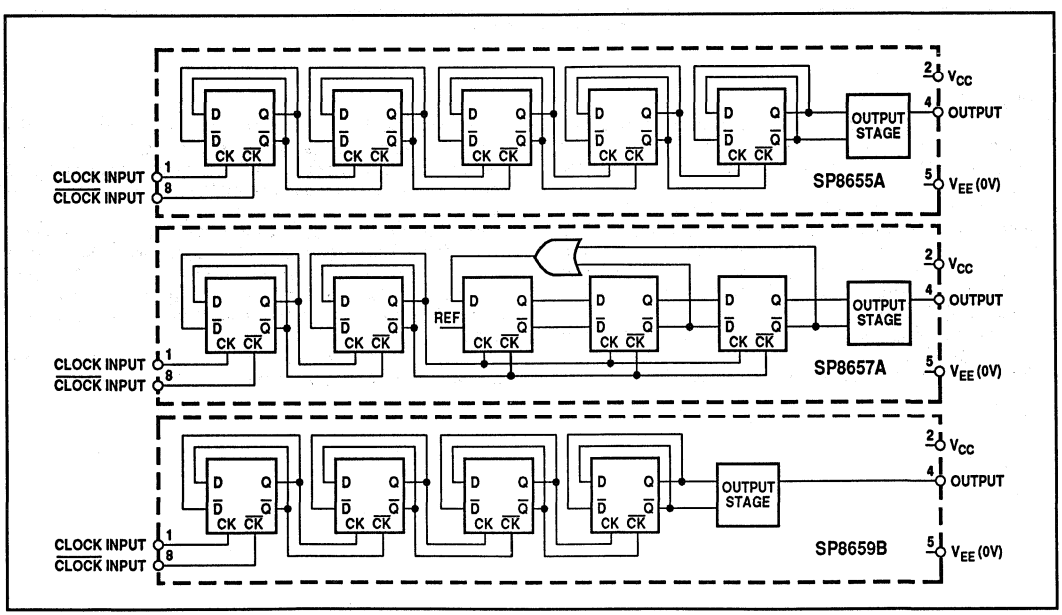


Fig. 2 Functional diagrams

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range
Supply voltage, V_{CC} = 5·0V±0·25V, V_{EE} = 0V
Temperature, T_{AMB} = −55°C to +125°C (SP8655A, SP8657A), −30°C to +70°C (SP8659B)

Characteristic	Symbol	Value		Units	Conditions
		Min.	Max.		
Maximum frequency (sinewave input)	f_{MAX}	200		MHz	Input = 400-800mV p-p
Minimum frequency (sinewave input)	f_{MIN}		40	MHz	Input = 400-800mV p-p
Power supply current	I_{CC}		13	mA	
Output high voltage	V_{OH}	7·5		V	V_{CC} = 5V, C_{LOAD}≤5pF, pin 4 = 1·5kΩ to 10V
Output low voltage	V_{OL}		0·45	V	V_{CC} = 5V, pin 4 = 1·5kΩ to 10V

NOTES
1. The test configuration for dynamic testing is shown in Fig.5.
2. Above characteristics are not tested at 25°C (tested at low and high temperatures only).

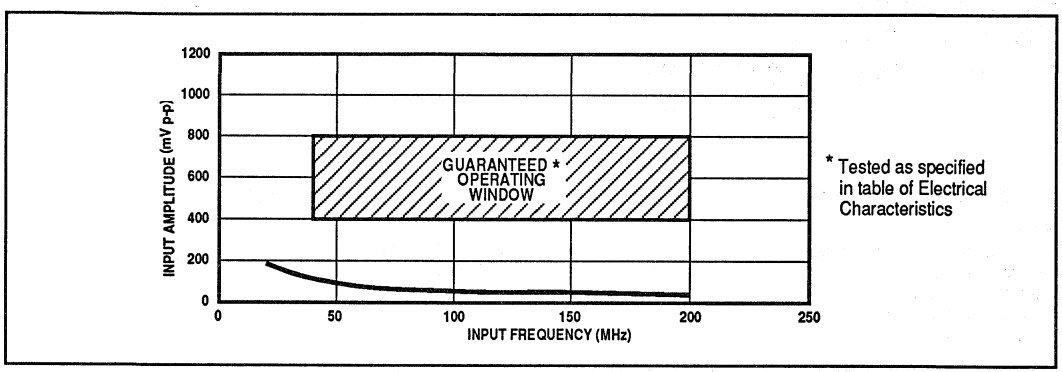


Fig. 3 Typical input characteristic

OPERATING NOTES

1.The clock inputs (pins 1 and 8) should be capacitively coupled to the signal source. When driven single ended, the input signal path is completed by a capacitor from the unused input to ground.
2. In the absence of a signal the devices will self-oscillate. This can be prevented by connecting a 39kΩ resistor from either input to ground. If the device is driven single ended, it is recommended that the pull-down resistor be connected to the decoupled unused input. There will be a loss in sensitivity of approximately 200mV.
3. The device will operate down to DC but input slew rate must be better than 100V/µs.
4. The open collector output will drive three TTL loads, and therefore requires a a suitable resistor to V_{CC} to maintain noise immunity. In order to maintain noise immunity on transitions, this resistor should not exceed 4·7kΩ For interfacing to CMOS, the open collector may be restored to a +10V line via a 3·3kΩ resistor.
5. Input impedance varies as a function of frequency; see Fig. 4.
6. The rise time of the open collector output waveform is directly proportional to the load capacitance and load resistor value. Therefore, the load capacitance should be minimised and the load resistor kept to a minimum compatible with system power requirements.

In the test configuration of Fig. 5, the output rise time is approximately 20ns and the fall time is typically 10ns.

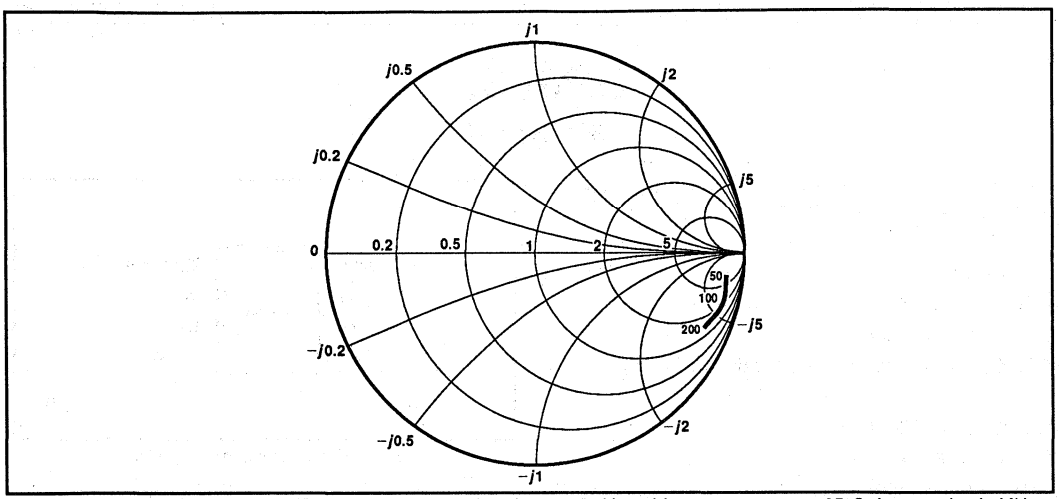


Fig. 4 Typical input impedance. Test conditions: supply voltage = 5·0V, ambient temperature = 25°C, frequencies in MHz, Impedances normalised to 50Ω

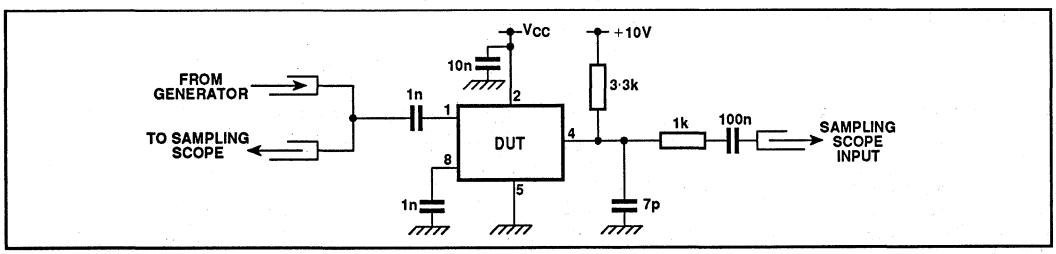


Fig. 5 Test circuit

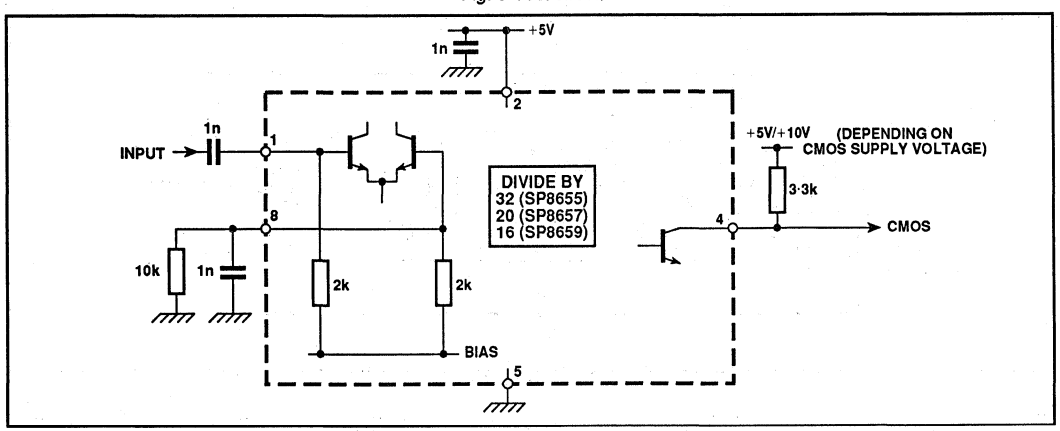


Fig. 6. Typical application circuit showing interfacing

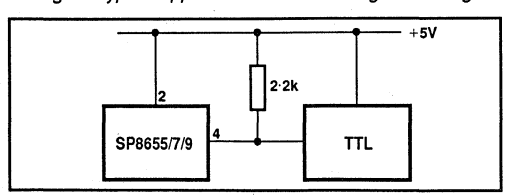


Fig. 7. Interfacing to TTL. Load not to exceed 3 TTL unit loads

SP8660

150MHz÷10

The SP8660 is a low power ECL counter with an open collector output capable of driving TTL or CMOS. It has internally biased inputs.

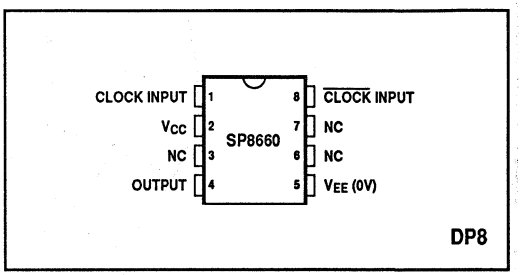


Fig. 1 Pin connections - top view

FEATURES

- AC Coupled Inputs
- Low Power Consumption
- CMOS/TTL Compatible Open Collector Output

QUICK REFERENCE DATA

- Supply Voltage: 5·0V
- Power Consumption: 50mW
- Temperature Range: −30°C to +70°C
- 8-Lead Plastic Package

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Open collector output voltage	12V
Storage temperature range	−55°C to +150°C
Max. junction temperature	+150°C
Max. clock input voltage	2·5V p-p
Output sink current	10mA

ORDERING INFORMATION

SP8660 DP

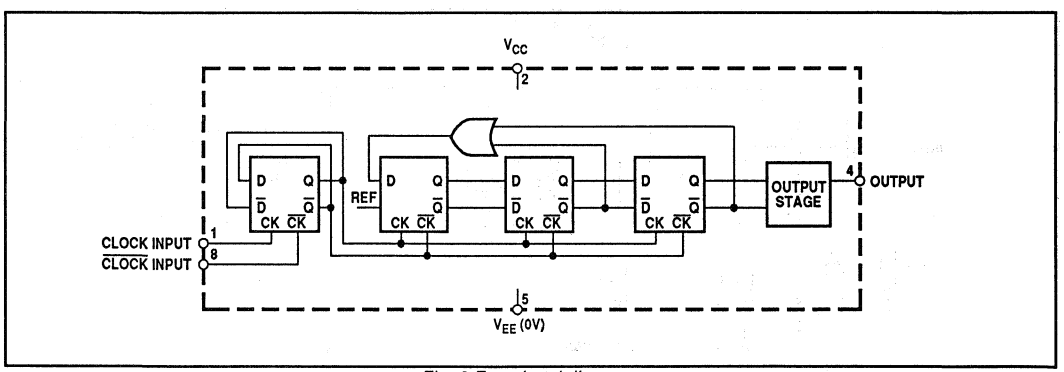


Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range
Supply voltage, V_{CC} = 5·0V±0·25V, V_{EE} = 0V
Temperature, T_{AMB} = −30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions
		Min.	Max.		
Maximum frequency (sinewave input)	f_{MAX}	150		MHz	Input = 200-1000mV p-p
Minimum frequency (sinewave input)	f_{MIN}		40	MHz	Input = 400-1000mV p-p
Power supply current	I_{CC}		13	mA	V_{CC} = 5·25V
Output high voltage	V_{OH}	9		V	V_{CC} = 5V, pin 4 = 1·5kΩ to 10V, see note 3
Output low voltage	V_{OL}		400	mV	V_{CC} = 5V, pin 4 = 1·5kΩ to 10V, see note 3

NOTES
1. The test configuration for dynamic testing is shown in Fig.5.
2. All characteristics above are tested at 25°C only.
3. C_{LOAD} ∂ 5pF.

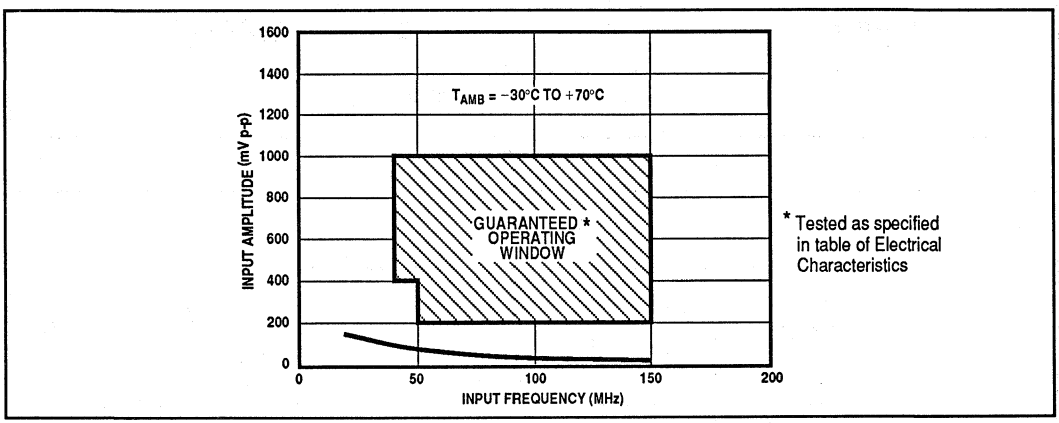


Fig. 3 Typical input characteristic

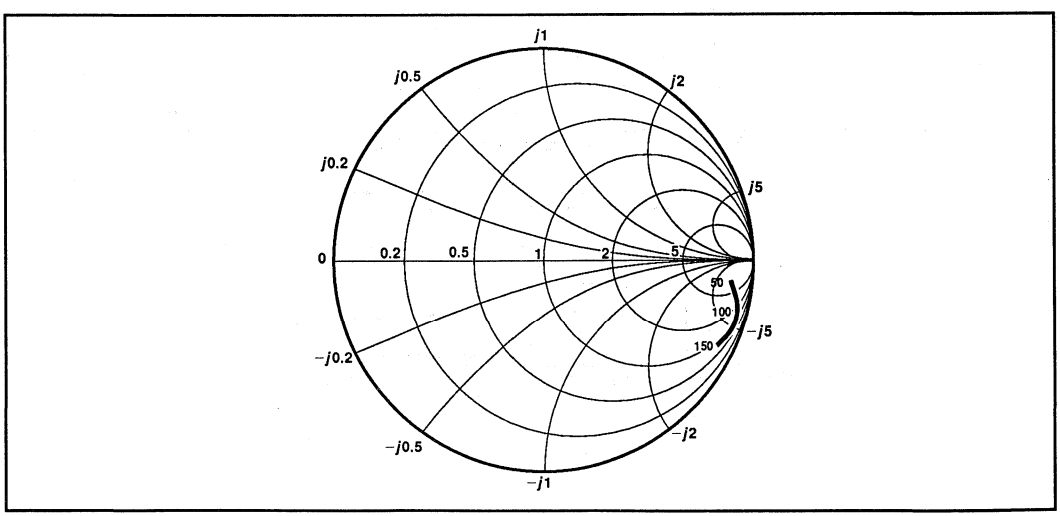


Fig. 4 Typical input impedance. Test conditions: supply voltage = 5·0V, ambient temperature = 25°C, frequencies in MHz, Impedances normalised to 50Ω

OPERATING NOTES

1.The clock inputs (pins 1 and 8) should be capacitively coupled to the signal source. When driven single ended, the input signal path is completed by a capacitor from the unused input to ground.
2. In the absence of a signal the devices will self-oscillate. This can be prevented by connecting a 39kΩ resistor from either input to ground. If the device is driven single ended, it is recommended that the pull-down resistor be connected to the decoupled unused input. There will be a loss in sensitivity of approximately 200mV.
3. The device will operate down to DC but input slew rate must be better than 100V/μs.
4. The open collector output will drive three TTL loads, and therefore requires a a suitable resistor to V_{CC} to maintain noise immunity. In order to maintain noise immunity on transitions, this resistor should not exceed 4·7kΩ. For interfacing to CMOS, the open collector may be restored to a +10V line via a 3·3kΩresistor. The output sink current must not exceed 10mA and the use of too low a value of resistor may lead to a loss of noise immunity, especially at low temperatures.
5. Input impedance varies as a function of frequency; see Fig. 4.
6. The rise time of the open collector output waveform is directly proportional to the load capacitance and load resistor value. Therefore, the load capacitance should be minimised and the load resistor kept to a minimum compatible with system power requirements.

In the test configuration of Fig. 5, the output rise time is approximately 20ns and the fall time is typically 10ns.

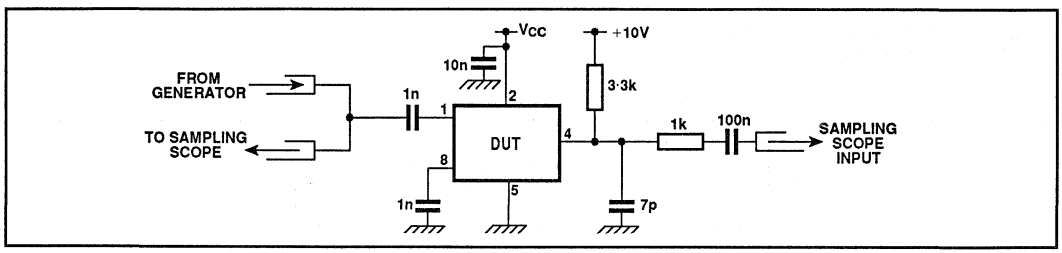


Fig. 5 Test circuit

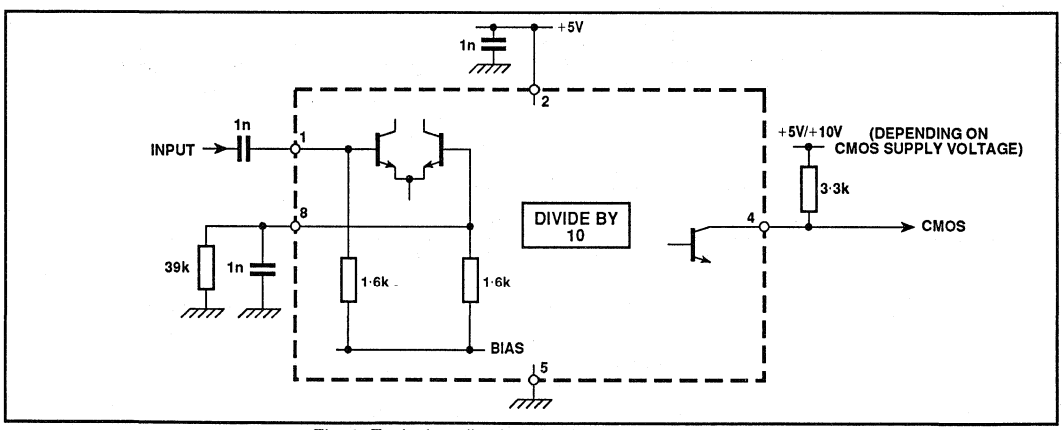


Fig. 6. Typical application circuit showing interfacing

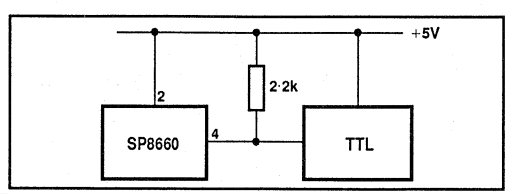


Fig. 7. Interfacing to TTL. Load not to exceed 3 TTL unit loads

SP8660A

150MHz÷10

The SP8660A is a low power ECL counter with an open collector output capable of driving TTL or CMOS.The device has internally biased inputs.

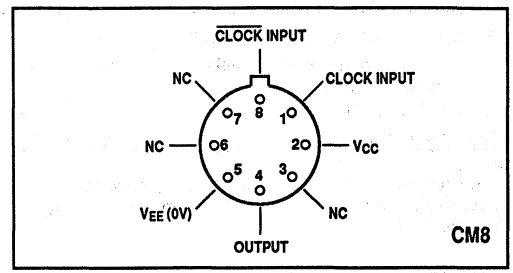


Fig. 1 Pin connections - bottom view

FEATURES

- AC Coupled Inputs
- Low Power Consumption
- CMOS/TTL Compatible Open Collector Output

QUICK REFERENCE DATA

- Supply Voltage: 5·0V
- Power Consumption: 50mW
- Temperature Range: −55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Open collector output voltage	12V
Storage temperature range	−65°C to +150°C
Max. junction temperature	+175°C
Max. clock input voltage	2·5V p-p
Output sink current	10mA

ORDERING INFORMATION

SP8660 A CM

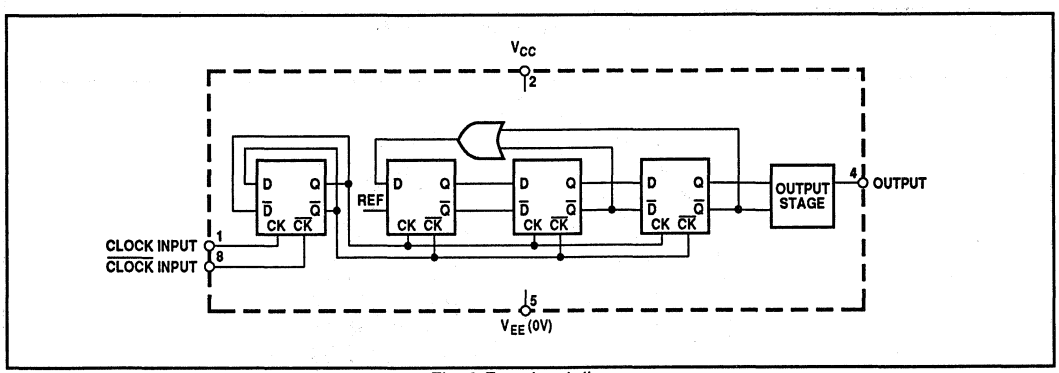


Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range
Supply voltage, V_{CC} = 5·0V±0·25V, V_{EE} = 0V
Temperature, T_{AMB} = −55°C to +125°C

Characteristic	Symbol	Value		Units	Conditions
		Min.	Max.		
Maximum frequency (sinewave input)	f_{MAX}	150		MHz	Input = 400-800mV p-p
Minimum frequency (sinewave input)	f_{MIN}		40	MHz	Input = 400-800mV p-p
Power supply current	I_{CC}		13	mA	V_{CC} = 5·25V
Output high voltage	V_{OH}	7·5		V	V_{CC} = 5V, pin 4 = 1·5kΩ to 10V, see note 3
Output low voltage	V_{OL}		400	mV	V_{CC} = 5V, pin 4 = 1·5kΩ to 10V

NOTES
1. The test configuration for dynamic testing is shown in Fig.5.
2. Above characteristics are not tested at 25°C. Tested at high and low temperatures only.
3. $C_{LOAD} \leq 5pF$.

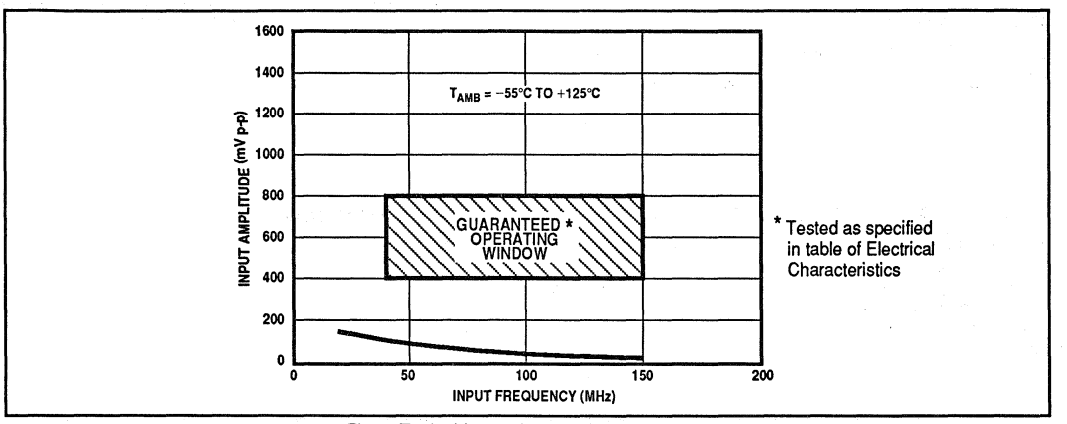


Fig. 3 Typical input characteristic, SP8660A

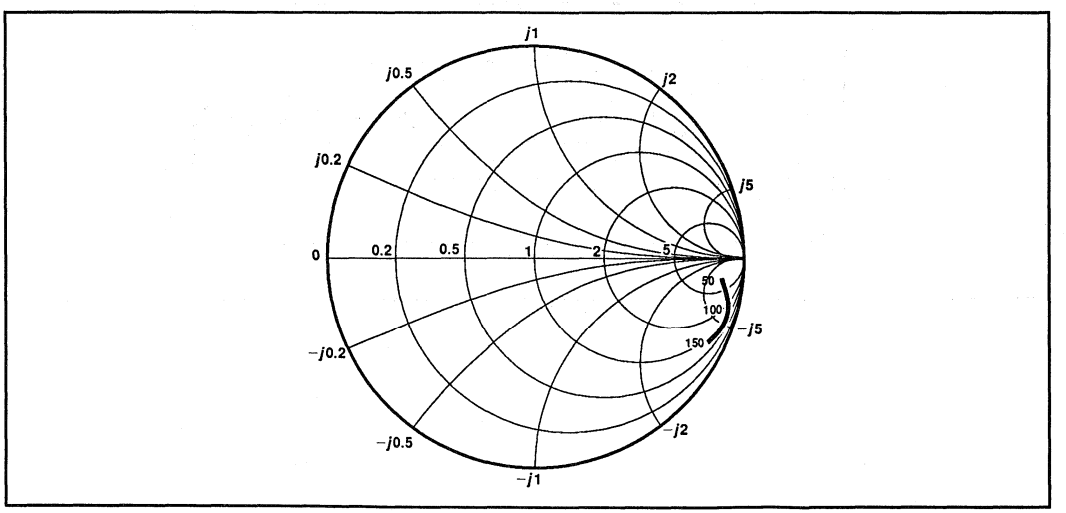


Fig. 4 Typical input impedance. Test conditions: supply voltage = 5·0V, ambient temperature = 25°C, frequencies in MHz, Impedances normalised to 50Ω

OPERATING NOTES

1. The clock inputs (pins 1 and 8) should be capacitively coupled to the signal source. When driven single ended, the input signal path is completed by a capacitor from the unused input to ground.
2. In the absence of a signal the devices will self-oscillate. This can be prevented by connecting a 39kΩ resistor from either input to ground. If the device is driven single ended, it is recommended that the pull-down resistor be connected to the decoupled unused input. There will be a loss in sensitivity of approximately 200mV.
3. The device will operate down to DC but input slew rate must be better than 100V/μs.
4. The open collector output will drive three TTL loads, and therefore requires a a suitable resistor to V_{CC} to maintain noise immunity. In order to maintain noise immunity on transitions, this resistor should not exceed 4·7kΩ. For interfacing to CMOS, the open collector may be restored to a +10V line via a 3·3kΩ resistor. The output sink current must not exceed 10mA and the use of too low a value of resistor may lead to a loss of noise immunity, especially at low temperatures.
5. Input impedance varies as a function of frequency; see Fig. 4.
6. The rise time of the open collector output waveform is directly proportional to the load capacitance and load resistor value. Therefore, the load capacitance should be minimised and the load resistor kept to a minimum compatible with system power requirements.

In the test configuration of Fig. 5, the output rise time is approximately 20ns and the fall time is typically 10ns.

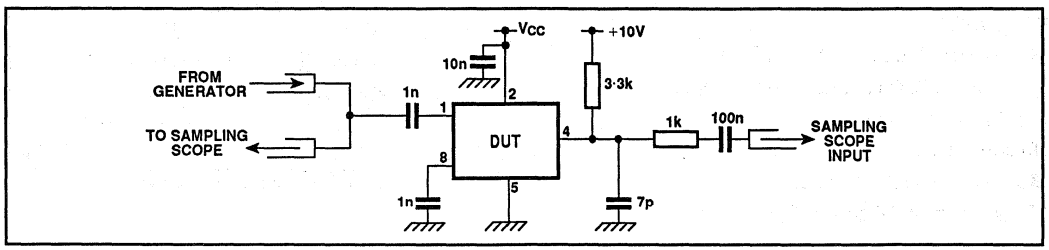


Fig. 5 Test circuit

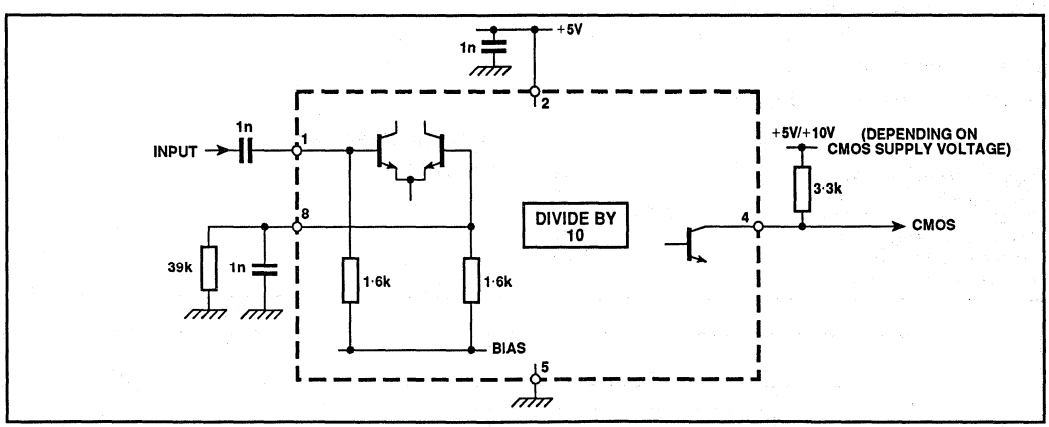


Fig. 6. Typical application circuit showing interfacing

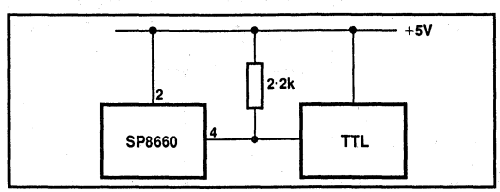


Fig. 7. Interfacing to TTL. Load not to exceed 3 TTL unit loads

SP8680A

550MHz÷10/11

The SP8680A is an ECL variable modulus divider, with ECL and TTL compatible outputs. The circuit can operate from either ECL or TTL supplies. It divides by 10 when either of the ECL control inputs, $\overline{PE1}$ or $\overline{PE2}$, is in the high state and by 11 when both are low (or open circuit). The divider can be set asynchronously to the eleventh state by applying a high level to the master set (MS) input.

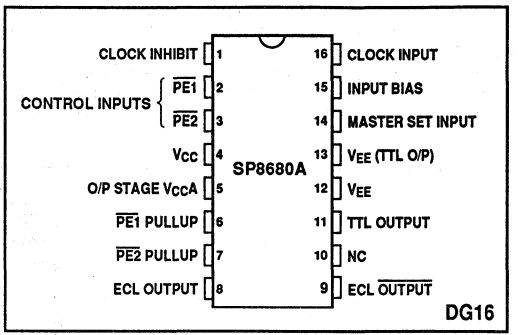


Fig. 1 Pin connections - top view

FEATURES

- Very High Speed – 650MHz (Typ.)
- ECL and TTL Compatible Inputs/Outputs
- DC or AC Clocking
- Clock Inhibit
- Asynchronous Master Set
- Equivalent to Fairchild 11C90

QUICK REFERENCE DATA

- Supply Voltage: −4·75V to −5·5V (ECL), 4·75V to 5·5V (TTL)
- Power Consumption: 420mW
- Temperature Range: −55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage, $\lvert V_{CC}-V_{EE}\rvert$	8V
ECL output source current	50mA
Storage temperature range	−65°C to +150°C
Max. junction temperature	+175°C
TTL output sink current	30mA
Max. clock input voltage	2·5V p-p

ORDERING INFORMATION

SP8680 A DG

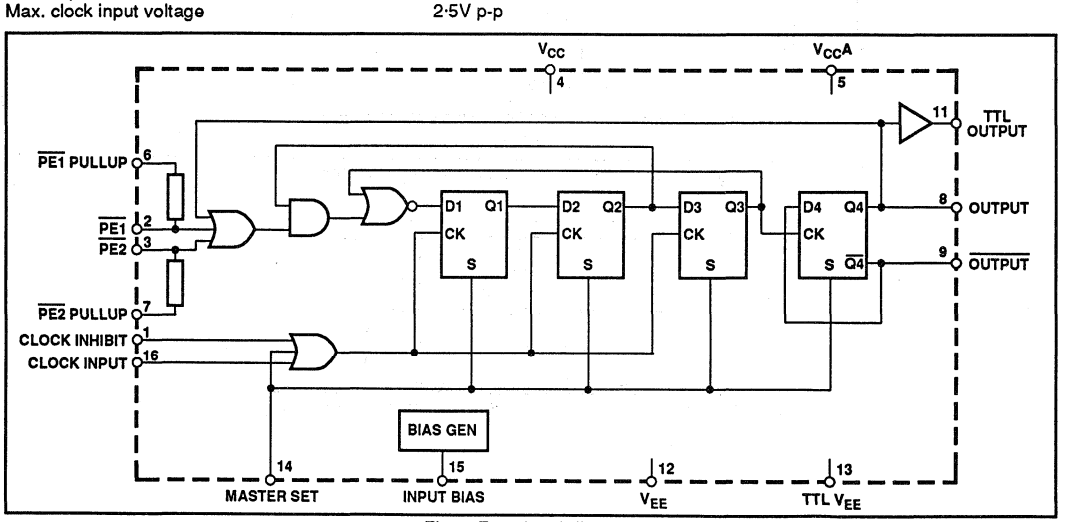


Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range

ECL OPERATION

Supply voltage, V_{EE} = −4·75V to − 5·5V, V_{CC} = 0V
Temperature, T_{AMB} = −55°C to +125°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{MAX}	550		MHz	AC coupled clock = 350mV p-p	5
Minimum frequency (sinewave input)	f_{MIN}		10	MHz	AC coupled clock = 600mV p-p	6
Power supply current	I_{EE}		105	mA	V_{EE} = −5·5V, pins 6, 7, 13 o/c	5
ECL output high voltage	V_{OH}	−0·93	−0·78	V	V_{EE} = −5·2V (25°C), R_L = 100Ω to −2V	
ECL output low voltage	V_{OL}	−1·85	−1·62	V	V_{EE} = −5·2V (25°C), R_L = 100Ω to −2V	
Input high voltage	V_{INH}	−0·095	−0·81	V	V_{EE} = −5·2V (25°C)	
Input low voltage	V_{INL}	−1·85	−1·475	V	V_{EE} = −5·2V (25°C)	
Input low currents	I_{IL}	0·5		µA	25°C	
Input high current, clock and MS	I_H		400	µA	V_{IN} = −1·85V (25°C)	
Input high current, $\overline{PE1}$ and $\overline{PE2}$	I_H		250	µA	V_{IN} = −0·8V (25°C)	
Propagation delay, clock to Q4 low	t_{pHL}		4	ns	R_L = 100Ω to −2V (25°C)	6
Propagation delay, clock to Q4 high	t_{pLH}		3	ns	R_L = 100Ω to −2V (25°C)	6
Propagation delay, MS to Q4 high	t_{pLH}		6	ns	25°C	6
Modulus control set-up time	t_s	4		ns	25°C	3, 6
Modulus control release time	t_r	4		ns	25°C	4, 6
ECL output rise time (20% - 80%)	t_{ELH}		2	ns	25°C	6
ECL output fall time (80% - 20%)	t_{EHL}		2	ns	25°C	6

TTL OPERATION

Supply voltage, V_{CC} = V_{CC}A = 4·75V to 5·5V, V_{EE} = 0V
Temperature, T_{AMB} = −55°C to +125°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{MAX}	550		MHz	AC coupled clock = 350mV p-p	5
Minimum frequency (sinewave input)	f_{MIN}		10	MHz	AC coupled clock = 600mV p-p	6
Power supply current	I_{CC}		111	mA	V_{CC} = 5·5V, pins 6, 7 o/c, pin 13 to pin 12	5
TTL output high voltage	V_{OH}	2·3		V	V_{CC} = 4·75V, I_{OH} = −640µA	5
TTL output low voltage	V_{OL}		0·5	V	V_{CC} = 5·5V, I_{OL} = −20µA	5
Input high voltage, $\overline{PE1}$ and $\overline{PE2}$	V_{INH}	3·9		V	V_{CC} = 5·0V (25°C)	
Input low voltage, $\overline{PE1}$ and $\overline{PE2}$	V_{INL}		3·5	V	V_{CC} = 5·0V (25°C)	
Input low current, $\overline{PE1}$ and $\overline{PE2}$	I_{IL}	−4		mA	V_{CC} = 5·5V (25°C), pins 6, 7 = V_{CC}, V_{IN} = 0·4V	
Propagation delay, clock to TTL low	t_{pHL}	6	14	ns	V_{CC} = 5·0V (25°C)	6
Propagation delay, clock to TTL high	t_{pLH}	6	14	ns	V_{CC} = 5·0V (25°C)	6
Propagation delay, MS to TTL high	t_p		17	ns	V_{CC} = 5·0V (25°C)	6
Modulus control set-up time	t_s	4		ns	V_{CC} = 5·0V (25°C)	3, 6
Modulus control release time	t_r	4		ns	V_{CC} = 5·0V (25°C)	4, 6
TTL output rise time (20% - 80%)	t_{TLH}		5	ns	V_{CC} = 5·0V (25°C)	6
TTL output fall time (80% - 20%)	t_{THL}		5	ns	V_{CC} = 5·0V (25°C)	6

NOTES

1. The temperature coefficients of V_{OH} = +1·2mV/°C, V_{OL} = +0·24mV/°C and of V_{IN} = +0·8mV/°C.
2. The test configuration for dynamic testing is shown in Fig.6.
3. The set-up time t_s is defined as the minimum time that can elapse between L→H transition of control input and the next L→H clock pulse transition to ensure that the ÷10 mode is obtained.
4. The release time t_r is defined as the minimum time that can elapse between H→L transition of control input and the next L→H clock pulse transition to ensure that the ÷11 mode is obtained.
5. Tested at +25°C and +125°C only.
6. Guaranteed but not tested.

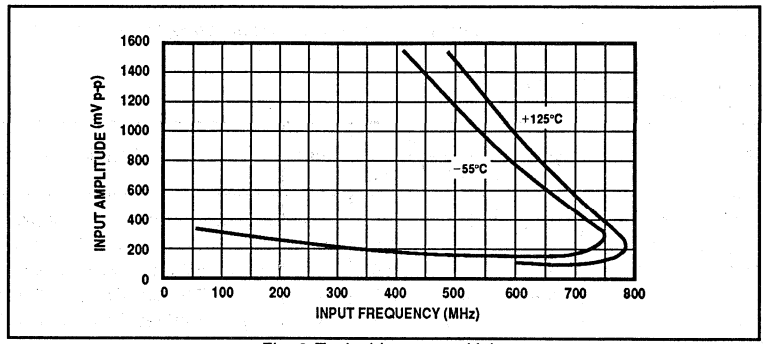
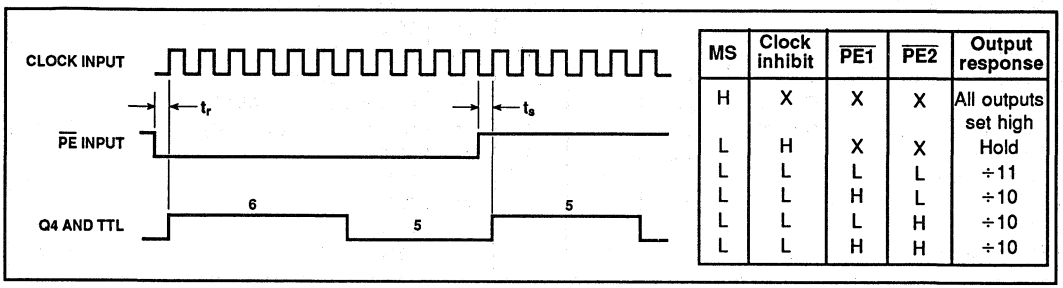


Fig. 3 Typical input sensitivity



MS	Clock inhibit	$\overline{PE1}$	$\overline{PE2}$	Output response
H	X	X	X	All outputs set high
L	H	X	X	Hold
L	L	L	L	÷11
L	L	H	L	÷10
L	L	L	H	÷10
L	L	H	H	÷10

Fig. 4 Truth table and timing diagram

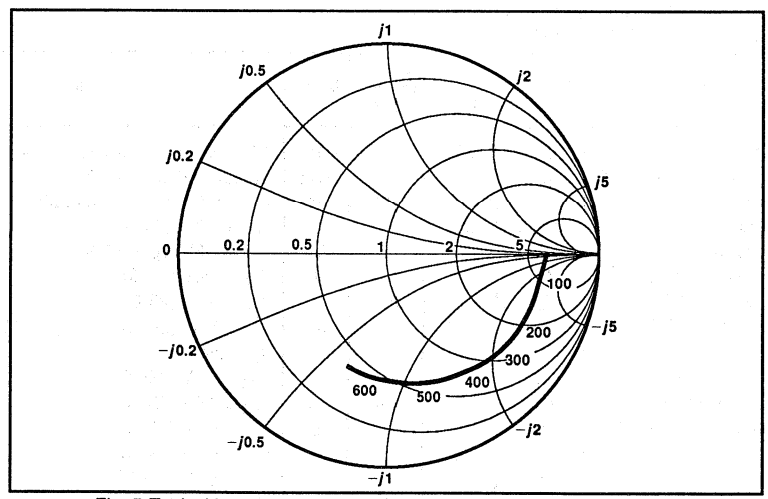


Fig. 5 Typical input impedance. Test conditions: Supply Voltage = 5V, Ambient Temperature = 25°C. Frequencies in MHz, impedances normalised to 50Ω.

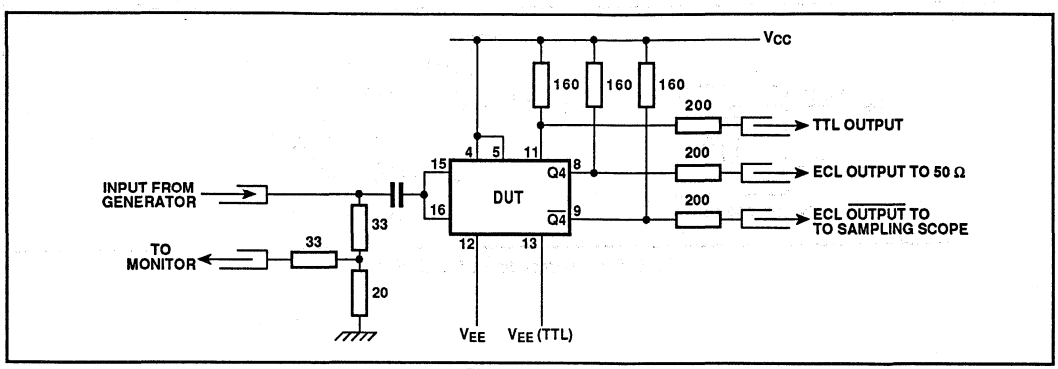


Fig. 6 Test circuit

OPERATING NOTES

1. The clock input, which is ECL10K compatible throughout the temperature range −55°C to +125°C, can also be coupled to TTL as shown in Fig. 9. The clock can also be capacitively coupled to the signal source (see Fig, 7). Connecting the internally-generated bias voltage to the clock input i.e., pin 15 to pin 16, centres the clock input about the switching threshold (see Fig. 8).
2. The two complementary outputs are ECL10K compatible but internal pulldown resistors are not included and therefore external pulldown resistors to V_{EE} are required.

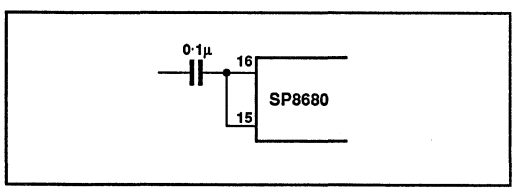


Fig. 7. AC coupled input

3. The TTL totem pole output operates with the same supply and is powered up by connecting V_{EE} (pin 12) to TTL V_{EE} (pin 13). If the TTL output is not required then the TTL V_{EE} pin should be left open circuit, reducing the power consumption by 20mW, typically.
4. Both control inputs ($\overline{PE1}$ and $\overline{PE2}$) are ECL10K compatible throughout the temperature range. Each control input is provided with a pullup resistor, the remote ends of which are connected to pins 6 and 7, respectively. This allows the pullup resistors to be unused if so desired or to be used to interface from TTL (see Fig. 9). If interfacing to ECL is required then pins 6 and 7 should be left open circuit; alternatively, they can be connected to V_{EE} to act as pulldown resistors. When high, the master set input sets the divider to the eleventh state, is asynchronous and overrides the clock input.
5. All the inputs have internal 50kΩ pulldown resistors.
6. The circuit will operate down to DC but inputslew rate must be better than 20V/µs.
7. Input impedance is a function of frequency. See Fig. 5.

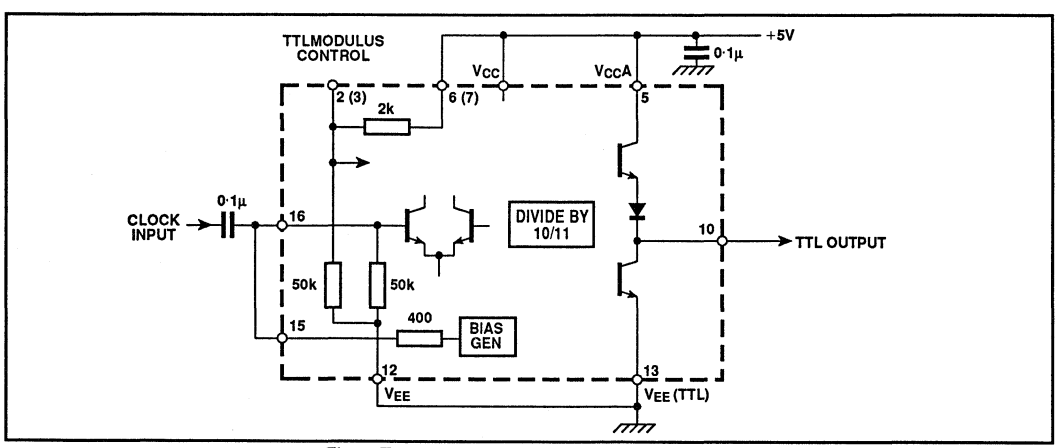


Fig. 8 Typical application showing TTL interfacing.

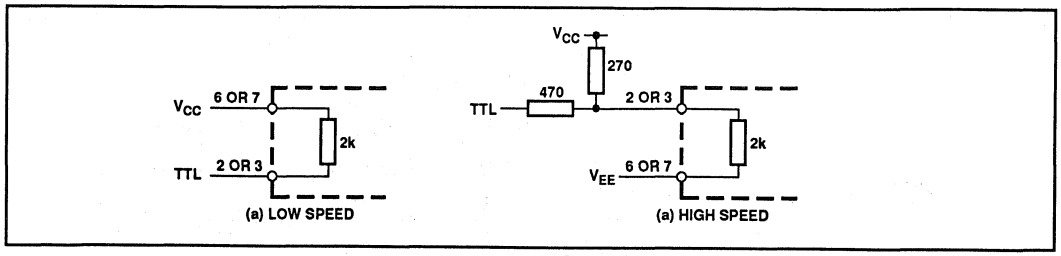


Fig. 9 TTL interface to $\overline{PE1}$ and $\overline{PE2}$

SP8680B

575MHz÷10/11

The SP8680B is an ECL variable modulus divider, with ECL and TTL compatible outputs. The circuit can operate from either ECL or TTL supplies. It divides by 10 when either of the ECL control inputs, $\overline{PE1}$ or $\overline{PE2}$, is in the high state and by 11 when both are low (or open circuit). The divider can be set asynchronously to the eleventh state by applying a high level to the master set (MS) input.

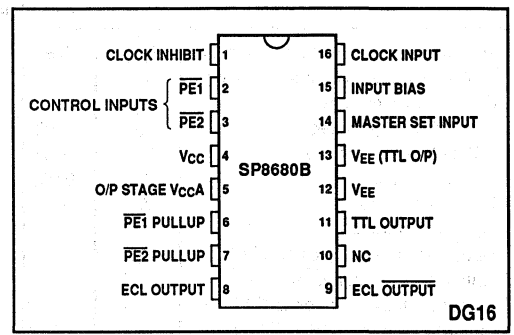


Fig. 1 Pin connections - top view

FEATURES

- Very High Speed – 650MHz (Typ.)
- ECL and TTL Compatible Inputs/Outputs
- DC or AC Clocking
- Clock Inhibit
- Asynchronous Master Set
- Equivalent to Fairchild 11C90

QUICK REFERENCE DATA

- Supply Voltage: −4·75V to −5·5V (ECL), 4·75V to 5·5V (TTL)
- Power Consumption: 420mW
- Temperature Range: −40°C to +85°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage, $\|V_{CC}-V_{EE}\|$	8V
ECL output source current	50mA
Storage temperature range	−65°C to +150°C
Max. junction temperature	+175°C
TTL output sink current	30mA
Max. clock input voltage	2·5V p-p

ORDERING INFORMATION

SP8680 B DG
SP8680 NA 1C

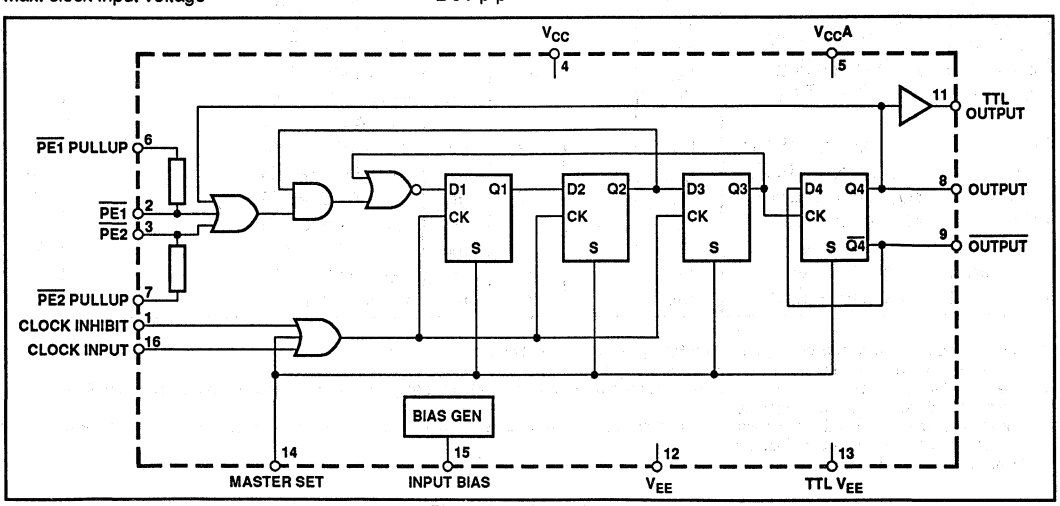


Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range

ECL OPERATION

Supply voltage, V_{EE} = −4·75V to − 5·5V, V_{CC} = 0V
Temperature, T_{AMB} = −40°C to +85°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{MAX}	575		MHz	AC coupled clock = 350mV p-p	
Minimum frequency (sinewave input)	f_{MIN}		10	MHz	AC coupled clock = 600mV p-p	5
Power supply current	I_{EE}		105	mA	V_{EE} = −5·5V, pins 6, 7, 13 o/c	
ECL output high voltage	V_{OH}	−0·93	−0·78	V	V_{EE} = −5·2V (25°C), R_L = 100Ω to −2V	
ECL output low voltage	V_{OL}	−1·85	−1·62	V	V_{EE} = −5·2V (25°C), R_L = 100Ω to −2V	
Input high voltage	V_{INH}	−0·095	−0·81	V	V_{EE} = −5·2V (25°C)	
Input low voltage	V_{INL}	−1·85	−1·475	V	V_{EE} = −5·2V (25°C)	
Input low currents	I_{IL}	0·5		µA	25°C	
Input high current, clock and MS	I_H		400	µA	V_{IN} = −1·85V (25°C)	
Input high current, $\overline{PE1}$ and $\overline{PE2}$	I_H		400	µA	V_{IN} = −0·8V (25°C)	
Propagation delay, clock to Q4 high	t_{pLH}		3	ns	R_L = 100Ω to −2V (25°C)	5
Propagation delay, MS to Q4 high	t_{pLH}		6	ns	25°C	5
Modulus control set-up time	t_s	4		ns	25°C	3, 5
Modulus control release time	t_r	4		ns	25°C	4, 5
ECL output rise time (20% - 80%)	t_{ELH}		2	ns	25°C	5
ECL output fall time (80% - 20%)	t_{EHL}		2	ns	25°C	5

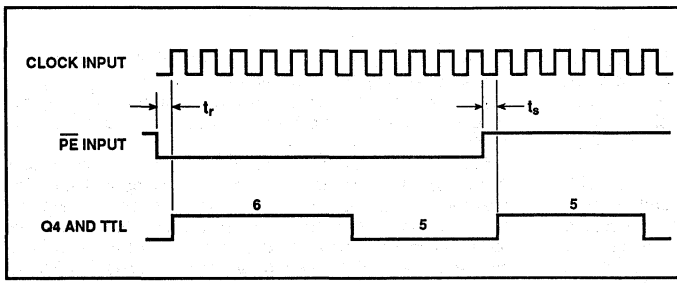
TTL OPERATION

Supply voltage, V_{CC} = V_{CC}A = 4·75V to 5·5V, V_{EE} = 0V
Temperature, T_{AMB} = −40°C to +85°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{MAX}	575		MHz	AC coupled clock = 350mV p-p	
Minimum frequency (sinewave input)	f_{MIN}		10	MHz	AC coupled clock = 600mV p-p	5
Power supply current	I_{CC}		111	mA	V_{CC} = 5·5V, pins 6, 7 o/c, pin 13 to pin 12	
TTL output high voltage	V_{OH}	2·3		V	V_{CC} = 4·75V, I_{OH} = −640µA	
TTL output low voltage	V_{OL}		0·5	V	V_{CC} = 5·5V, I_{OL} = −20µA	
Input high voltage, $\overline{PE1}$ and $\overline{PE2}$	V_{INH}	3·9		V	V_{CC} = 5·0V (25°C)	
Input low voltage, $\overline{PE1}$ and $\overline{PE2}$	V_{INL}		3·5	V	V_{CC} = 5·0V (25°C)	
Input low current, $\overline{PE1}$ and $\overline{PE2}$	I_{IL}	−4		mA	V_{CC} = 5·5V (25°C), pins 6, 7 = V_{CC}, V_{IN} = 0·4V	
Propagation delay, clock to TTL low	t_{pHL}	6	14	ns	V_{CC} = 5·0V (25°C)	5
Propagation delay, clock to TTL high	t_{pLH}	6	14	ns	V_{CC} = 5·0V (25°C)	5
Propagation delay, MS to TTL high	t_p		17	ns	V_{CC} = 5·0V (25°C)	5
Modulus control set-up time	t_s	4		ns	V_{CC} = 5·0V (25°C)	3, 5
Modulus control release time	t_r	4		ns	V_{CC} = 5·0V (25°C)	4, 5
TTL output rise time (20% - 80%)	t_{TLH}		5	ns	V_{CC} = 5·0V (25°C)	5
TTL output fall time (80% - 20%)	t_{THL}		5	ns	V_{CC} = 5·0V (25°C)	5

NOTES

1. The temperature coefficients of V_{OH} = +1·2mV/°C, V_{OL} = +0·25mV/°C and of V_{IN} = +0·8mV/°C.
2. The test configuration for dynamic testing is shown in Fig.6.
3. The set-up time t_s is defined as the minimum time that can elapse between L→H transition of control input and the next L→H clock pulse transition to ensure that the ÷10 mode is obtained.
4. The release time t_r is defined as the minimum time that can elapse between H→L transition of control input and the next L→H clock pulse transition to ensure that the ÷11 mode is obtained.
5. Guaranteed but not tested.



MS	Clock Inhibit	$\overline{PE1}$	$\overline{PE2}$	Output response
H	X	X	X	All outputs set high
L	H	X	X	Hold
L	L	L	L	÷11
L	L	H	L	÷10
L	L	L	H	÷10
L	L	H	H	÷10

Fig. 3 Truth table and timing diagram

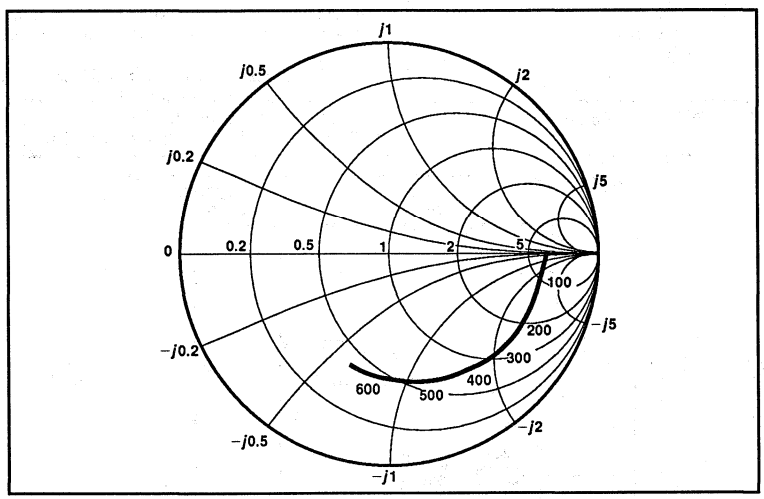


Fig. 4 Typical input impedance. Test conditions: Supply Voltage = 5V, Ambient Temperature = 25°C. Frequencies in MHz, impedances normalised to 50Ω.

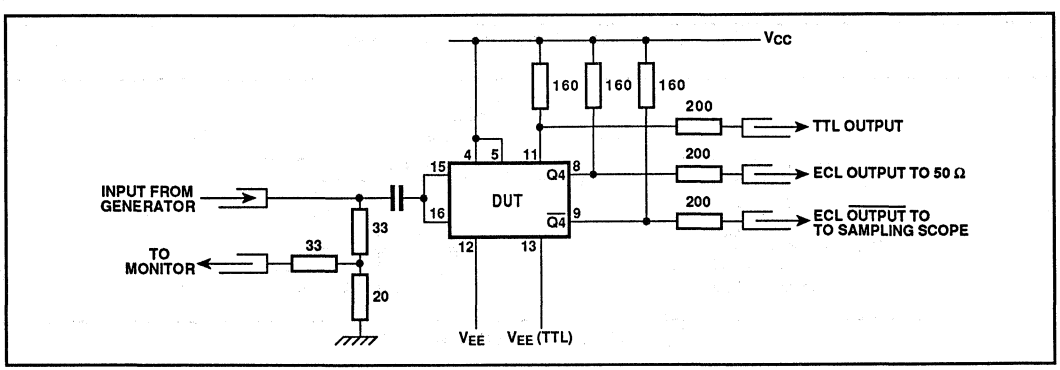


Fig. 5 Test circuit

OPERATING NOTES

1. The clock input, which is ECL10K compatible throughout the temperature range, can also be coupled to TTL as shown in Fig. 8. The clock can also be capacitively coupled to the signal source (see Fig, 6). Connecting the internally-generated bias voltage to the clock input i.e., pin 15 to pin 16, centres the clock input about the switching threshold (see Fig.7).
2. The two complementary outputs are ECL10K compatible but internal pulldown resistors are not included and therefore external pulldown resistors to V_{EE} are required. The outputs are capable of driving a 50Ω load to −2V over the temperature range −40°C to +85°C. The output high level will typically be reduced by 50mV.
3. The TTL totem pole output operates with the same supply and is powered up by connecting V_{EE} (pin 12) to TTL V_{EE} (pin 13). If the TTL output is not required then the TTL V_{EE} pin should be left open circuit, reducing the power consumption by 20mW, typically.
4. Both control inputs ($\overline{PE1}$ and $\overline{PE2}$) are ECL10K compatible throughout the temperature range. Each control input is provided with pullup resistor, the remote ends of which are connected to pins 6 and 7, respectively. This allows the pullup resistors to be unused if so desired or to be used to interface from TTL (see Fig. 9). If interfacing to ECL is required then pins 6 and 7 should be left open circuit; alternatively, they can be connected to V_{EE} to act as pulldown resistors. When high, the master set input sets the divider to the eleventh state, is asynchronous and overrides the clock input.
5. All the inputs have internal 50kΩ pulldown resistors.
6. The circuit will operate down to DC but inputslew rate must be better than 20V/µs.
7. Input impedance is a function of frequency. See Fig. 5.

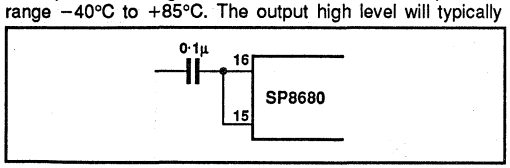


Fig. 6 AC coupled input

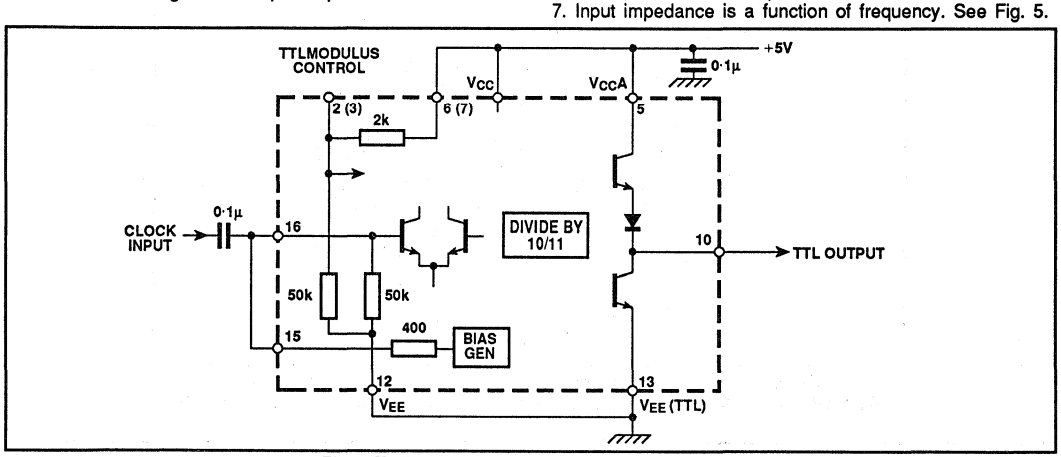


Fig. 7 Typical application showing TTL interfacing.

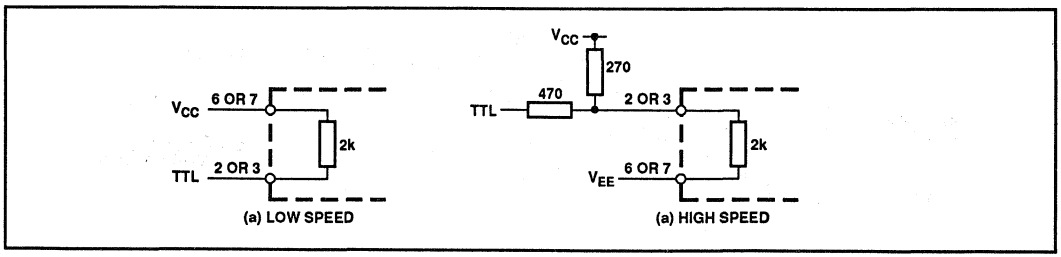


Fig. 8 TTL interface to $\overline{PE1}$ and $\overline{PE2}$

SP8685

500MHz÷10/11

The SP8685 is an ECL variable modulus divider, with ECL10K compatible outputs. It divides by 10 when either of the ECL control inputs, $\overline{PE1}$ or $\overline{PE2}$, is in the high state and by 11 when both are low (or open circuit).

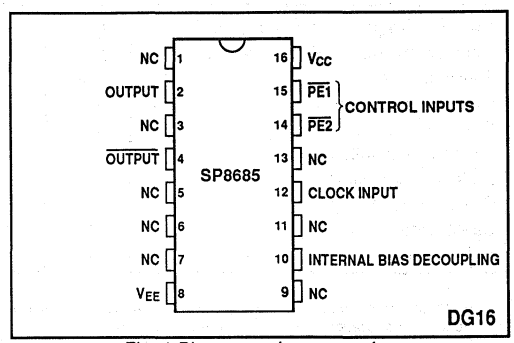


Fig. 1 Pin connections - top view

FEATURES

- Divides by 10 or 11
- AC-Coupled Input (Internal Bias)
- ECL Compatible Output

QUICK REFERENCE DATA

- Supply Voltage: −5·2V
- Power Consumption: 300mW
- Temperature Range:
  −55°C to +125°C (A Grade)
  −30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	−8V
Output current	20mA
Storage temperature range	−65°C to +150°C
Max. junction temperature	+175°C
Max. clock input voltage	2·5V p-p

ORDERING INFORMATION

SP8685 A DG
SP8685 B DG
SP8685 AC DG
SP8685 NA 1C

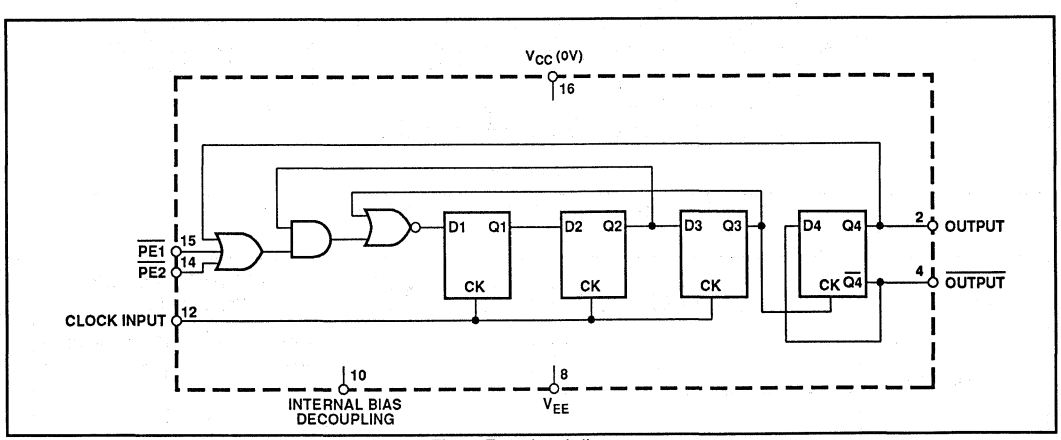


Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range
Supply voltage, V_{CC} = 0V, V_{EE} = −5·2V ± 0·25V
Temperature, T_{AMB} = −55°C to +125°C (A Grade), −30°C to +70°C (B Grade)

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{MAX}	500		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f_{MIN}		50	MHz	Input = 400-800mV p-p	
Power supply current	I_{EE}		70	mA	V_{EE} = −5·2V	
Output high voltage	V_{OH}	−0·87	−0·7	V	V_{EE} = −5·2V (25°C)	
Output low voltage	V_{OL}	−1·8	−1·5	V	V_{EE} = −5·2V (25°C)	
$\overline{PE}$ input high voltage	V_{INH}	−0·93		V	V_{EE} = −5·2V (25°C)	
$\overline{PE}$ input low voltage	V_{INL}		−1·62	V	V_{EE} = −5·2V (25°C)	
Clock to output delay	t_p		6	ns		5
Set-up time	t_s	2		ns		5
Release time	t_r	2		ns		5

NOTES
1. The temperature coefficients of V_{OH} = +1·63mV/°C, V_{OL} = +0·94mV/°C and of V_{IN} = +1·22mV/°C.
2. The test configuration for dynamic testing is shown in Fig.6.
3. The set-up time t_s is defined as the minimum time that can elapse between L→H transition of control input and the next L→H clock pulse transition to ensure that the ÷10 mode is obtained.
4. The release time t_r is defined as the minimum time that can elapse between H→L transition of control input and the next L→H clock pulse transition to ensure that the ÷11 mode is obtained.
5. Guaranteed but not tested.

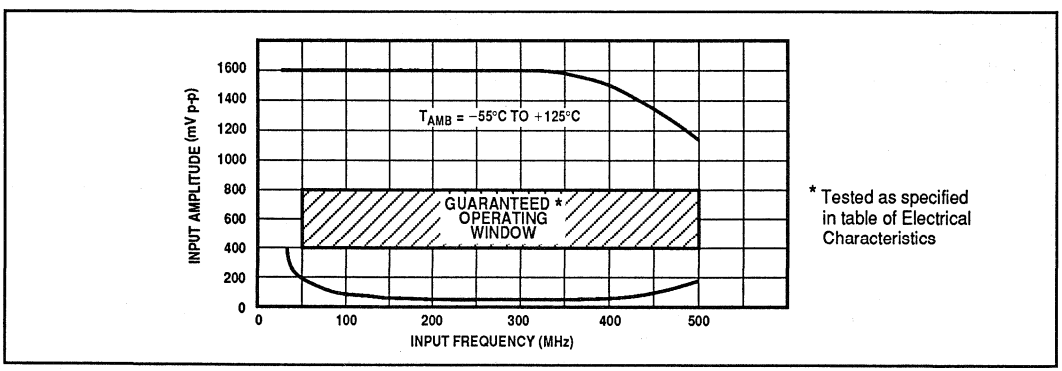
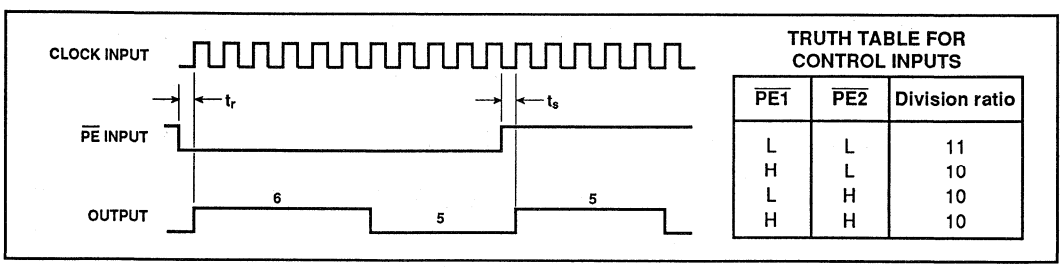


Fig. 3 Typical input characteristic of SP8685A



TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division ratio
L	L	11
H	L	10
L	H	10
H	H	10

Fig. 4 Timing diagram

OPERATING NOTES

1. The clock input is biased internally and is coupled to the signal source with a suitable capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected from pin 10 to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable, it may be prevented by connecting a 15kΩ resistor from the clock input (pin 12) to V_{EE}. This will reduce the input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/μs.
4. The outputs are compatible with ECLII but can be interfaced to ECL10K as shown in Fig. 7.
5. The PE inputs are ECLIII/10K compatible and include 4·3kΩ pulldown resistors. Unused inputs can therefore be left open.
6. Input impedance is a function of frequency, See Fig. 5.
7. All components should be suitable for the frequency in use.

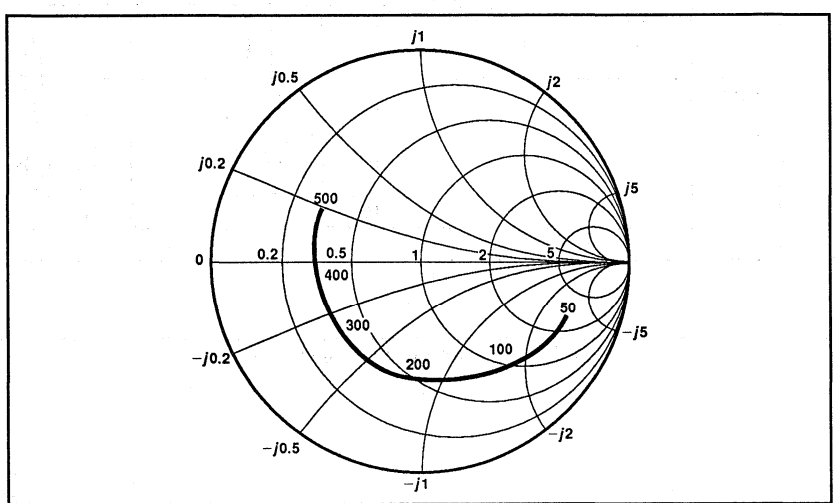


Fig. 5 Typical input impedance. Test conditions: Supply Voltage = −5·2V, Ambient Temperature = 25°C. Frequencies in MHz, impedances normalised to 50Ω.

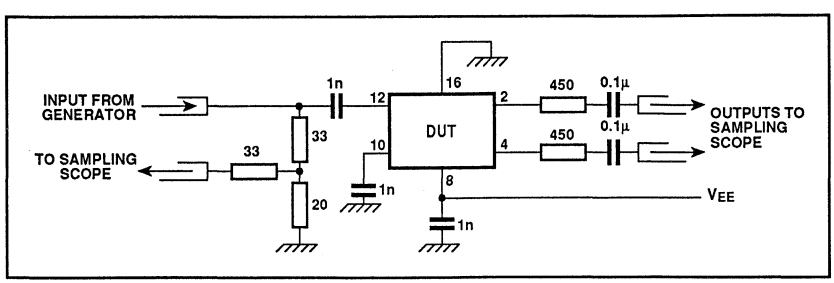


Fig. 6 Test circuit

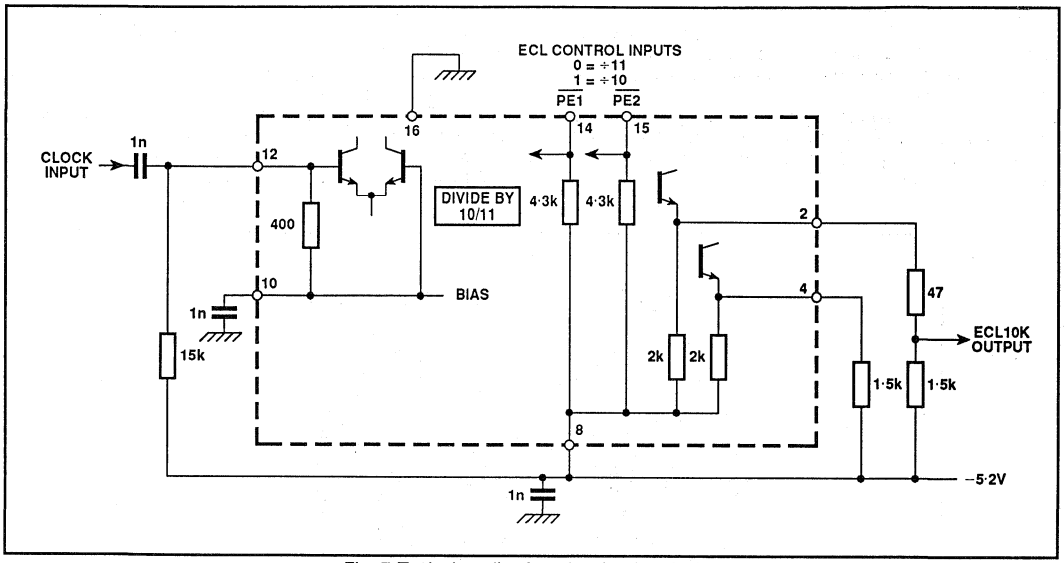


Fig. 7 Typical application showing interfacing

SP8690 200MHz÷10/11
SP8691 200MHz÷8/9

The SP8690 and SP8691 are low power ECL variable modulus dividers, with both ECL10K and TTL/CMOS compatible outputs. They divide by the lower division ratio when either of the ECL control inputs, $\overline{PE1}$ or $\overline{PE2}$, is in the high state and by the higher ratio when both are low (or open circuit).

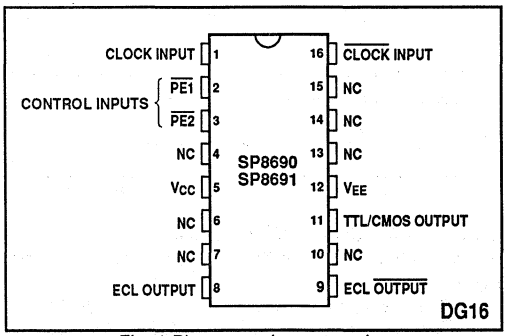


Fig. 1 Pin connections - top view

FEATURES

- ECL and TTL/CMOS Compatible Outputs
- AC-Coupled Input
- Control Inputs ECL Compatible

QUICK REFERENCE DATA

- Supply Voltage: −5·2V±0·25V (ECL), 5V±0·25V (TTL)
- Power Consumption: 70mW (Typ.)
- Temperature Range:
  - −55°C to +125°C (A Grade)
  - −30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage, $\lvert V_{CC}-V_{EE}\rvert$	8V
ECL output current	10mA
Storage temperature range	−65°C to +150°C
Max. junction temperature	+175°C
TTL output voltage	+12V
Input voltage	2·5V p-p
Max. open collector current	15mA

ORDERING INFORMATION

SP8690 A DG
SP8690 B DG
SP8691 A DG
5962-87678 (SMD) (SP8690)

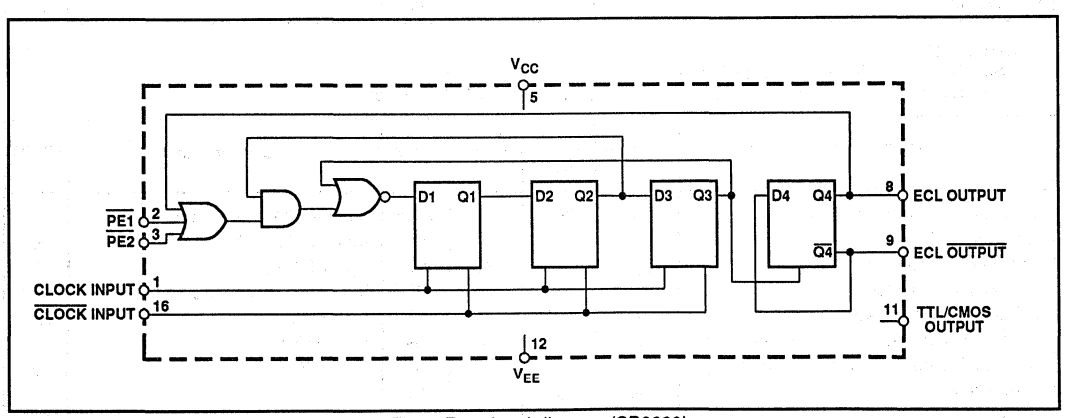


Fig. 2 Functional diagram (SP8690)

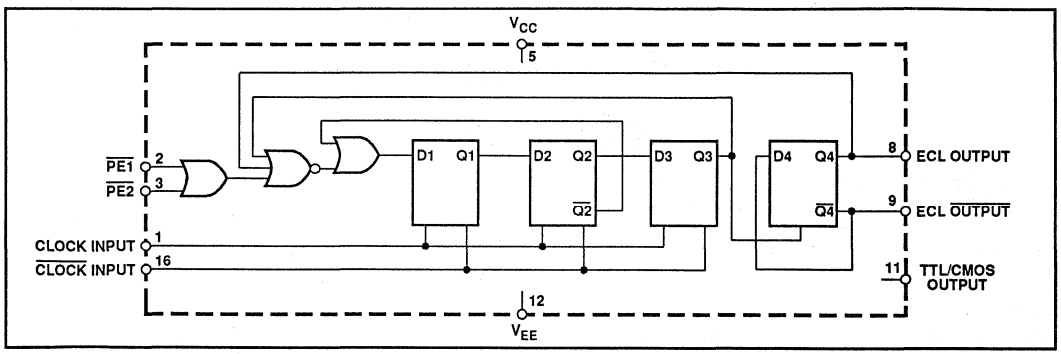


Fig. 3 Functional diagram (SP8691)

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range

ECL OPERATION

Supply voltage, V_{CC} = 0V, V_{EE} = −5·2V ± 0·25V
Temperature, T_{AMB} = −55°C to +125°C (A Grade), −30°C to +70°C (B Grade)

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{MAX}	200		MHz	Input = 400-800mV p-p	5
Minimum frequency (sinewave input)	f_{MIN}		40	MHz	Input = 400-800mV p-p	5
Power supply current	I_{EE}		21	mA	V_{EE} = −5·0V	5
ECL output high voltage	V_{OH}	−0·85	−0·7	V	V_{EE} = −5·2V (25°C)	
ECL output low voltage	V_{OL}	−1·8	−1·5	V	V_{EE} = −5·2V (25°C)	
$\overline{PE}$ input high voltage	V_{INH}	−0·93		V	V_{EE} = −5·2V (25°C)	
$\overline{PE}$ input low voltage	V_{INL}		−1·62	V	V_{EE} = −5·2V (25°C)	
Clock to ECL output delay	t_p		9	ns		6
Set-up time	t_s	3		ns		3, 6
Release time	t_r	8		ns		4, 6

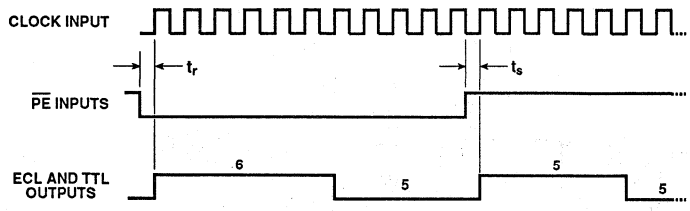
TTL OPERATION

Supply voltage, V_{CC} = 5V ± 0·25V, V_{EE} = 0V
Temperature, T_{AMB} = −55°C to +125°C (A Grade), −30°C to +70°C (B Grade)

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{MAX}	200		MHz	Input = 400-800mV p-p	5
Minimum frequency (sinewave input)	f_{MIN}		40	MHz	Input = 400-800mV p-p	5
Power supply current	I_{EE}		21	mA	V_{CC} = 5·0V	5
TTL output low voltage	V_{OL}		0·5	V	V_{CC} = 5V, R_L = 560Ω	5, 7
TTL output high voltage	V_{OH}	3·75		V	R_L = 560Ω	5, 7
Clock to TTL output high delay, +ve going	t_{PLH}		32	ns	R_L = 560Ω	6
Clock to TTL output low delay, −ve going	t_{PHL}		18	ns	R_L = 560Ω	6
Set-up time	t_s	3		ns		3, 6
Release time	t_r	8		ns		4, 6

NOTES

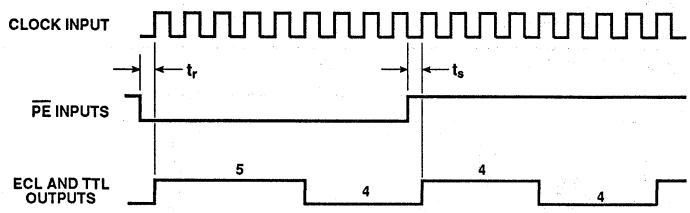
1. The temperature coefficients of V_{OH} = +1·63mV/°C, V_{OL} = +0·94mV/°C and of V_{IN} = +1·22mV/°C.
2. The test configuration for dynamic testing is shown in Fig.8
3. The set-up time t_s is defined as the minimum time that can elapse between L→H transition of control input and the next L→H clock pulse transition to ensure that division by the lower modulus is obtained.
4. The release time t_r is defined as the minimum time that can elapse between H→L transition of control input and the next L→H clock pulse transition to ensure that division by the higher modulus is obtained.
5. SP8690/1B tested at 25°C only.
6. Guaranteed but not tested.
7. The open collector output is not recommended for use at output frequencies above 15MHz. $C_{LOAD} \leq 5pF$.



TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division ratio
L	L	11
H	L	10
L	H	10
H	H	10

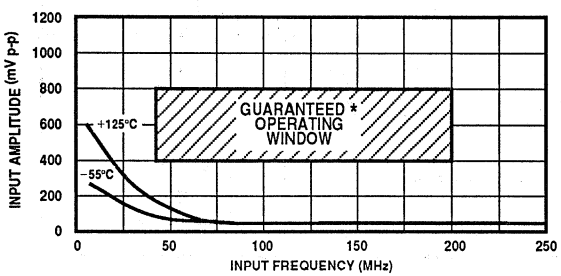
Fig. 4 Timing diagram, SP8690



TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division ratio
L	L	9
H	L	8
L	H	8
H	H	8

Fig. 5 Timing diagram, SP8691



* Tested as specified in table of Electrical Characteristics

Fig. 6 Typical input characteristics, SP8690/1

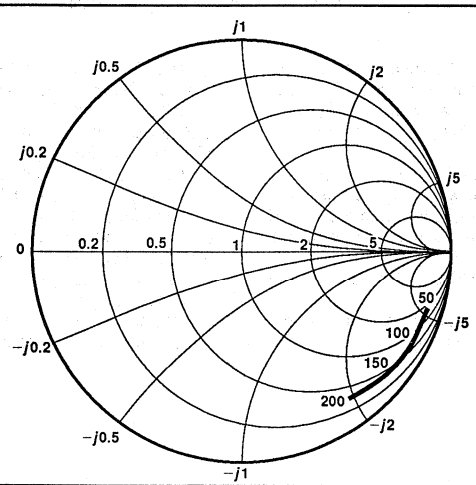


Fig. 7 Typical input impedance. Test conditions: Supply Voltage = 5.0V, Ambient Temperature = 25°C. Frequencies in MHz, impedances normalised to 50Ω.

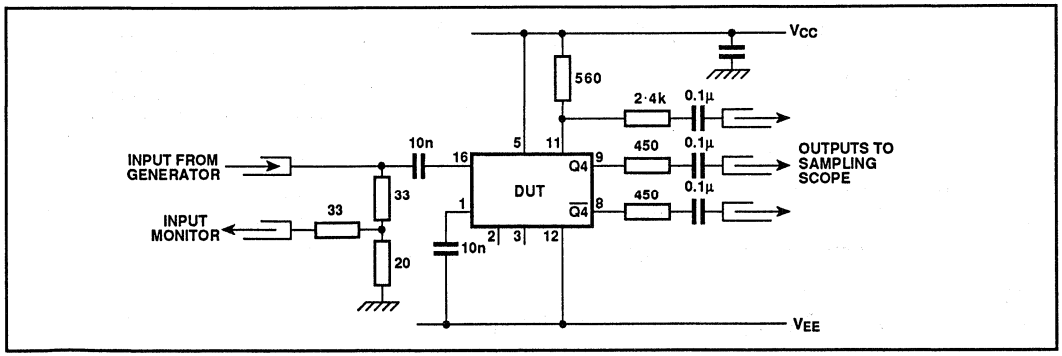


Fig. 8 Test circuit for dynamic measurements

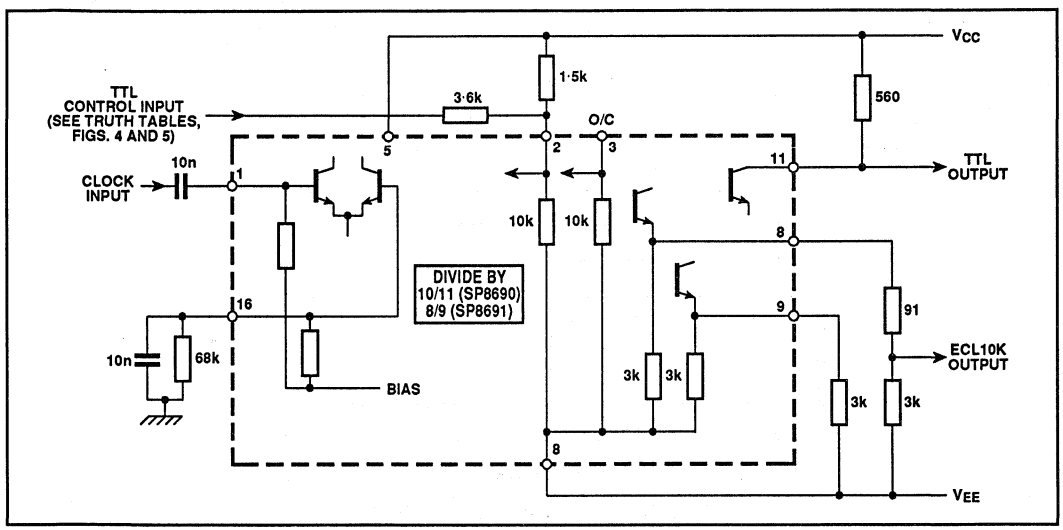


Fig. 9 Typical application showing interfacing.

OPERATING NOTES

1. The clock inputs can be single or differentially driven. The clock input is biased internally and is coupled to the signal source with a suitable capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to ground.
2. In the absence of a signal the device will self-oscillate. If this is undesirable, it may be prevented by connecting a 68kΩ resistor from the input to V_{EE} i.e., from pin 1 or pin 16 to pin 12. This reduces the input sensitiviy by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/µs.
4. The Q_4 and $\overline{Q}_4$ outputs are compatible with ECLII but can be interfaced to ECL10K as shown in Fig. 9.
5. The PE inputs are ECLIII/10K compatible and include internal 10kΩ pulldown resistors. Unused inputs can therefore be left open circuit.
6. The input impedance of the SP8690/1 varies as a function of frequency. See Fig. 7.
7. The TTL/CMOS output is a free collector and the high state output voltage will depend on the supply that the collector load is taken to. This should not exceed 12V.
8. The rise/fall time of the open collector output waveform is directly proportional to load capacitance and load resistor value. Therefore, load capacitance should be minimised and the load resistor kept to a minimum consistent with system power requirements. In the test configuration of Fig. 8 the output rise time is approximately 10ns and the fall time

SP8695

200MHz÷10/11

The SP8695 is a low power ECL variable modulus divider, with ECL10K and TTL/CMOS compatible outputs. It divides by 10 when either of the ECL control inputs, $\overline{PE1}$ or $\overline{PE2}$, is in the high state and by 11 when both are low (or open circuit). The inputs are ECLII compatible but can also be AC coupled. An open collector output is provided for interfacing to TTL or CMOS.

FEATURES

- Low Frequency Operation
- ECL and TTL/CMOS Compatible Outputs
- DC or AC-Coupled Input

QUICK REFERENCE DATA

- Supply Voltage: −5·2V±0·25V (ECL), 5·0V±0·25V (TTL)
- Power Consumption: 80mW
- Maximum Input Frequency: 200MHz
- Temperature Range: −55°C to +125°C

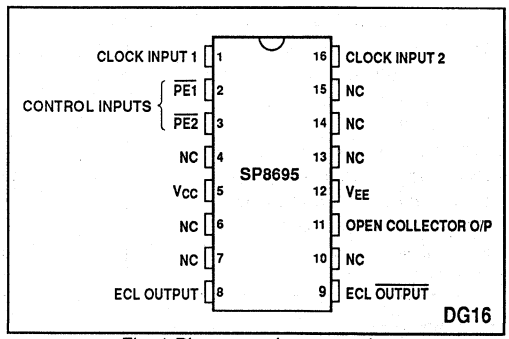


Fig. 1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage, $\lvert V_{CC}-V_{EE}\rvert$	8V
Output ECL current	10mA
Storage temperature range	−65°C to +150°C
Max. junction temperature	+175°C
Max. input voltage	2·5V p-p
Max. open collector output voltage	+12V
Max. open collector current	15mA

ORDERING INFORMATION

SP8695 A DG

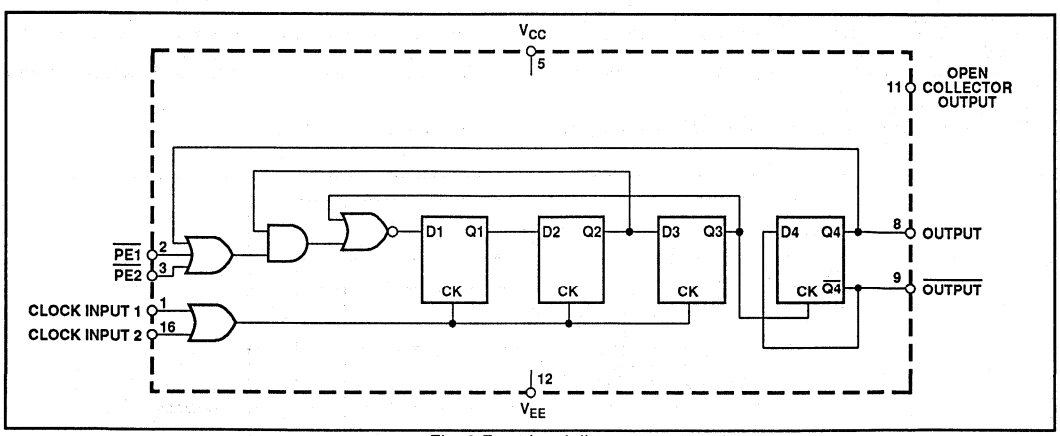


Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range

ECL OPERATION

Supply voltage, V_{CC} = 0V, V_{EE} = −5·2V ± 0·25V
Temperature, T_{AMB} = −55°C to +125°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{MAX}	200		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f_{MIN}		2	MHz	Input = 400-800mV p-p	5
Power supply current	I_{EE}		21	mA	V_{EE} = −5·0V	
ECL output high voltage	V_{OH}	−0·85	−0·7	V	V_{EE} = −5·2V (25°C)	
ECL output low voltage	V_{OL}	−1·8	−1·5	V	V_{EE} = −5·2V (25°C)	
Clock and $\overline{PE}$ input high voltage	V_{INH}	−0·93		V	V_{EE} = −5·2V (25°C)	
Clock and $\overline{PE}$ input low voltage	V_{INL}		−1·62	V	V_{EE} = −5·2V (25°C)	
Clock to ECL output delay	t_p		9	ns		5
Set-up time	t_s	3		ns		3, 5
Release time	t_r	8		ns		4, 5

TTL OPERATION

Supply voltage, V_{CC} = 5·0V ± 0·25V, V_{EE} = 0V
Temperature, T_{AMB} = −55°C to +125°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{MAX}	200		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f_{MIN}		2	MHz	Input = 400-800mV p-p	5
Power supply current	I_{CC}		21	mA	V_{CC} = 5·0V	
TTL output high voltage	V_{OH}	3·75		V	V_{CC} = 5V, R_L = 560Ω	6
TTL output low voltage	V_{OL}		0·5	V	R_L = 560Ω	6
Clock to TTL output high delay, +ve going	t_{PLH}		32	ns	R_L = 560Ω	5
Clock to TTL output low delay, −ve going	t_{PHL}		18	ns	R_L = 560Ω	5
Set-up time	t_s	3		ns		3, 5
Release time	t_r	8		ns		4, 5

NOTES

1. The temperature coefficients of V_{OH} = +1·63mV/°C, V_{OL} = +0·94mV/°C and of V_{IN} = +1·22mV/°C but these are not tested.
2. The test configuration for dynamic testing is shown in Fig.6.
3. The set-up time t_s is defined as the minimum time that can elapse between L→H transition of control input and the next L→H clock pulse transition to ensure that the ÷10 mode is obtained.
4. The release time t_r is defined as the minimum time that can elapse between H→L transition of control input and the next L→H clock pulse transition to ensure that the ÷11 mode is obtained.
5. Guaranteed but not tested.
6. The open collector output is not recommended for use at output frequencies above 15MHz. $C_{LOAD} \leq 5pF$.

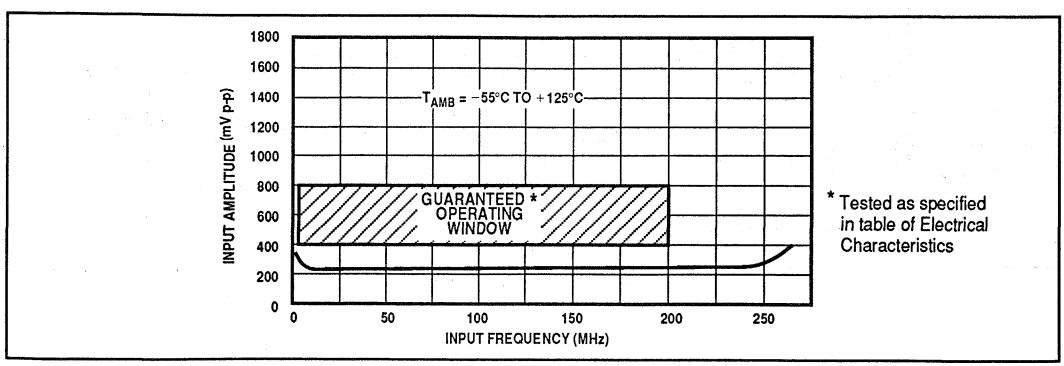
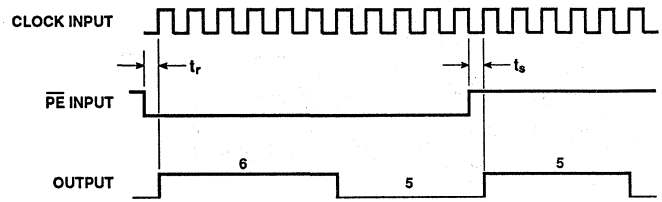


Fig. 3 Typical input characteristic



TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division ratio
L	L	11
H	L	10
L	H	10
H	H	10

Fig. 4 Timing diagram

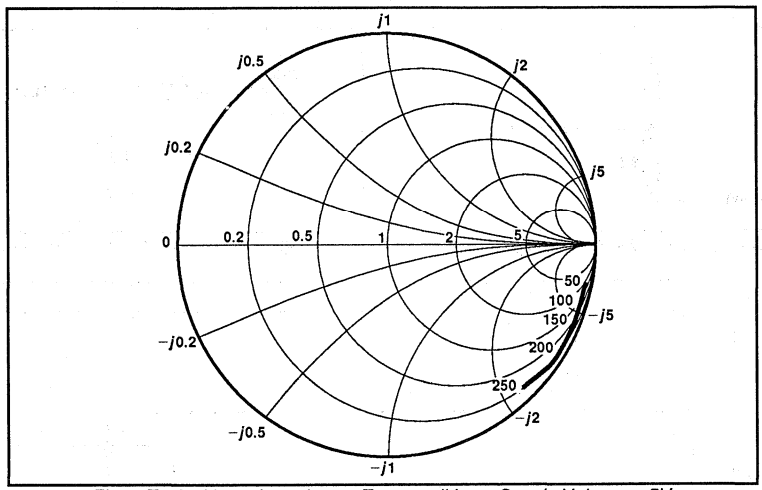


Fig. 5 Typical input impedance. Test conditions: Supply Voltage = 5V, Ambient Temperature = 25°C. Frequencies in MHz, impedances normalised to 50Ω.

OPERATING NOTES

1. The clock inputs can be driven from ECLII, III and 10K. The input reference voltage (−3·8V at 25°C) is compatible with ECLII, III and 10K over the specified temperature range. The inputs can also be capacitively coupled by addition of external bias as shown in Fig. 6. Each input has an internal pulldown resistor of 10kΩ and can therefore be left open circuit. They should be be bypassed to RF where maximum noise immunity is required.
2. The $\overline{PE}$ control inputs are similarly ECLIII/10K compatible and also have internal 10kΩ pulldown resistors, allowing unused inputs to be left open circuit if required.
3. The Q4 and $\overline{Q4}$ ECL outputs have internal circuitry equivalent to a 14kΩ pulldown resistor on each output and are ECLII compatible; they can, however, be interfaced to ECLIII/ 10K as shown in Fig. 8.
4. The circuit will operate down to DC but slew rate must be better than 5V/μs.
4. The input impedance of the SP8695 varies as a function of frequency. See Fig. 5.
5. The TTL/CMOS output is a free collector and the high state output voltage will depend on the supply that the collector load is taken to; this should not exceed 12V. The rise and fall time of the open collector output waveform is directly proportional to load resistance and load capacitance. The load capacitance should therefore be kept to a minimum and the load resistance should be kept to the minimum consistent with system power requirements. In the test configuration of Fig. 6 the output rise time is approximately 10ns and fall time is 7ns typically.

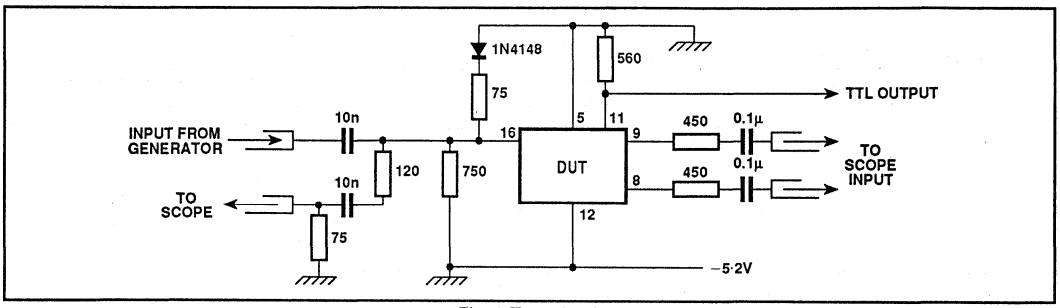


Fig. 6 Test circuit

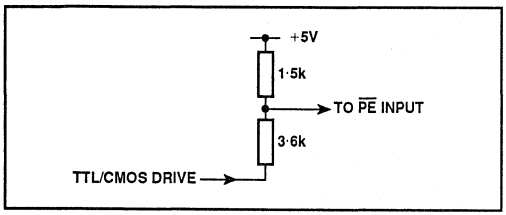


Fig. 7 Interfacing TTL/CMOS to $\overline{PE}$ inputs

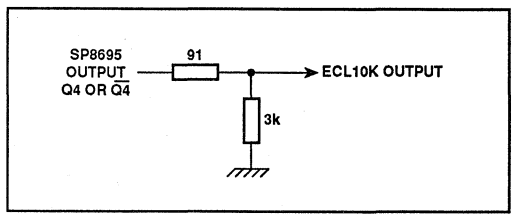


Fig. 8 Interfacing SP8695 output to ECL10K

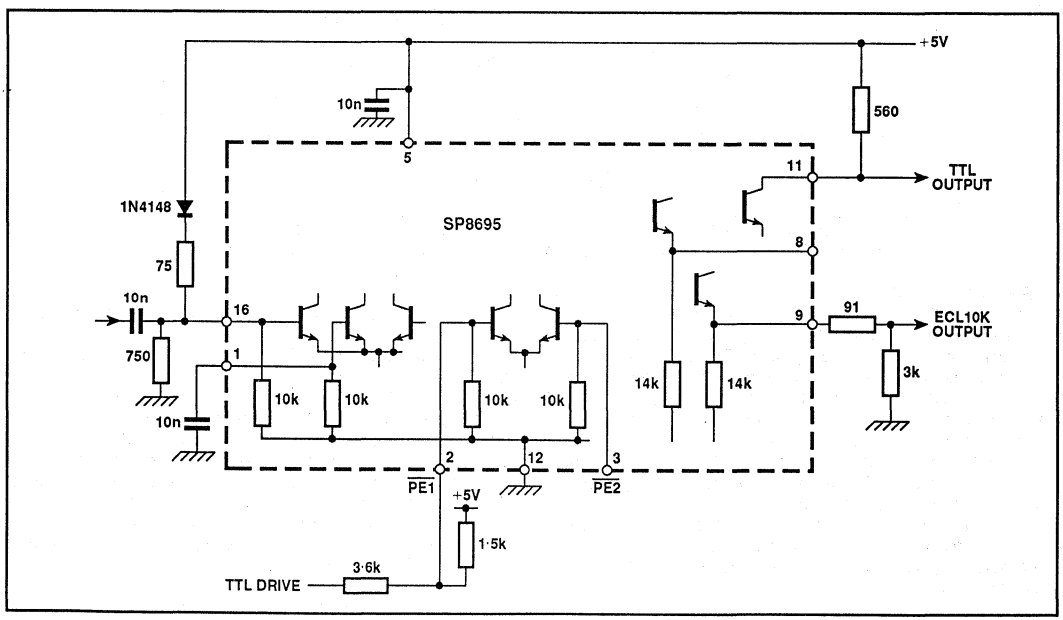


Fig. 9 Typical application showing interfacing.

SP8720

300MHz÷3/4

The SP8720 is an ECL two-modulus divider, with ECL10K compatible outputs. It divides by 3 when either of the ECL control inputs, $\overline{PE1}$ or $\overline{PE2}$, is in the high state and by 4 when both are low (or open circuit). An AC coupled input of 600mVp-p is required.

FEATURES

- ECL Compatible Outputs
- AC-Coupled Input (Internal Bias)
- Control Inputs ECL III/10K Compatible

QUICK REFERENCE DATA

- Supply Voltage: −5·2V
- Power Consumption: 240mW
- Temperature Range:
  −55°C to +125°C (A Grade)
  −30°C to +70°C (B Grade)

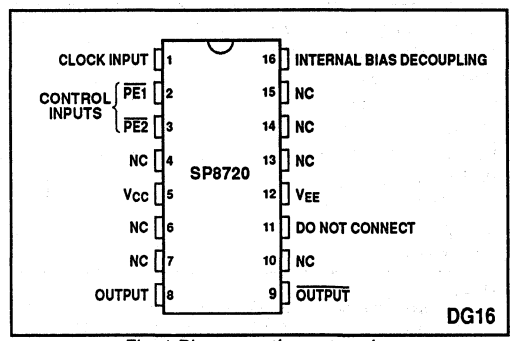


Fig. 1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage	−8V
Output current	20mA
Storage temperature range	−65°C to +150°C
Max. junction temperature	+175°C
Max. clock input voltage	2·5V p-p

ORDERING INFORMATION

SP8720 A DG
SP8720 B DG
5962-90577 (SMD)

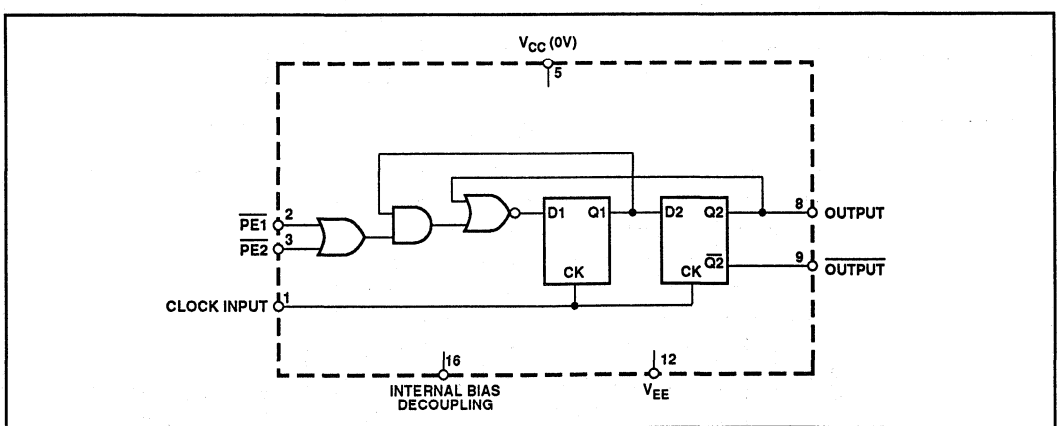


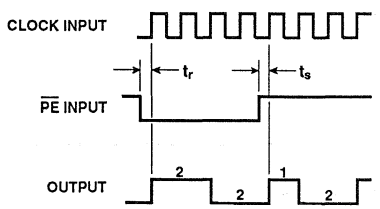
Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range
Supply voltage, V_{CC} = 0V, V_{EE} = −5·2V ± 0·25V
Temperature, T_{AMB} = −55°C to +125°C (A Grade), −30°C to +70°C (B Grade)

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{MAX}	300		MHz	Input = 400-800mV p-p	5
Minimum frequency (sinewave input)	f_{MIN}		40	MHz	Input = 400-800mV p-p	5
Power supply current	I_{EE}		65	mA	V_{EE} = −5·2V	5
Output high voltage	V_{OH}	−0·85	−0·7	V	V_{EE} = −5·2V (25°C)	
Output low voltage	V_{OL}	−1·8	−1·5	V	V_{EE} = −5·2V (25°C)	
$\overline{PE}$ input high voltage	V_{INH}	−0·93		V	V_{EE} = −5·2V (25°C)	
$\overline{PE}$ input low voltage	V_{INL}		−1·62	V	V_{EE} = −5·2V (25°C)	
Clock to output delay	t_p		6	ns		6
Set-up time	t_s	2·5		ns		3, 6
Release time	t_r	3		ns		4, 6

NOTES
1. The temperature coefficients of V_{OH} = +1·63mV/°C, V_{OL} = +0·94mV/°C and of V_{IN} = +1·22mV/°C.
2. The test configuration for dynamic testing is shown in Fig.6.
3. The set-up time t_s is defined as the minimum time that can elapse between L→H transition of control input and the next L→H clock pulse transition to ensure that the ÷3 mode is obtained.
4. The release time t_r is defined as the minimum time that can elapse between H→L transition of control input and the next L→H clock pulse transition to ensure that the ÷4 mode is obtained.
5. SP8720B tested at 25°C only.
6. Guaranteed but not tested.



TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division ratio
L	L	4
H	L	3
L	H	3
H	H	3

Fig. 3 Timing diagram

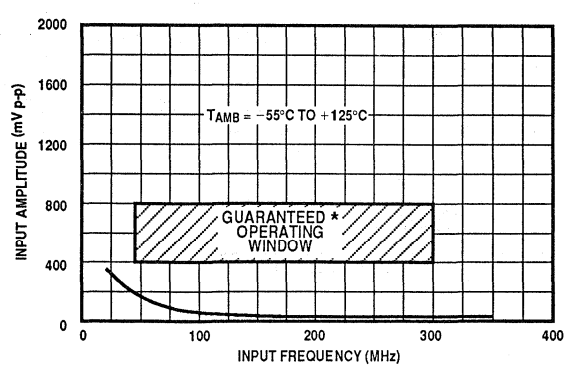


Fig. 4 Typical input characteristic of SP8720A

OPERATING NOTES

1. The clock input is biased internally and is coupled to the signal source with a suitable capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected from pin 16 to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable, it may be prevented by connecting a 15kΩ resistor from the clock input (pin 1) to V_{EE}. This will reduce the input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/μs.
4. The Q and $\overline{Q}$ outputs are compatible with ECLII but can be interfaced to ECL10K as shown in Fig. 7. There is an internal circuit equivalent to a load of 2kΩ at each output.
5. The PE inputs are ECLIII/10K compatible and include 4·3kΩ pulldown resistors. Unused inputs can therefore be left open.
6. The input impedance of the SP8720 varies as a function of frequency, see Fig. 5.
7. All components should be suitable for the frequency in use.

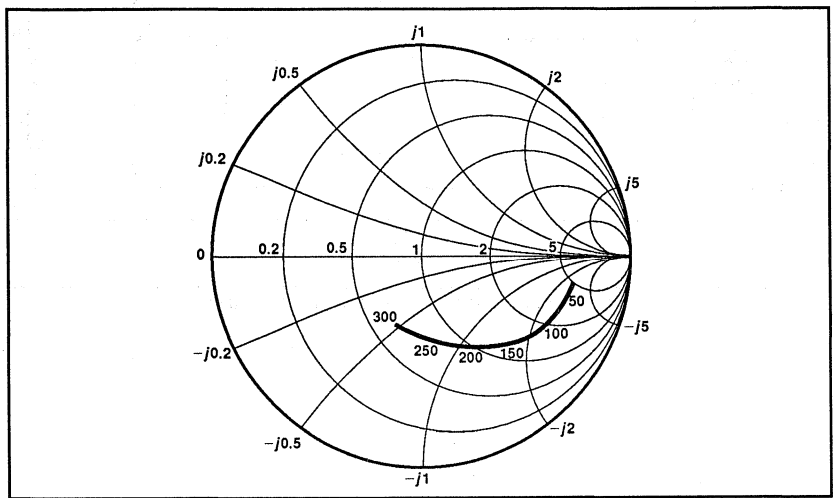


Fig. 5 Typical input impedance. Test conditions: Supply Voltage = −5·2V, Ambient Temperature = 25°C. Frequencies in MHz, impedances normalised to 50Ω.

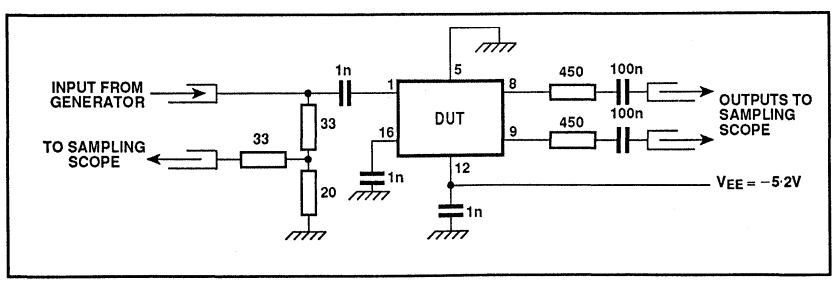


Fig. 6 Test circuit

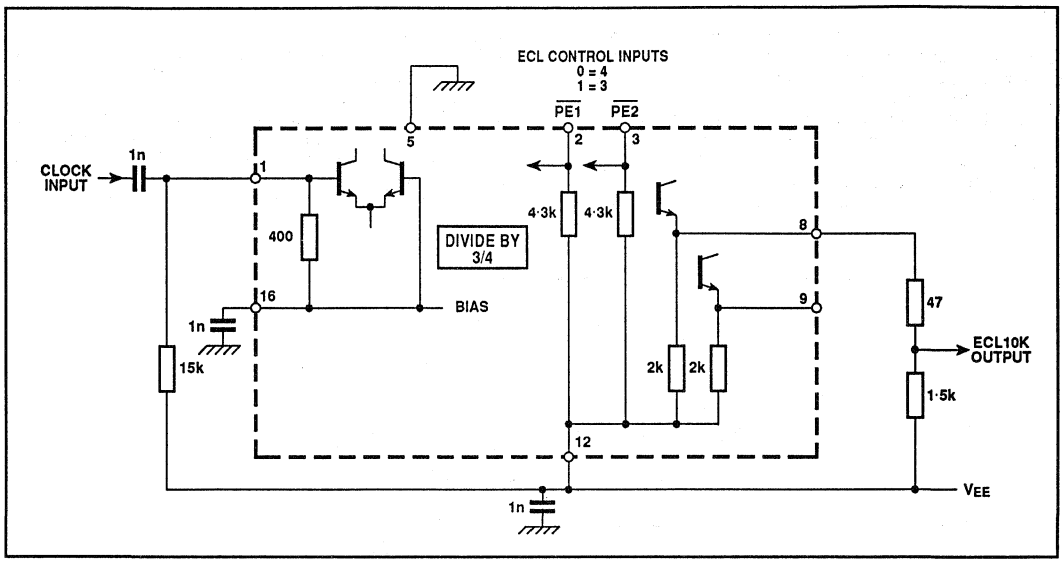


Fig. 7 Typical application circuit showing interfacing

SP8735

600MHz÷8 (BINARY OUTPUTS)

The SP8735 is a ÷8 ECL counter with binary outputs. In addition, carry outputs are provided in TTL and ECL. The AC coupled input requires a 600mV p-p signal and the outputs are open collectors. A TTL compatible reset is provided, making this device ideal for instrumentation applications.

FEATURES

- Binary Outputs to Open Collectors
- TTL Compatible Reset Input
- AC Coupled Input (Internal Bias)
- TTL and ECL Compatible Carry Outputs
- ECL Compatible Clock Inhibit Input

QUICK REFERENCE DATA

- Supply Voltage: −5·2V
- Power Consumption: 400mW
- Temperature Range: 0°C to +70°C

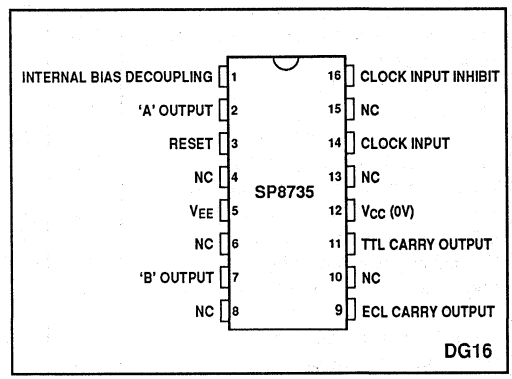


Fig. 1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage	−8V
Binary output voltage	V_{EE}+11V
Storage temperature range	−55°C to +150°C
Max. junction temperature	+175°C
Max. clock input voltage	2·5V p-p

ORDERING INFORMATION

SP8735 B DG

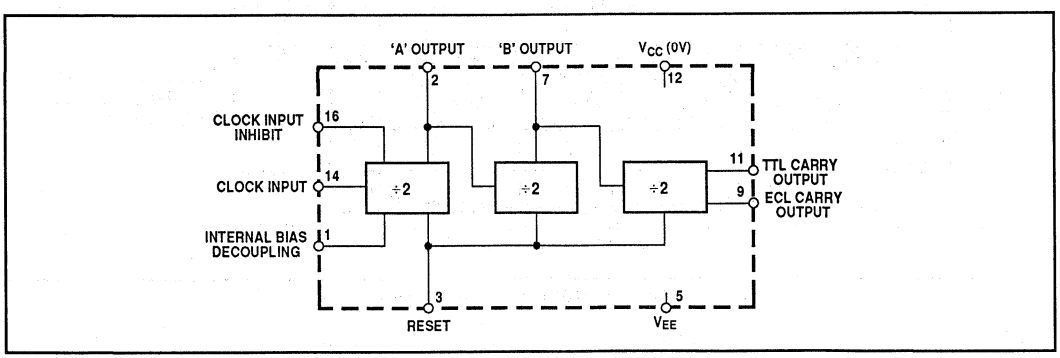


Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range
Supply voltage, V_{CC} = 0V, V_{EE} = −5·2V±0·25V
Temperature, T_{AMB} = 0°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{MAX}	600		MHz	Input = 400-800mV p-p	4
Minimum toggle frequency (sinewave input)	f_{MIN}		40	MHz	Input = 400-800mV p-p	6
Power supply current	I_{CC}		90	mA	V_{EE} = −5·2V	5
Clock inhibit high voltage	V_{INH}	−0·96		V	V_{EE} = −5·2V (25°C)	
Clock inhibit low voltage	V_{INL}		−1·65	V	V_{EE} = −5·2V (25°C)	
TTL output high voltage (pins 2, 7)	V_{OH}	2·4		V	10kΩ from TTL output to +5V	5
TTL output low voltage (pins 2, 7)	V_{OL}		0·4	V	10kΩ from TTL output to +5V	5
TTL carry output high voltage (pin 11)	V_{OH}	2·4		V	5kΩ from TTL output to +5V	5
TTL carry output low voltage (pin 11)	V_{OL}		0·4	V	5kΩ from TTL output to +5V	5
ECL output high voltage (pin 9)	V_{OH}	−0·9	−0·7	V	V_{EE} = −5·2V (25°C)	
ECL output low voltage (pin 9)	V_{OL}	−1·8	−1·5	V	V_{EE} = −5·2V (25°C)	
Edge speed for correct operation at maximum frequency	t_E		2·5	ns	10% to 90%	6
Reset ON time for correct operation	t_{ON}	100		ns		6
Reset input high voltage	V_{INH}	2·4		V		5
Reset input low voltage	V_{INL}		0·5	V		5

NOTES
1. The temperature coefficient of V_{OH} (ECL) = +3mV/°C and V_{OL} = +0·5mV/°C but these are not tested.
1. The temperature coefficient of inhibit threshold voltage = +0·24mV/°C but this is not tested.
3. The test configuration for dynamic testing is shown in Fig.5.
4. Tested at 0°C and +70°C only.
5. Tested at +25°C only.
6. Guaranteed but not tested.

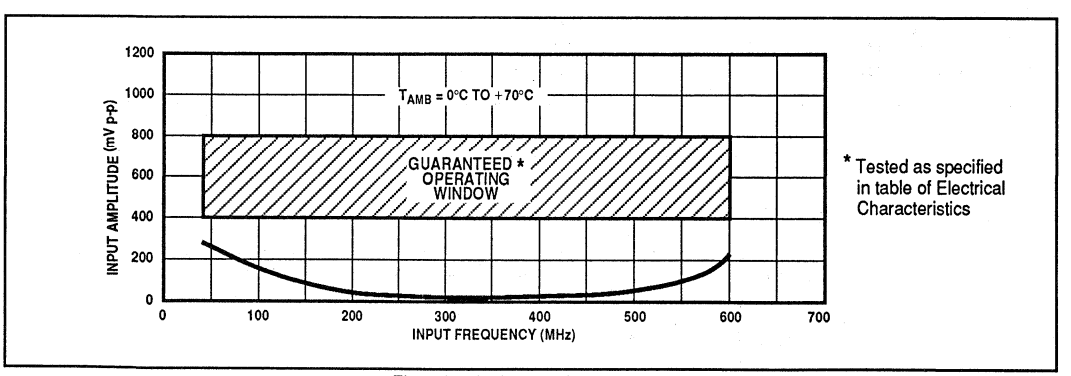


Fig. 3 Typical input characteristic

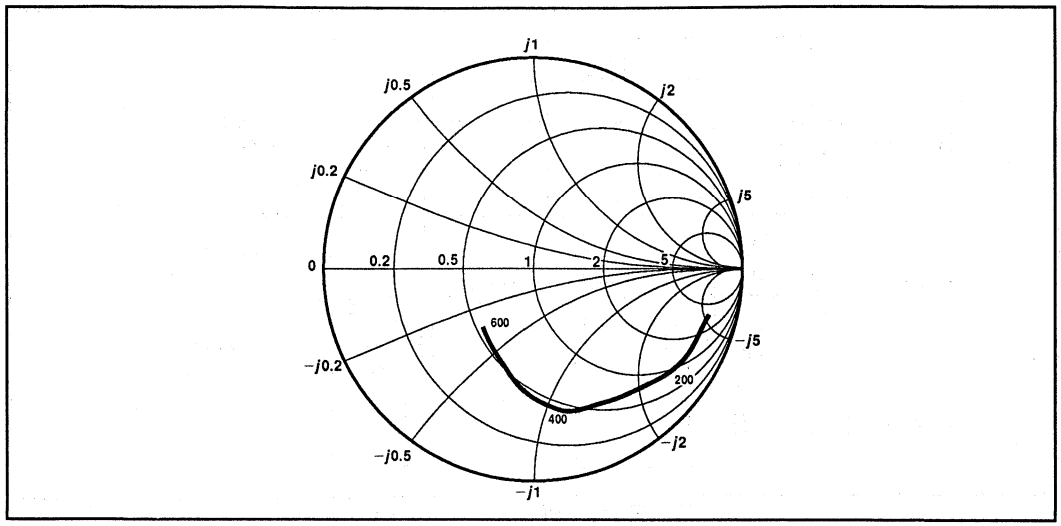


Fig. 4 Typical input impedance. Test conditions: supply voltage = −5·2V, ambient temperature = 25°C, frequencies in MHz, Impedances normalised to 50Ω

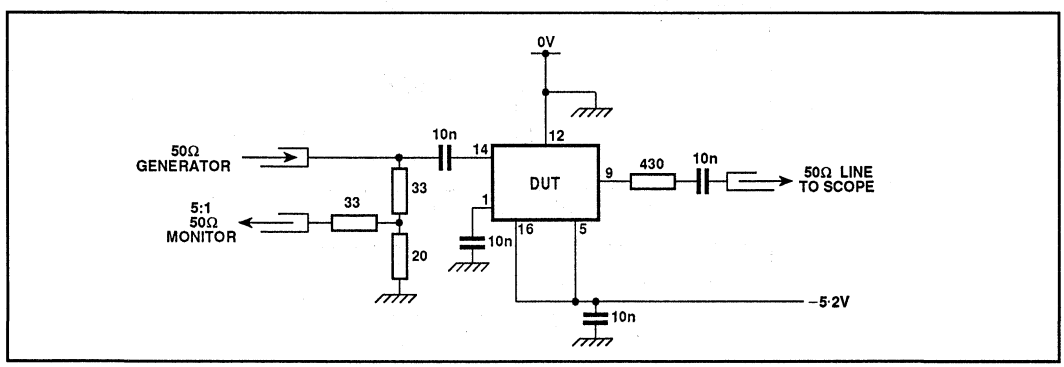


Fig. 5 SP8735 high frequency test circuit

OPERATING NOTES

1. The clock input (pin 14) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling (pin 1) to ground.
2. In the absence of a signal the device will self-oscillate. This can be prevented by connecting a 68kΩ resistor between the clock input (pin 14) and the negative supply (pin 5).
3. The device will operate down to DC but the input slew rate must be better than 100V/µs.
4. The ECL carry output (pin 9) is ECLII compatible but can be interfaced to ECLIII/10K by the addition of two resistors as shown in Fig. 7.
5. The clock inhibit is compatible with ECLIII/10K throughout the temperature range.
6. The 'A', 'B' and TTL carry outputs (pin 11) are current sources and require the addition of 10kΩ resistors (pins 2 and 7) and a 5kΩ resistor (pin 11) to +5V as shown in Fig. 6. This gives a fan-out of 1, which can be increased by buffering with a PNP transistor as shown in Fig. 6.
7. The circuits are clocked on the positive transitions of the clock input, provided that the clock inhibit input (pin 16) is in the low state.
8. Input impedance varies as a function of frequency; see Fig. 4

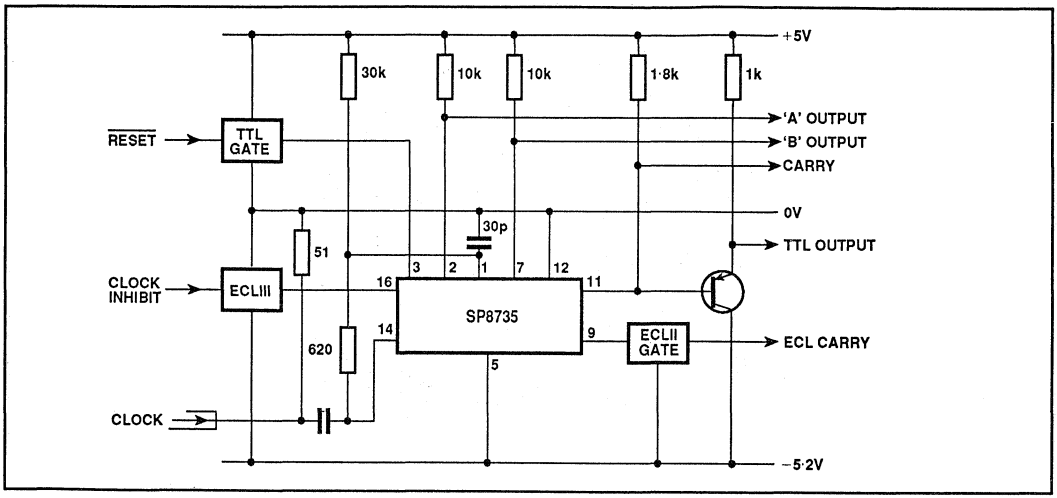


Fig. 6 Typical application configuration

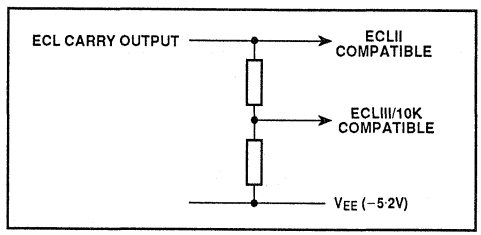


Fig. 7 ECLIII/10k interfacing

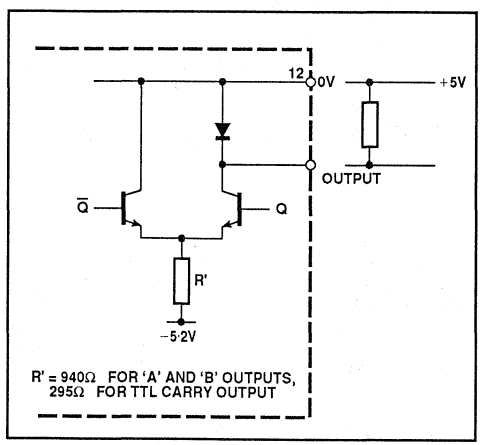


Fig. 8 TTL output circuit

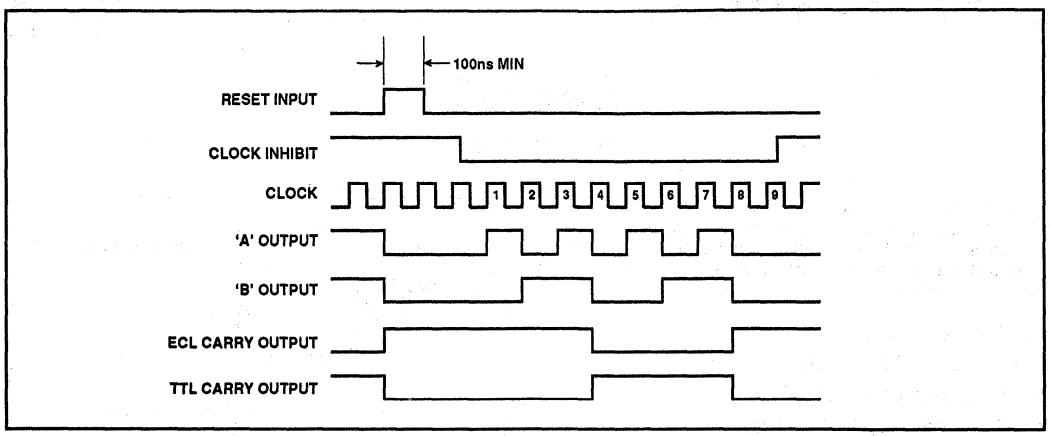


Fig.9 Timing diagram

SP8741

300MHz÷6/7

The SP 8741 is an ECL ÷6/7 two-modulus divider, with ECL10K compatible outputs. It divides by 6 when either of the ECL control inputs, $\overline{PE1}$ or $\overline{PE2}$, is in the high state and by 7 when both are low (or open circuit). An AC coupled input of 600mVp-p is required.

FEATURES

- ECL Compatible Outputs
- AC-Coupled Input (Internal Bias)
- ECL Compatible Control Inputs

QUICK REFERENCE DATA

- Supply Voltage: −5·2V
- Power Consumption: 240mW
- Temperature Range: −55°C to +125°C

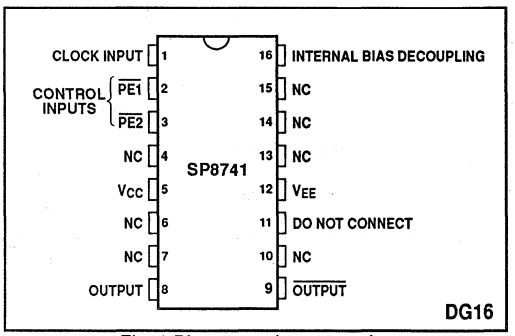


Fig. 1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage	−8V
Output current	20mA
Storage temperature range	−65°C to +150°C
Max. junction temperature	+175°C
Max. clock input voltage	2·5V p-p

ORDERING INFORMATION

SP8741 A DG
5962-91590 (SMD)

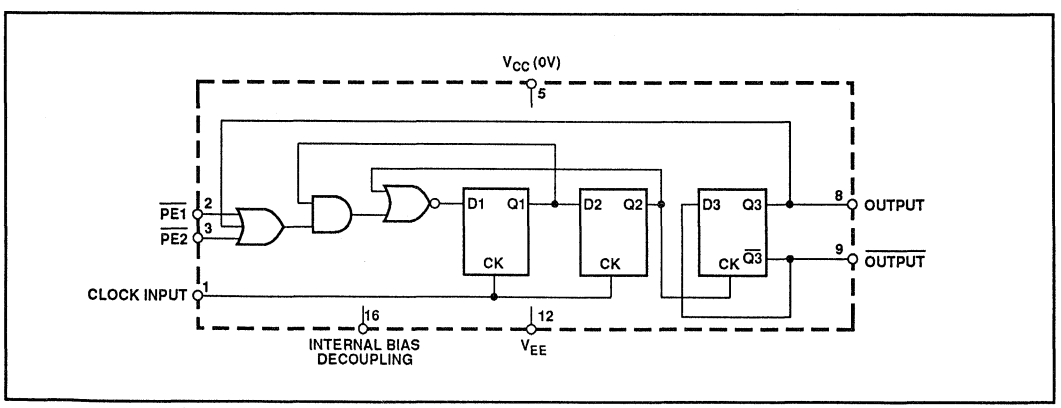


Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range

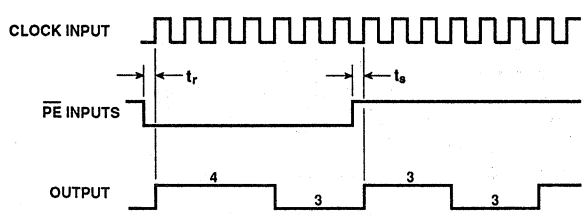
Supply voltage, V_{CC} = 0V, V_{EE} = −5·2V ± 0·25V

Temperature, T_{AMB} = −55°C to +125°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{MAX}	300		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f_{MIN}		40	MHz	Input = 400-800mV p-p	
Power supply current	I_{EE}		60	mA	V_{EE} = −5·2V	
Output high voltage	V_{OH}	−0·85	−0·7	V	V_{EE} = −5·2V (25°C)	
Output low voltage	V_{OL}	−1·8	−1·5	V	V_{EE} = −5·2V (25°C)	
$\overline{PE}$ input high voltage	V_{INH}	−0·93		V	V_{EE} = −5·2V (25°C)	
$\overline{PE}$ input low voltage	V_{INL}		−1·62	V	V_{EE} = −5·2V (25°C)	
Clock to output delay	t_p		6	ns		5
Set-up time	t_s	2·5		ns		3, 5
Release time	t_r	3		ns		4, 5

NOTES

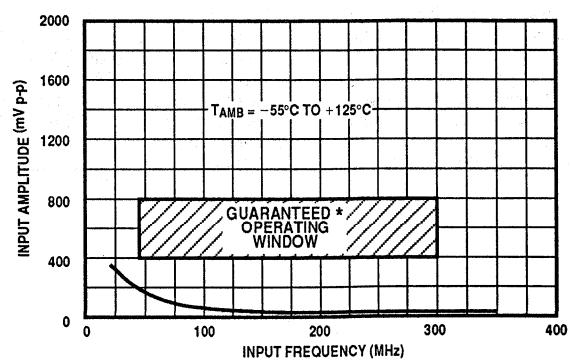
1. The temperature coefficients of V_{OH} = +1·63mV/°C, V_{OL} = +0·94mV/°C and of V_{IN} = +1·22mV/°C.
2. The test configuration for dynamic testing is shown in Fig.6.
3. The set-up time t_s is defined as the minimum time that can elapse between L→H transition of control input and the next L→H clock pulse transition to ensure that ÷6 is obtained.
4. The release time t_r is defined as the minimum time that can elapse between H→L transition of control input and the next L→H clock pulse transition to ensure that ÷7 is obtained.
5. Guaranteed but not tested.



TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division ratio
L	L	7
H	L	6
L	H	6
H	H	6

Fig. 3 Timing diagram



* Tested as specified in table of Electrical Characteristics

Fig. 4 Typical input characteristic

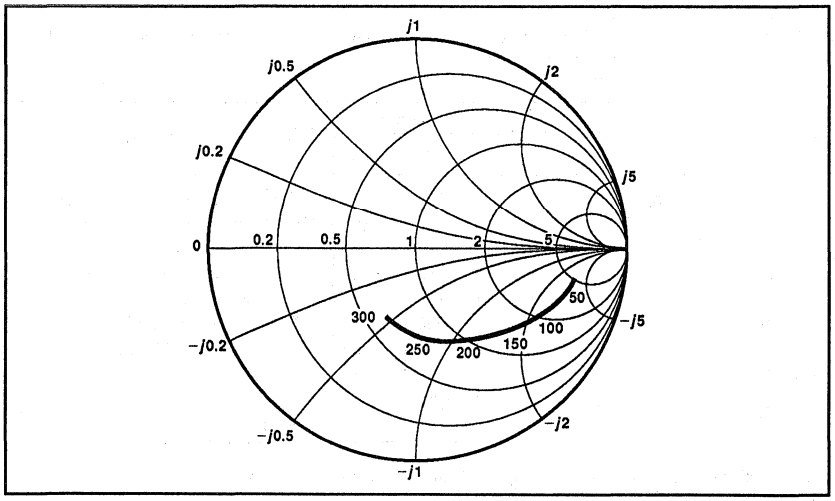


Fig. 5 Typical input impedance. Test conditions: Supply Voltage = −5·2V, Ambient Temperature = 25°C. Frequencies in MHz, impedances normalised to 50Ω.

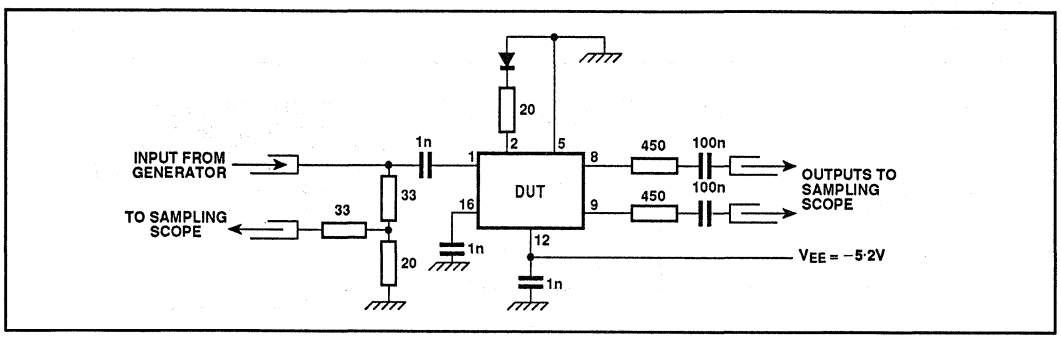


Fig. 6 Test circuit

OPERATING NOTES

1. The clock input is biased internally and is coupled to the signal source with a suitable capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected from pin 16 to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable, it may be prevented by connecting a 15kΩ resistor from the clock input (pin 1) to V_{EE}. This will reduce the input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/µs.
4. The Q and $\overline{Q}$ outputs are compatible with ECLII but can be interfaced to ECL10K as shown in Fig. 7. There is an internal circuit equivalent to a load of 2kΩ at each output.
5. The PE inputs are ECLIII/10K compatible and include 4·3kΩ pulldown resistors. Unused inputs can therefore be left open.
6. The input impedance of the SP8741 varies as a function of frequency, see Fig. 5.
7. All components should be suitable for the frequency in use.

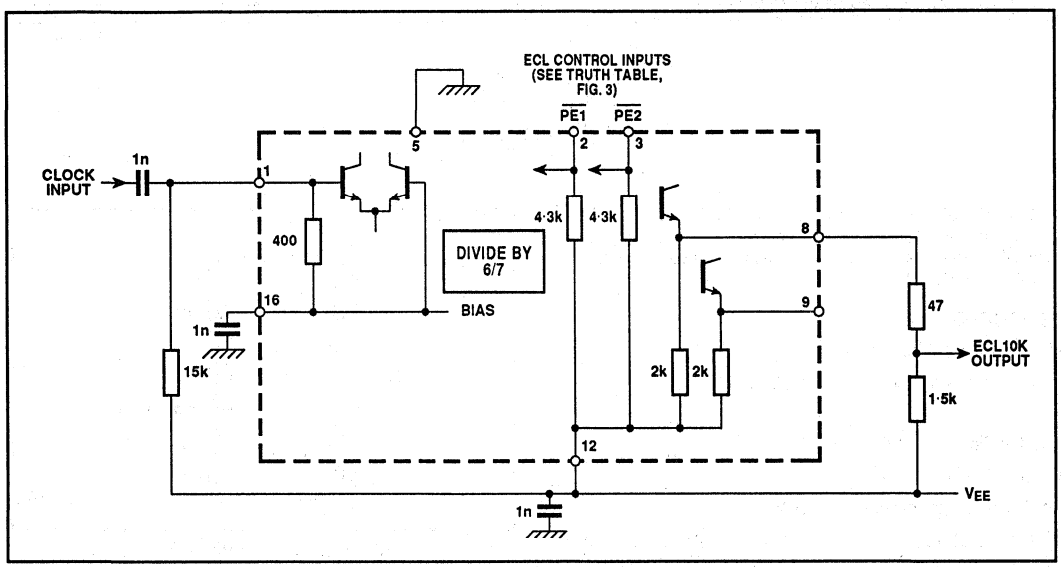


Fig. 7 Typical application circuit showing interfacing

SP8755

1200MHz÷64

The SP8755 is a divide by 64 prescaler which operates from a standard 5V TTL supply and will drive TTL directly. The SP8755A operates over the full military temperature range (−55°C to +125°C).

FEATURES

- TTL Compatible Output
- AC Coupled Input (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: 5V
- Power Consumption: 270mW
- Temperature Range: −55°C to +125°C (A Grade)
  −30°C to +70°C (B Grade)

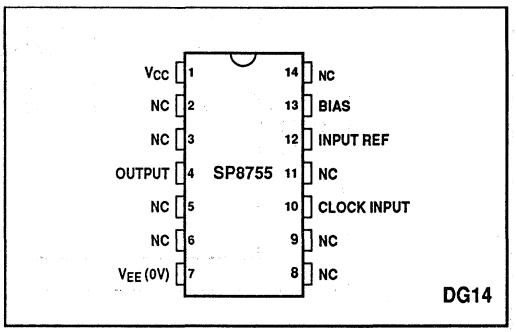


Fig. 1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Output current	±30mA
Storage temperature range	−65°C to +150°C
Max. junction temperature	+175°C
Max. clock input voltage	2·5V p-p

ORDERING INFORMATION

SP8755 A DG
SP8755 B BG
SP8755 NA 1C
5962-88684 (SMD)

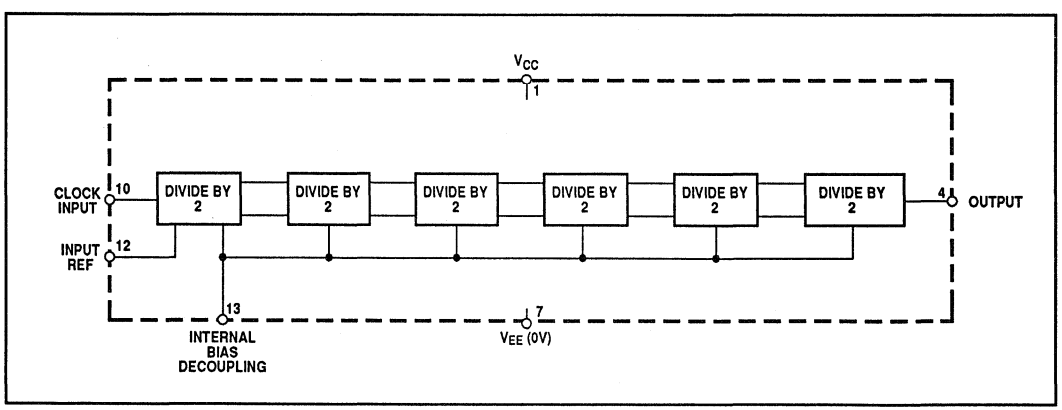


Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range
Supply voltage, V_{CC} = 5·0V±0·25V, V_{EE} = 0V
Temperature, T_{AMB} = −55°C to +125°C (A Grade), −30°C to +70°C (B Grade)

Characteristic	Symbol	Value		Units	Grade	Conditions
		Min.	Max.			
Maximum frequency (sinewave input)	f_{MAX}	1·2		GHz	SP8755A	Input = 600-1200mV p-p
	f_{MAX}	1·2		GHz	SP8755B	Input = 400-1200mV p-p
Minimum frequency (sinewave input)	f_{MIN}		100	MHz	Both	Input = 600-1200mV p-p
Power supply current	I_{CC}		75	mA	Both	
Output high voltage	V_{OH}	2·5		V	Both	
Output low voltage	V_{OL}		0·45	V	Both	Sink current = 5mA

NOTES
1. The test configuration for dynamic testing is shown in Fig.5.
2. Above characteristics are not tested at 25°C only (tested ar low and high temperatures only).

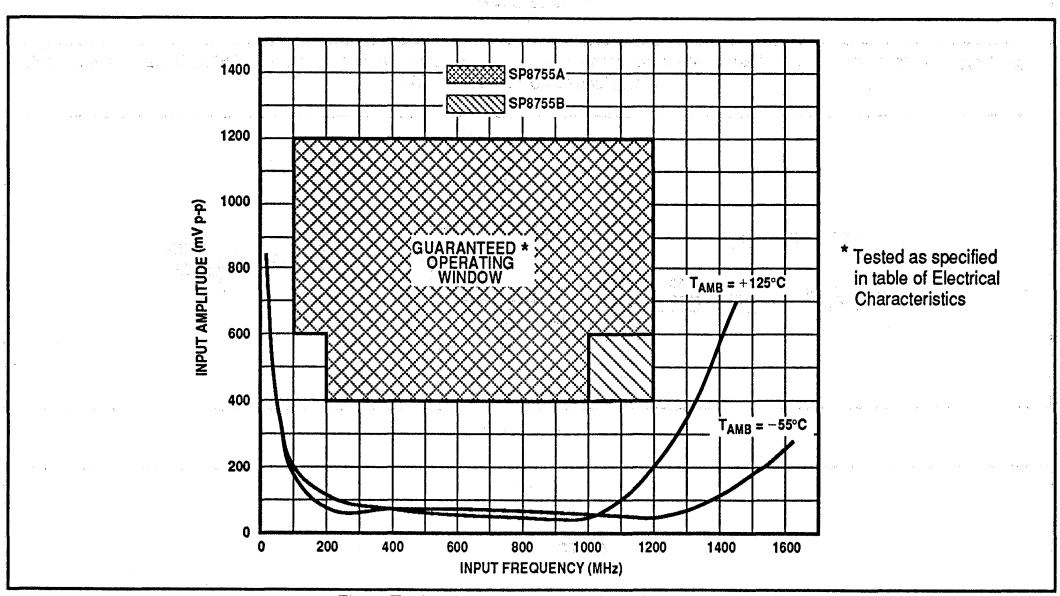


Fig. 3 Typical input characteristic of SP8755A/B

OPERATING NOTES

1. The clock input is biased internally and is connected to the signal source via a capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting an 18kΩ resistor between the input and V_{EE} (i.e. from pin 10 to pin 7). This will reduce sensitivity by approximately 100mV.
3. The device will operate down to DC but input slew rate must be better than 100V/µs.
4. The output is a standard totem pole TTL and can therefore be interfaced directly to TTL.

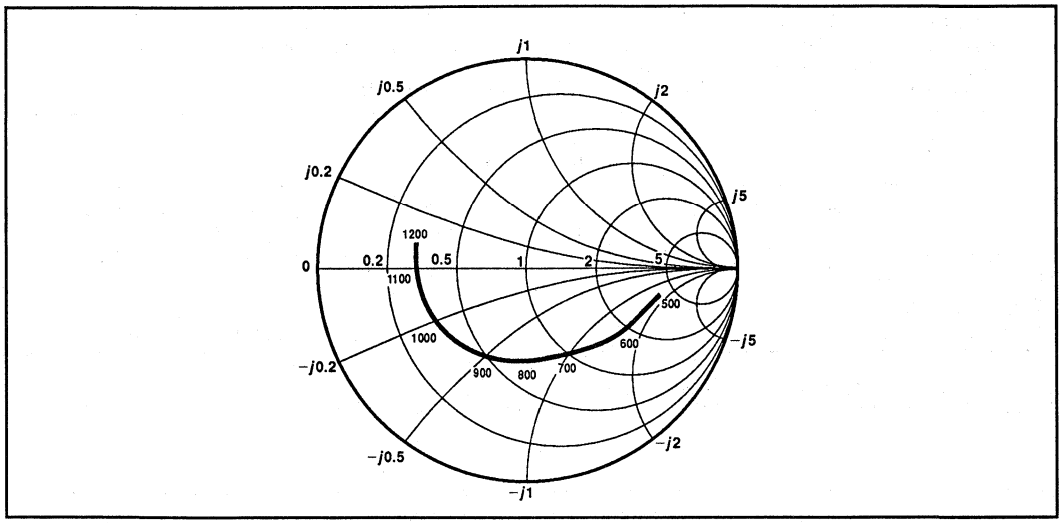


Fig. 4 Typical input impedance. Test conditions: supply voltage = 5·2V, ambient temperature = 25°C, frequencies in MHz, Impedances normalised to 50Ω

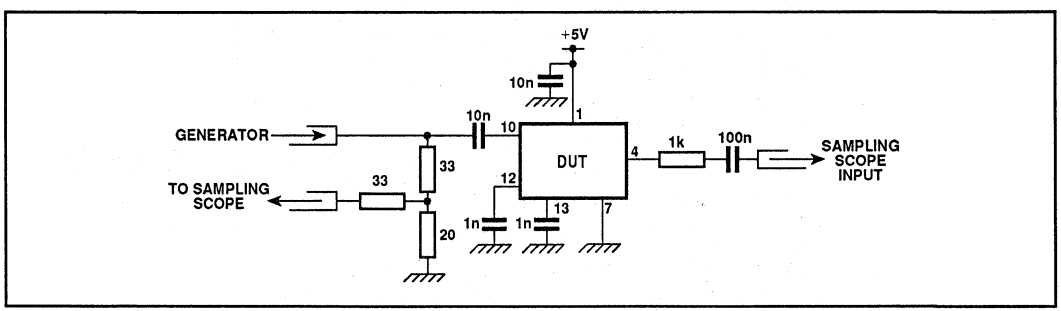


Fig. 5 Test circuit

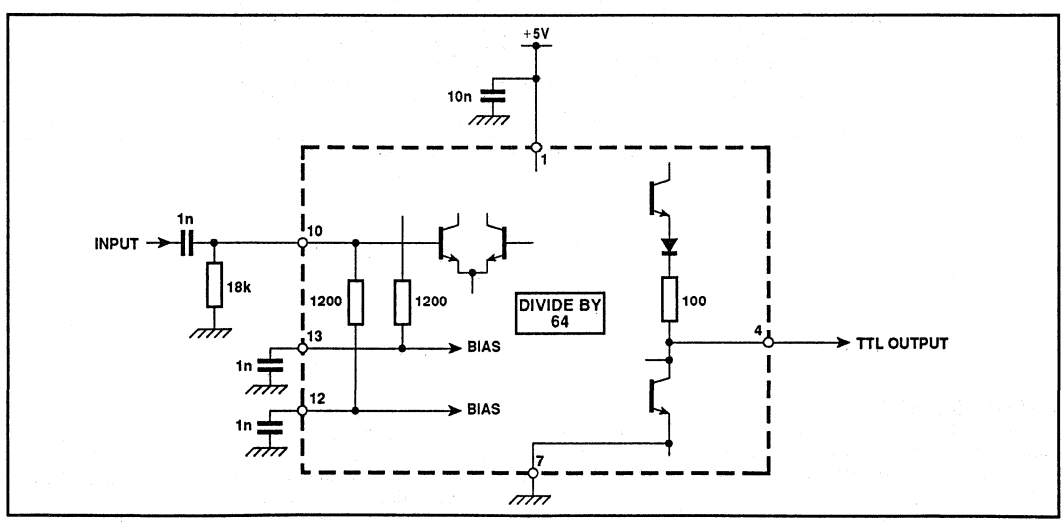


Fig. 6. Typical application circuit showing interfacing

SP8789

225MHz ÷ 20/21 TWO MODULUS DIVIDER

The SP8789 is a low power programmable ÷20/21 counter.It divides by 20, when the control input is in the high state and by 21 when in the low state. An internal voltage regulator allows operation from a wide range of supply voltages.

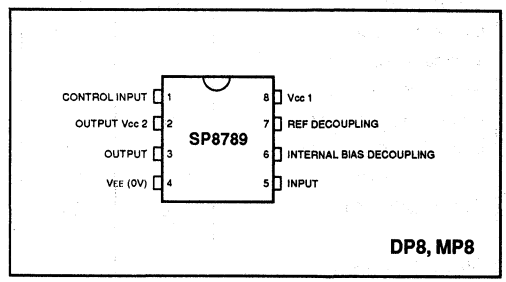


Figure 1 Pin connections - top view

FEATURES

- Very Low Power
- Control Input and Output CMOS/TTL Compatible
- AC Coupled Input
- Operation up to 9.5V using Internal Regulator

QUICK REFERENCE DATA

- Supply Voltage 5.2V or 6.8V to 9.5V
- Power consumption: 26mW Typical
- Temperature range: -40°C to +85°C

ABSOLUTE MAXIMUM RATINGS

Supply voltage	6.0V pins 7 & 8 tied
Supply voltage	13.5V pin 8, pin 7 decoupled
Storage temperature range	-55°C to +125°C
Max. Junction temperature	+175°C
Max. clock input voltage	2.5V p-p
Vcc2	Max. 10V

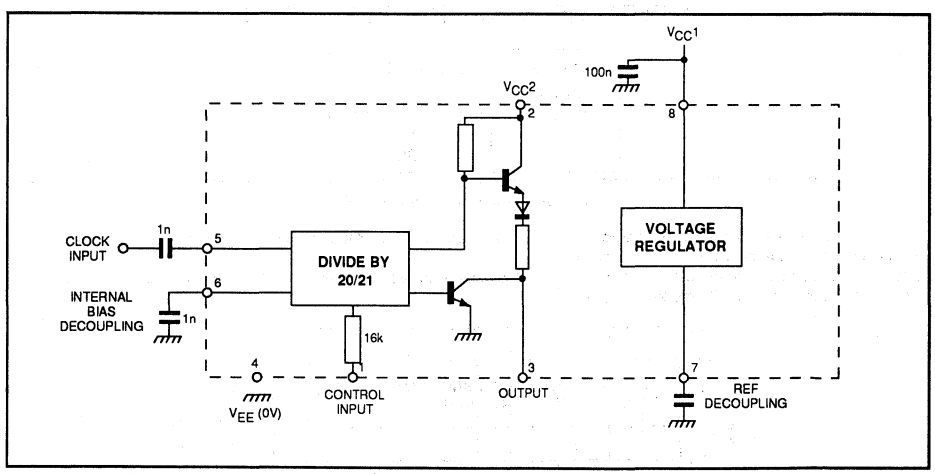


Figure 2 : Functional diagram SP8789

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):]

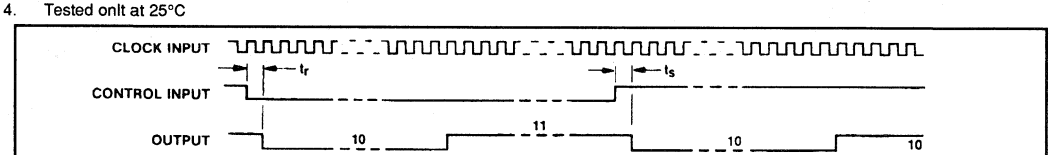
Supply voltage : Vcc 1 & 2 = 5.2 ± 0.25V or 6.8V to 9.5V (see Operating Note 7):

V_{EE} = 0V; Temperature T_{amb} = -40°C to +85°C

Characteristics	Symbol	Value		Units	Notes	Conditions
		Min.	Max.			
Maximum frequency (sinewave input))	f_{max}	225		MHz	Note 4	Input = 200-800mV p-p
Minimum frequency (sinewave input)	f_{min}		20	MHz	Note 4	Input = 400-800mV p-p
Power supply current	I_{EE}		7	mA	Note 4	
Control input high voltage	V_{INH}	4		V	Note 4	
Control input low voltage	V_{INL}		2	V	Note 4	
Output high voltage	V_{OH}	2.4		V	Note 4	Pins 2, 7 and 8 linked Vcc = 4.95V I_{OH} = 100µA
Output low voltage	V_{OL}		0.5	V	Note 4	Pin 2 linked to 8 and 7 I_{OL} = 1.6mA
Set up time	t_s	14		ns	Note 3	25°C
Release time	t_r	20		ns	Note 3	25°C
Clock to output propagation time	t_p		45	ns	Note 3	25°C

NOTES

1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. Guaranteed but not tested.
4. Tested onlt at 25°C



TRUTH TABLE FOR CONTROL INPUTS

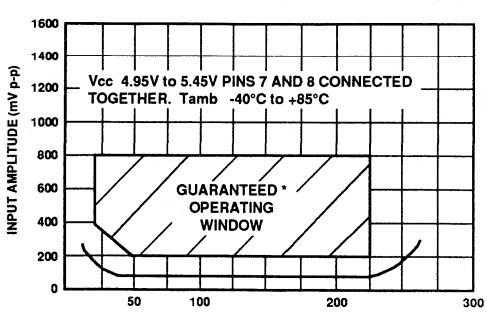
Control input	Division Ratio
0	21
1	20

Figure 3 : Timing diagramSP8789

NOTES

The set-up time ts is defined as the minimum time that can elapse between a L → H transition of the control input and the next L → H clock pulse transition to ensure that the ÷ 20 mode is selected.

The release time tr is defined as the minimum time that can elapse between a H → L transition of the control input and the next L → H clock pulse transition to ensure that the ÷ 21 mode is selected.



*Tested as specified in table of Electrical Characteristics

Figure 4 SP8789

OPERATING NOTES

1. The clock input (Pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, Pin 6 to ground.
2. The output stage which is normally open collector (Pin 2 open circuit) can be interfaced to CMOS. The open collector canbereturnedtoa +10Vlineviaa5kresistorbuttheoutput sink current should not exceed 2mA. If interfacing to TTL is required then Pins 2 and 7 should be connected together to give a fan-out = 1. This will increase supply current by approximately 2mA.
3. The circuit will operate down to DC but a slew rate of better than 20V/~s is required.
4. The mark space ratio of the output is approximately 1.2:1 at 200MHz.
5. Input impedance is a function of frequency. See Fig.5.
6. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 150k between unused input and ground. This reduces the input sensitivity by typically 50-100mV p-p.
7. The internal regulator has its input connected to Pin 8, while the internal reference voltage appears at Pin 7 and should be decoupled. For use from a 5.2V supply, Pins 7 and 8 should be connected together, and 5.2V applied to these pins. For operation from supply voltages in the range +6.8V to +9.5V, Pins 7 and 8 should be separately decoupled, and the supply voltage applied to Pin 8.

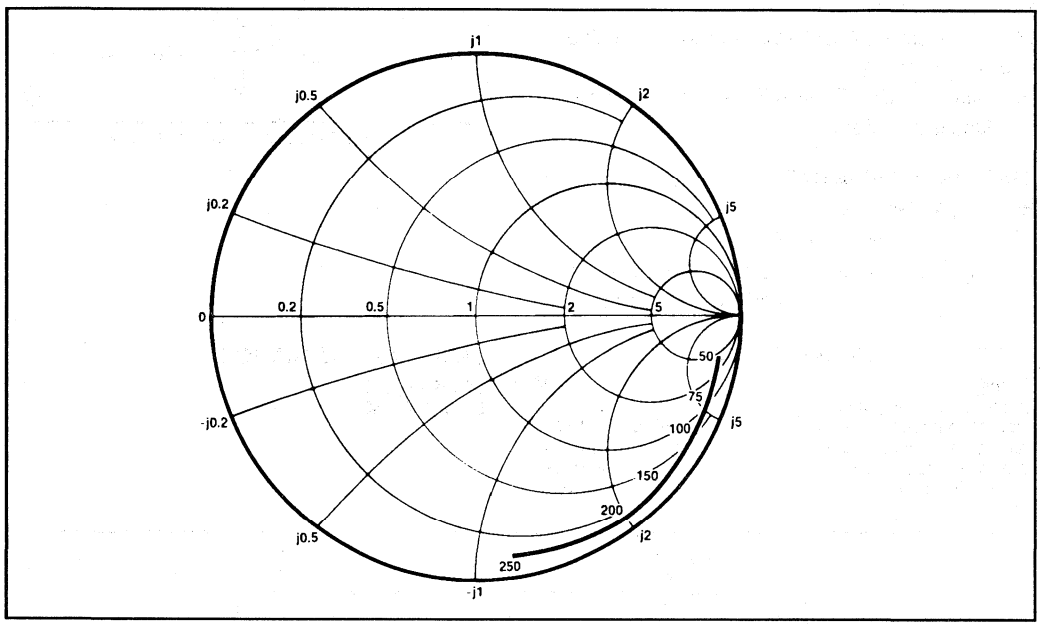


Figure 5 : Typical impedance. Test conditions: supply voltage 5.2V, ambient temperature 25°C, frequencies in MHz, impedance normalised to 50 ohms.

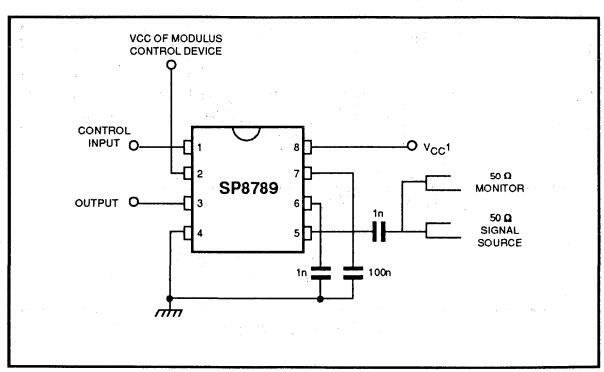


Figure 6 : Toggle frequency test circuit

SP8790

60MHz÷4 (2-MODULUS EXTENDER)

The SP8790 is a divide-by-four counter designed for use with 2-modulus dividers. It increases the minimum division ratio of the 2-modulus divider while retaining the same difference in division ratio. The device is suitable for use in low power frequency synthesis interfacing to CMOS or TTL.

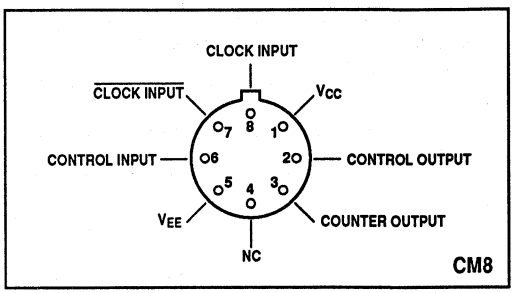


Fig. 1 Pin connections - bottom view

FEATURES

- Very Low Power
- Control Input and Counter Output will Interface Directly to TTL or CMOS
- Interfaces to GPS SP8000 Series Programmable 2-Modulus Dividers

QUICK REFERENCE DATA

- Supply Voltage: 5·0V
- Power Consumption: 40mW
- Temperature Range: −55°C to +125°C (A Grade)
  −30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Open collector output voltage	12V
Storage temperature range	−65°C to +150°C
Max. junction temperature	+175°C
Max. clock input voltage	2·5V p-p
Output sink current	10mA

ORDERING INFORMATION

SP8790 A CM
SP8790 B CM

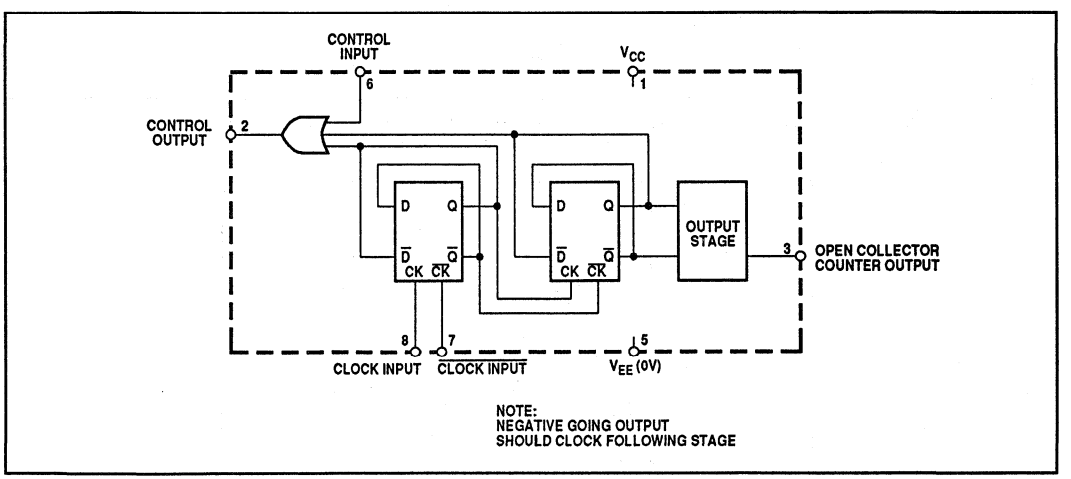


Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range
Supply voltage, V_{CC} = 5V ±0·25V, V_{EE} = 0V
Temperature, T_{AMB} = −55°C to +125°C (A Grade), −30°C to +70°C (B Grade)

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{MAX}	60		MHz	Tested as a controller, see Fig. 4	2
Power supply current	I_{CC}		11	mA		2
Control input high voltage	V_{INH}	3·5	10	V		2
Control input low voltage	V_{INL}	0	1·5	V		2
Output high voltage (pin 3)	V_{OH}	9		V	Pin 3 via 1·6kΩ to+10V	2
Output low voltage (pins 3)	V_{OL}		0·4	V	Pin 3 via 1·6kΩ to+10V	2
Output high voltage (pin 2)	V_{OH}	4·27	4·5	V	V_{CC} = 5·2V (25°C)	
Output low voltage (pin 2)	V_{OL}	3·28	3·7	V	V_{CC} = 5·2V (25°C)	
Clock to counter output −ve going delay	t_{pHL}		25	ns		3
Clock to counter output +ve going delay	t_{pLH}		40	ns		3
Clock to control output −ve going delay	t_{pHL}		15	ns	10kΩ pull-down on control output	3, 4
Clock to control output +ve going delay	t_{pLH}		26	ns	10kΩ pull-down on control output	3, 4
Control input to control output −ve going delay	t_{pHL}		12	ns	10kΩ pull-down on control output	3, 4
Control input to control output +ve going delay	t_{pLH}		16	ns	10kΩ pull-down on control output	3, 4

NOTES
1. The test configuration for dynamic testing is shown in Fig.4.
2. Tested at low and high temperatures only.
3. Guaranteed but not tested.
4. The propagation delays stated are with the device controlling the SP8695, which has internal 10kΩpull-down resistors on its $\overline{PE}$ inputs. These propagation delays will be reduced when the device is used with the SP8643/47 and SP8740 series of 2-modulus dividers, which have internal 4·3kΩ pull-downs. Refer to relevant data sheet/s.

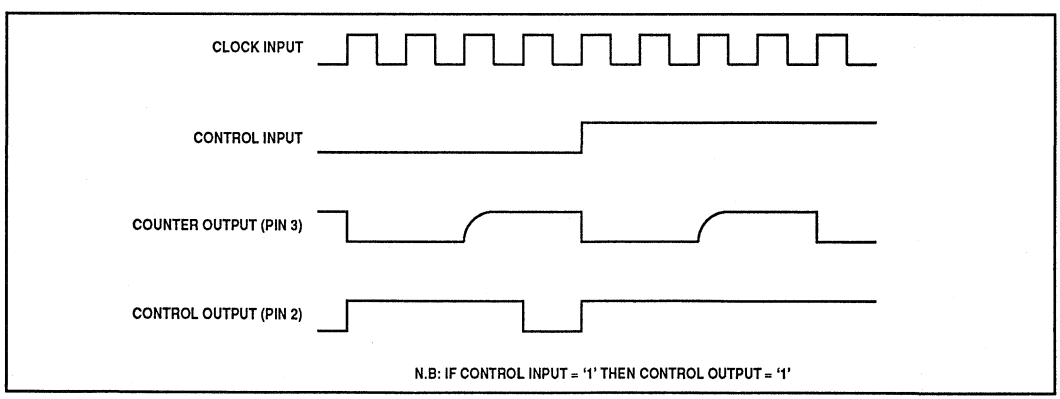


Fig. 3 Timing diagram

OPERATING NOTES

1. The device will normally be driven by capacitively coupling the inputs to the outputs of a 2-modulus divider, as shown in Figs. 4 and 5. The maximum frequency of the device when used as a controller is limited by the internal delays to 60MHz. However, when used as a ÷4 prescaler, it will operate at frequencies in excess of 80MHz, the maximum frequency being limited by saturation of the output stage.
2. The device is normally driven from very fast edges of a 2-modulus divider, in which case there is no input slew rate problem.
3. The control input is TTL/CMOS compatible.
4. The counter output (pin 3) interfaces to TTL/CMOS by the addition of a pull-up resistor. For interfacing to CMOS, the output can be connected with a pull-up resistor to a supply which must not exceed 12V.
5. When used as a controller the device will self-oscillate in the absence of an input signal; this can be prevented by connecting a 47kΩ resistor from pin 7 to ground, as shown in Fig. 5.
6. The control output, which includes an internal 16kΩ pull-down resistor, is ECL compatible and will interface directly to ECL 2-modulus dividers such as the GPS SP8600 and SP8700 series as shown in Figs. 4 and 5.

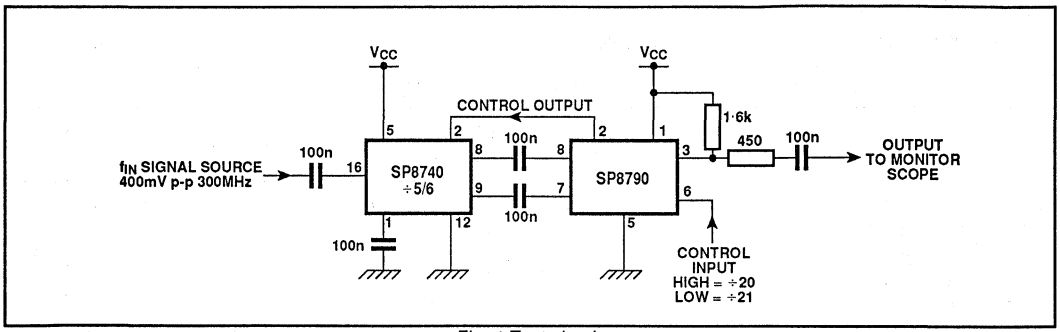


Fig. 4 Test circuit

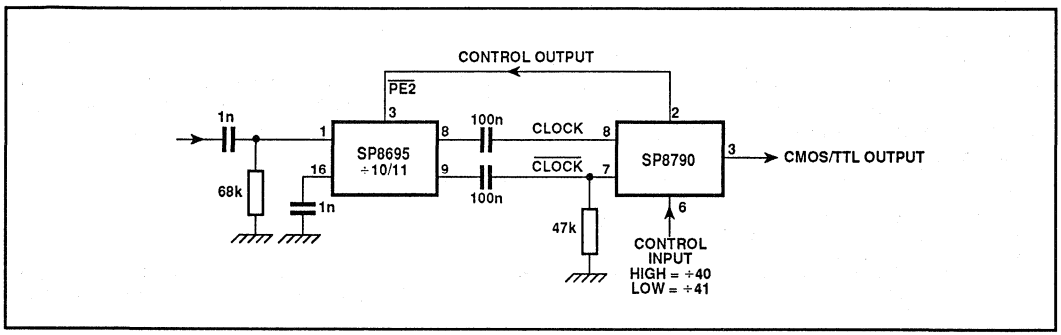


Fig. 5 Typical interfacing to suppress oscillation with no input signal

SP8794

60MHz÷8 (2-MODULUS EXTENDER)

The SP8794 is a divide-by-eight counter designed for use with 2-modulus dividers. It increases the minimum division ratio of the 2-modulus divider while retaining the same difference in division ratio. The device is suitable for use in low power frequency synthesis interfacing to CMOS or TTL.

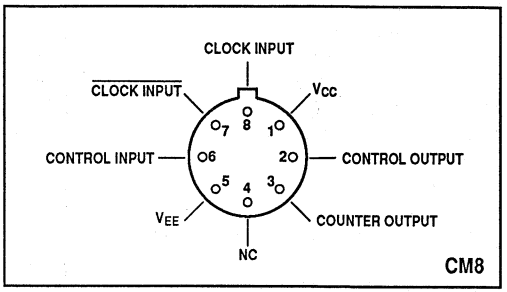


Fig. 1 Pin connections - bottom view

FEATURES

- Very Low Power
- Control Input and Counter Output will Interface Directly to TTL or CMOS
- Interfaces to GPS SP8000 Series Programmable 2-Modulus Dividers

QUICK REFERENCE DATA

- Supply Voltage: 5·0V
- Power Consumption: 40mW
- Temperature Range: −55°C to +125°C (A Grade)
  −30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Open collector output voltage	12V
Storage temperature range	−65°C to +150°C
Max. junction temperature	+175°C
Max. clock input voltage	2·5V p-p
Output sink current	10mA

ORDERING INFORMATION

SP8794 A CM
SP8794 B CM
SP8794 AC CM

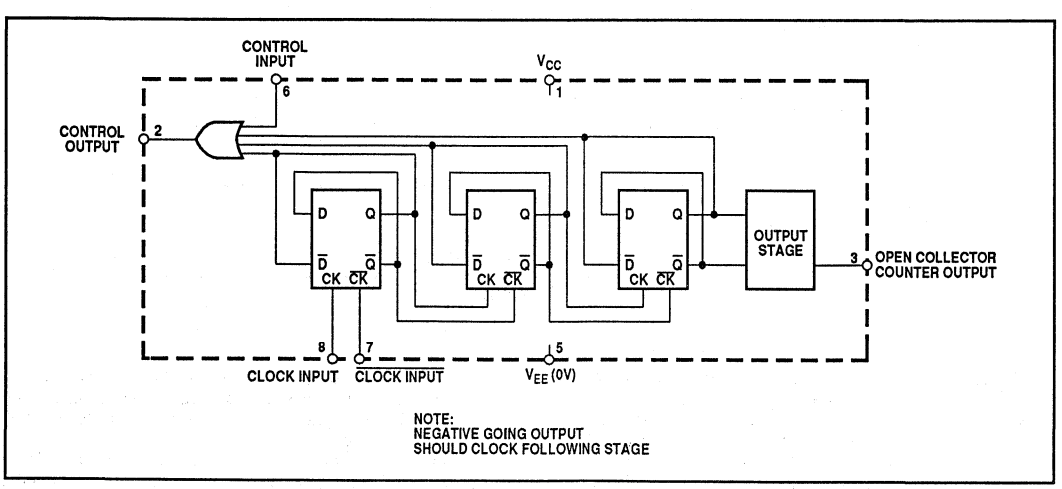


Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range
Supply voltage, V_{CC} = 5V ±0·25V, V_{EE} = 0V
Temperature, T_{AMB} = −55°C to +125°C (A Grade), −30°C to +70°C (B Grade)

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{MAX}	60		MHz	Tested as a controller, see Fig. 4	2
Power supply current	I_{CC}		11	mA		2
Control input high voltage	V_{INH}	3·5	10	V		2
Control input low voltage	V_{INL}	0	1·5	V		2
Output high voltage (pin 3)	V_{OH}	9		V	Pin 3 via 1·6kΩ to+10V	2
Output low voltage (pins 3)	V_{OL}		0·4	V	Pin 3 via 1·6kΩ to+10V	2
Output high voltage (pin 2)	V_{OH}	4·27	4·5	V	V_{CC} = 5·2V (25°C)	
Output low voltage (pin 2)	V_{OL}	3·28	3·7	V	V_{CC} = 5·2V (25°C)	
Clock to counter output −ve going delay	t_{pHL}		27	ns		3
Clock to counter output +ve going delay	t_{pLH}		48	ns		3
Clock to control output −ve going delay	t_{pHL}		15	ns	10kΩ pull-down on control output	3, 4
Clock to control output +ve going delay	t_{pLH}		26	ns	10kΩ pull-down on control output	3, 4
Control input to control output −ve going delay	t_{pHL}		12	ns	10kΩ pull-down on control output	3, 4
Control input to control output +ve going delay	t_{pLH}		16	ns	10kΩ pull-down on control output	3, 4

NOTES
1. The test configuration for dynamic testing is shown in Fig.4.
2. Tested at low and high temperatures only.
3. Guaranteed but not tested.
4. The propagation delays stated are with the device controlling the SP8695, which has internal 10kΩpull-down resistors on its $\overline{PE}$ inputs. These propagation delays will be reduced when the device is used with the SP8643/47 and SP8740 series of 2-modulus dividers, which have internal 4·3kΩ pull-downs. Refer to relevant data sheet/s.

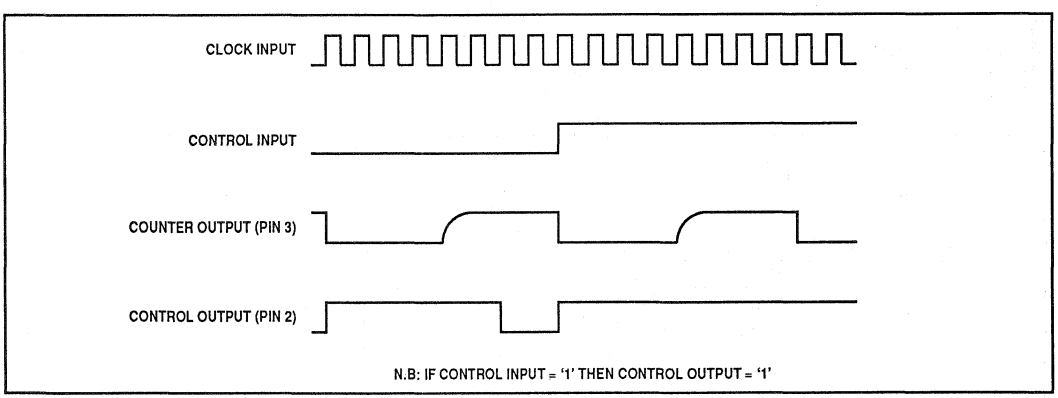


Fig. 3 Timing diagram

OPERATING NOTES

1. The device will normally be driven by capacitively coupling the inputs to the outputs of a 2-modulus divider, as shown in Figs. 4 and 5. The maximum frequency of the device when used as a controller is limited by the internal delays to 60MHz. However, when used as a ÷4 prescaler, it will operate at frequencies in excess of 120MHz, the maximum frequency being limited by saturation of the output stage.
2. The device is normally driven from very fast edges of a 2-modulus divider, in which case there is no input slew rate problem.
3. The control input is TTL/CMOS compatible.
4. The counter output (pin 3) interfaces to TTL/CMOS by the addition of a pull-up resistor. For interfacing to CMOS, the output can be connected with a pull-up resistor to a supply which must not exceed 12V.
5. When used as a controller the device will self-oscillate in the absence of an input signal; this can be prevented by connecting a 47kΩ resistor from pin 7 to ground, as shown in Fig. 5.
6. The control output, which includes an internal 16kΩ pull-down resistor, is ECL compatible and will interface directly to ECL 2-modulus dividers such as the GPS SP8600 and SP8700 series as shown in Figs. 4 and 5.

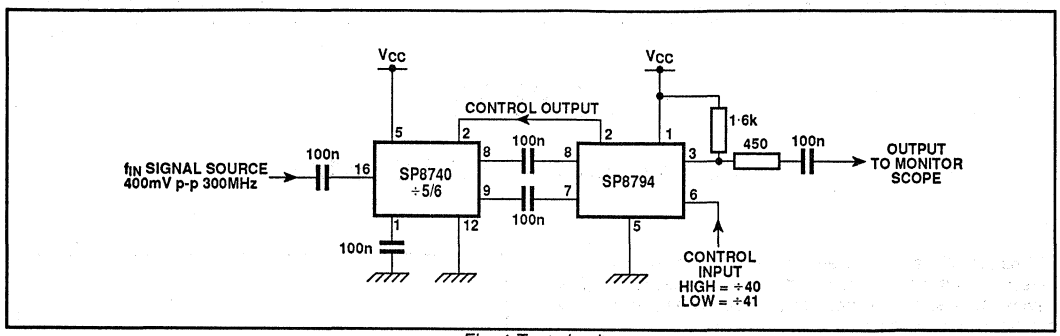


Fig. 4 Test circuit

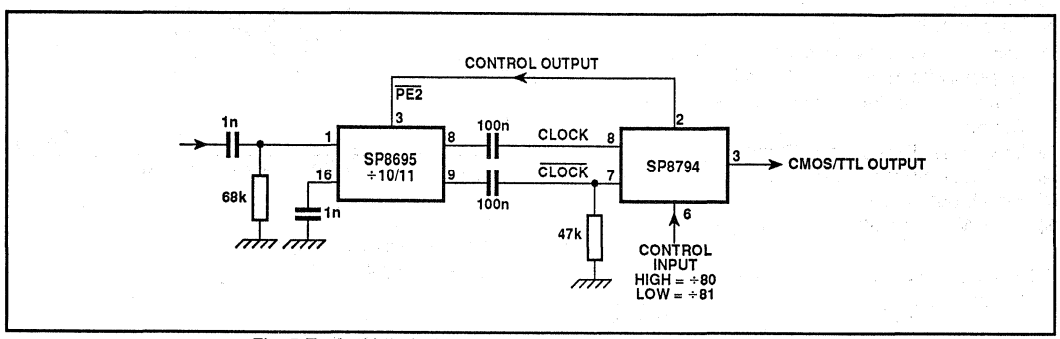


Fig. 5 Typical interfacing to suppress oscillation with no input signal

SP8801

3.3GHz ÷16 FIXED MODULUS DIVIDER

The SP8801 is one of a range of very high speed low power prescalers for professional and military applications. The device features a complementary output stage with on chip current source for the emitter follower outputs.

FEATURES

- Very High Speed Operation 3.3GHz
- Silicon Technology for low Phase Noise (Typically better than –150dBc/Hz)
- Specified Over the Full Military Temperature Range
- Low Power Dissipation 375mW (typ)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock Input voltage	2.5V p–p
Storage temperature Range	–65°C to +150°C
Junction temperature	+175°C

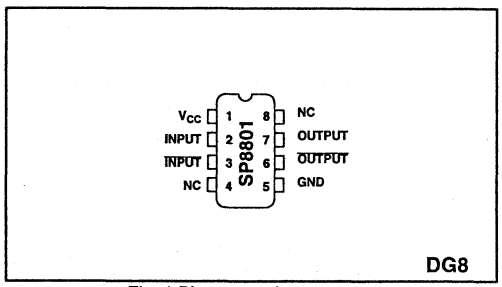


Fig. 1 Pin connections top view

THERMAL CHARACTERISTICS

θja = 150°C/W

ORDERING INFORMATION

SP8801/A/DG Military temperature range

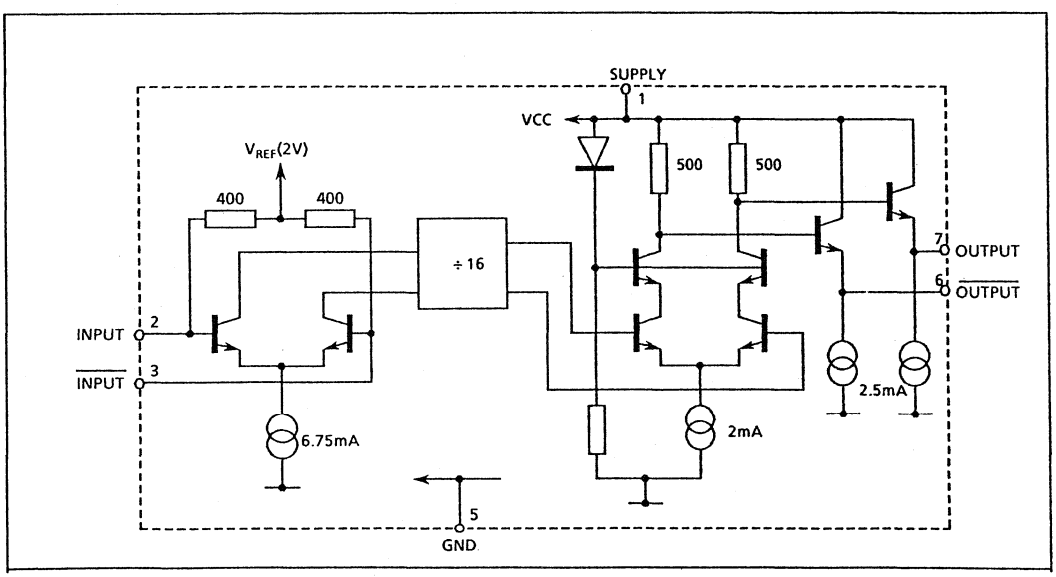


Fig.2 SP8831 Block diagram

ELECTRICAL CHARACTERISTICS

Guaranteed over the temperature range T_{amb} -55°C to +125°C (see note) and supply voltage range 4.75V to 5.25V
Tested at T_{amb} = -55°C and +125°C, V_{CC} = 4.75V and 5.25V.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	1		75	88	mA	V_{CC} = 5V
Input sensitivity 0.65GHz to 2.8GHz 3.3GHz	2, 3			 175 400	 mV mV	RMS sinewave measured in 50Ω system. see Figs. 3 & 4
Input impedance (series equivalent)	2, 3		50 2		Ω pF	
Output Voltage with f_{in} = 650MHz	6, 7	.780	1.04	1.30	Vp-p	V_{CC} = 5V
Output Voltage with f_{in} = 3GHz	6, 7		0.95		Vp-p	V_{CC} = 5V load as Fig. 4

NOTE.
Devices must be used with a suitable heatsink to maintain chip temperature below 175°C when operating at T_{amb} > 105°C

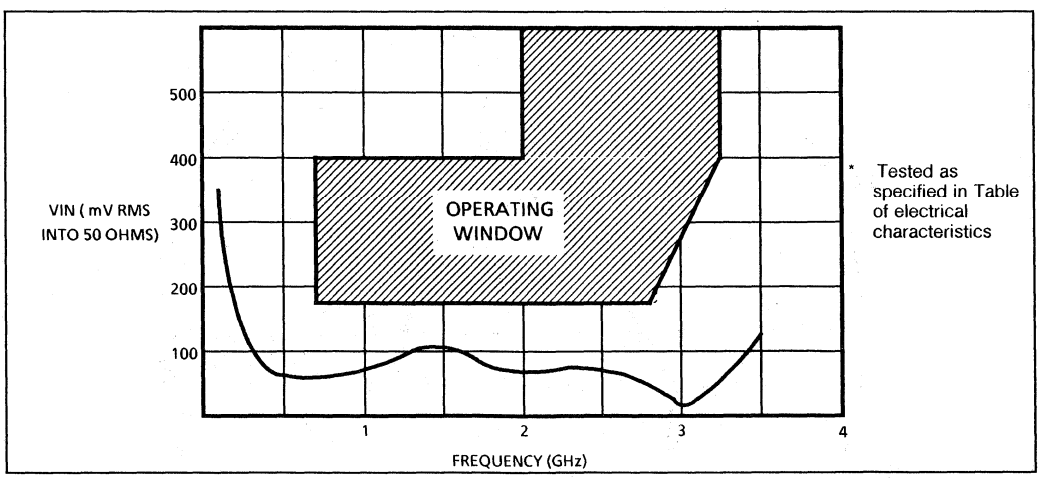


Fig.3 Typical input sensitivity

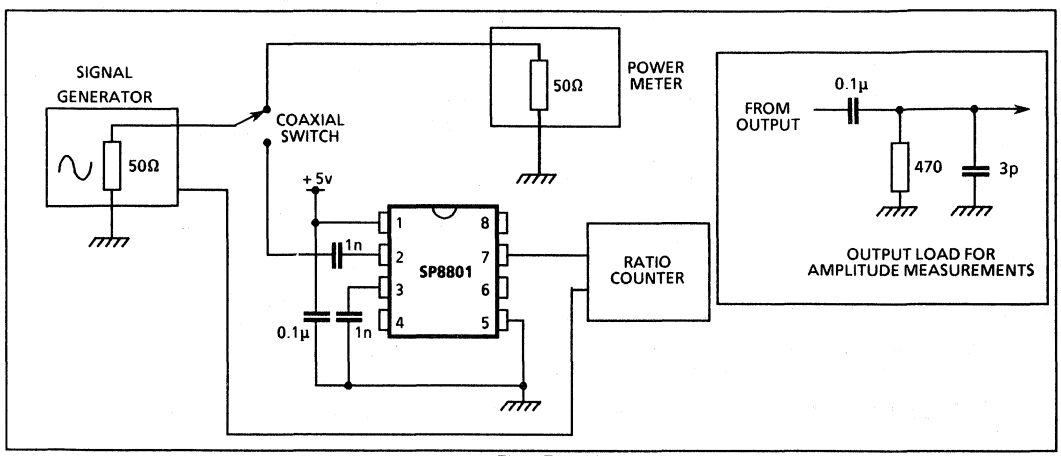


Fig.4 Test circuit

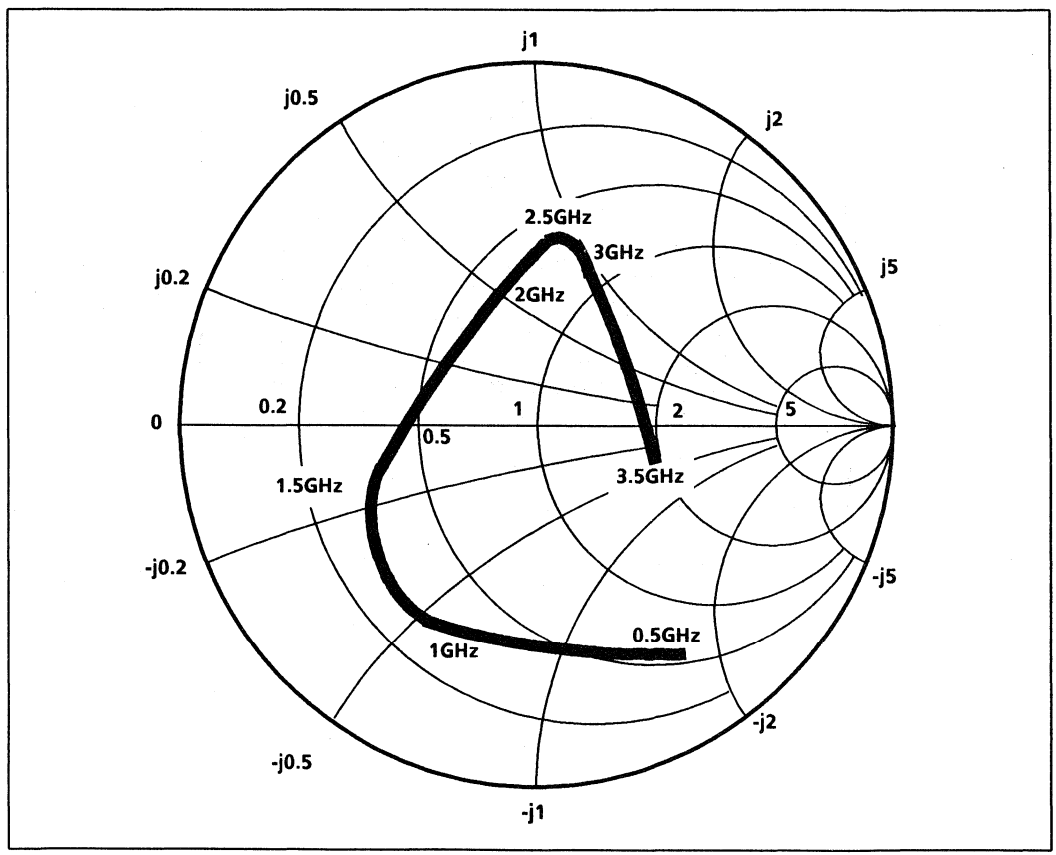


Fig. 5 Typical input impedance

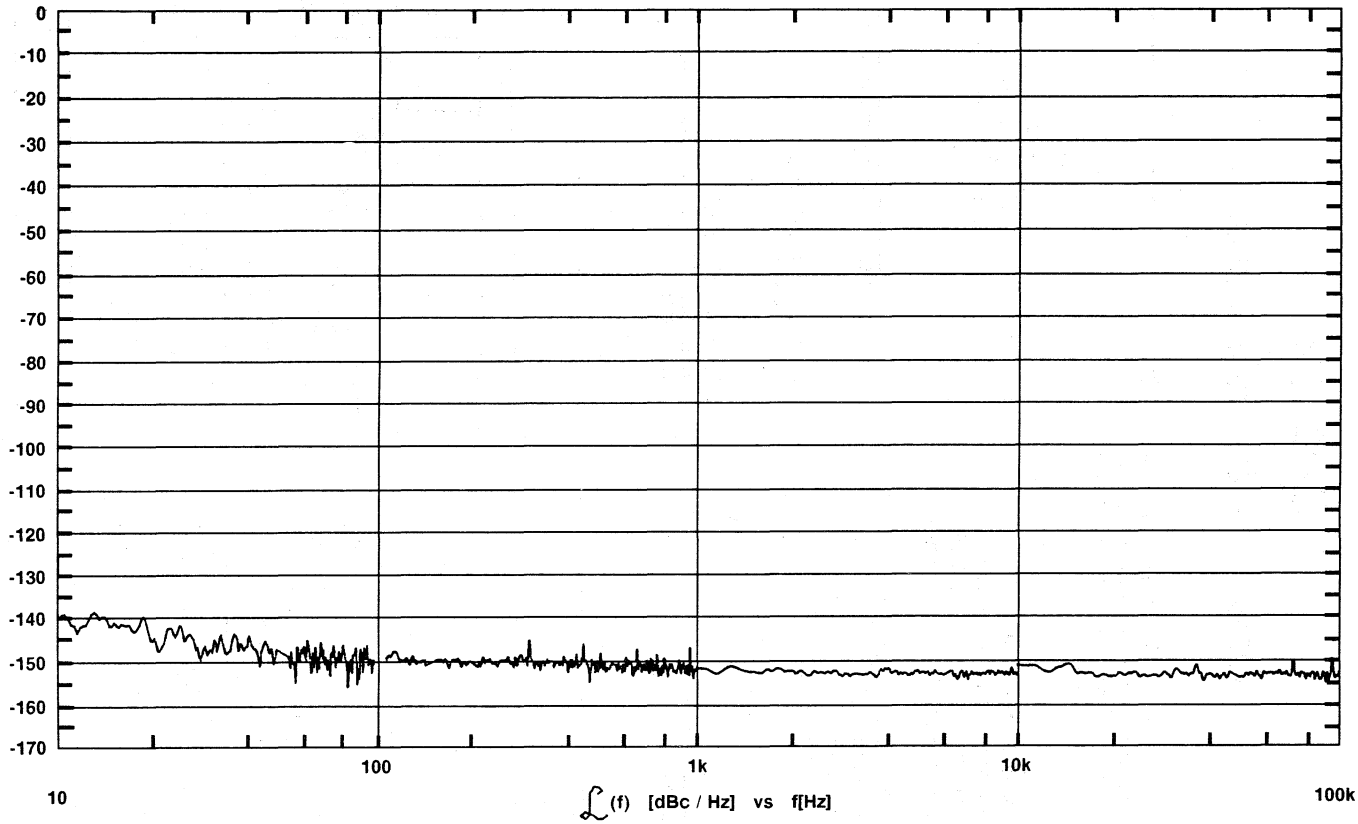


Fig. 6 Typical phase noise of SP8801 at 1GHz carrier

SP8802

3.3GHz ÷2 FIXED MODULUS DIVIDER

The SP8802 is one of a range of very high speed low power prescalers for professional and military applications. The device features a complementary output stage with on chip current source for the emitter follower outputs.

FEATURES

- Very High Speed Operation 3.3GHz
- Silicon Technology for low Phase Noise (Typically better than –140dBc/Hz at 10kHz)
- Specified Over the Full Military Temperature Range
- Low Power Dissipation 420mW (typ)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock Input voltage	2.5V p–p
Storage temperature Range	–65°C to +150°C
Junction temperature	+175°C

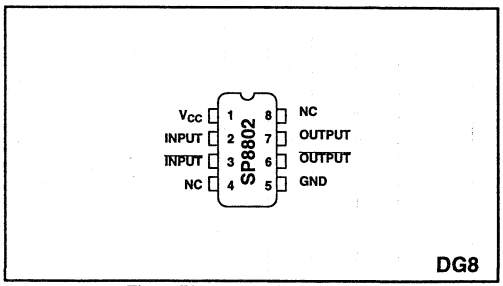


Fig. 1 Pin connections top view

THERMAL CHARACTERISTICS

θja = 150°C/W

ORDERING INFORMATION

SP8802/A/DG Military temperature range
5962–90661(SMD)

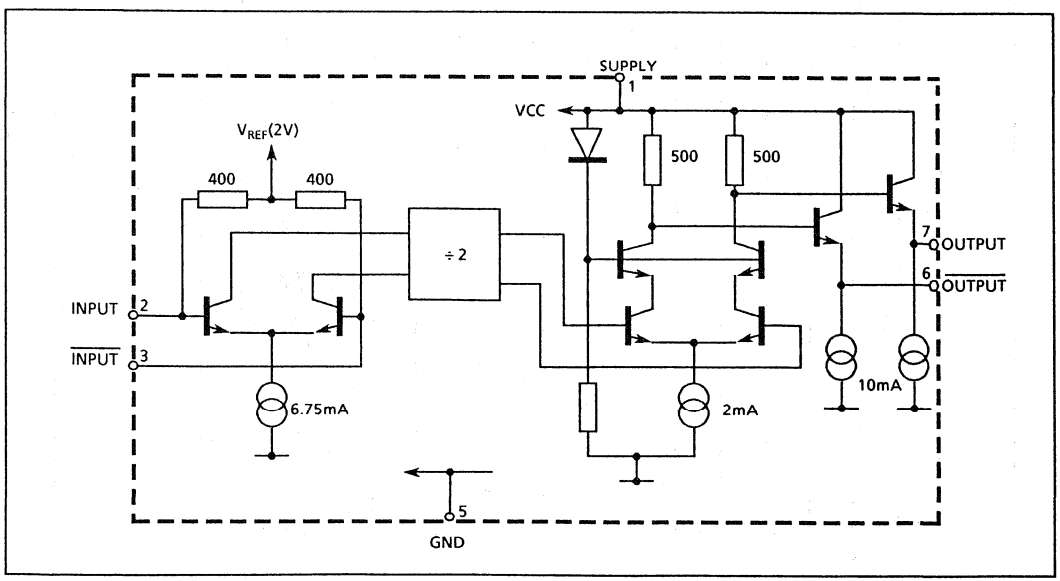


Fig.2 SP8802 Block diagram

ELECTRICAL CHARACTERISTICS

Guaranteed over the temperature range T_{amb} -55°C to +125°C (see note) and supply voltage range 4.75V to 5.25V
Tested at T_{amb} = -55°C and +100°C, V_{CC} = 4.75V and 5.25V.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	1		84	100	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave.
0.65GHz to 2.8GHz				175	mV	measured in 50 ohm system.
3.3GHz				400	mV	see Figs.3&4
Input impedance (series equivalvent)	2,3		50		Ω	
			2		pF	
Output voltage with fin = 1000MHz	6,7	0.8	1		Vp-p	V_{CC} = 5V
Output voltage with fin = 3GHz	6,7		0.35		Vp-p	V_{CC} = 5V Load as Fig. 4

NOTE: Devices must be used with a suitable heatsink to maintain chip temperature below 175°C when operating at T_{amb} > 100°C

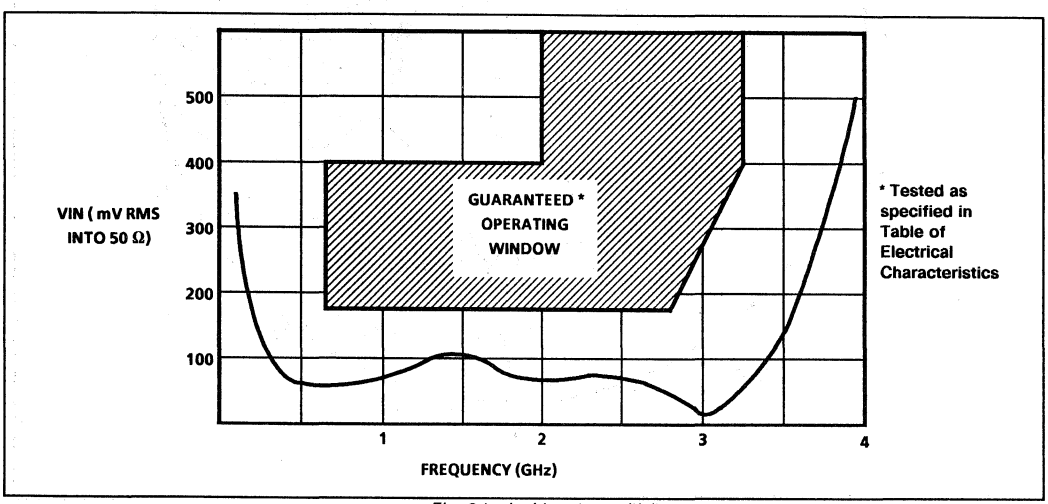


Fig. 3 typical input sensitivity

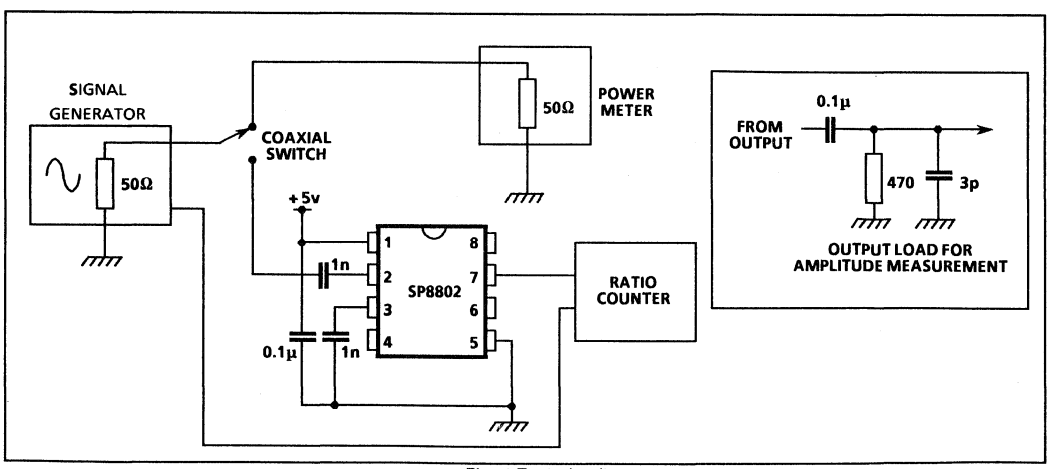


Fig. 4 Test circuit

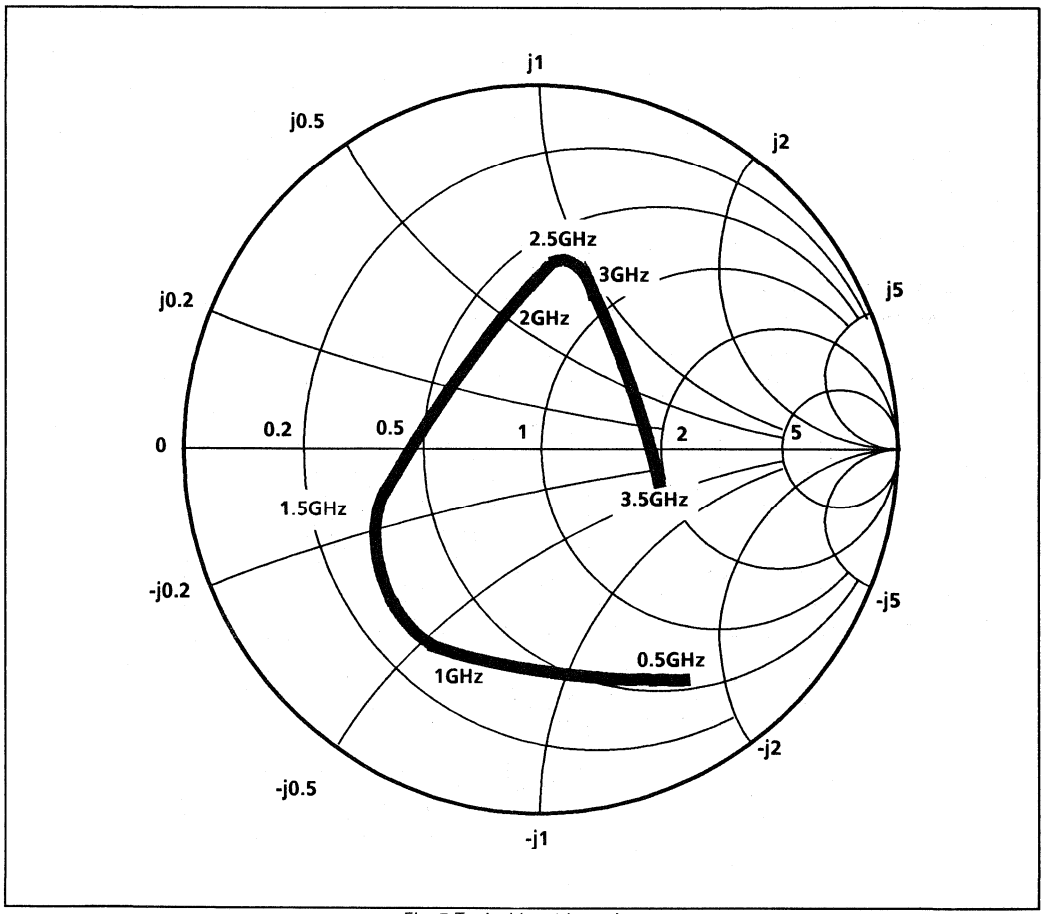


Fig. 5 Typical input impedance

SP8803

3.3GHz ÷32 FIXED MODULUS DIVIDER

The SP8803 is one of a range of very high speed low power prescalers for professional and military applications. The device features a complementary output stage with on chip current source for the emitter follower outputs.

FEATURES

- Very High Speed Operation 3.3GHz
- Silicon Technology for low Phase Noise (Typically better than –150dBc/Hz at 10kHz)
- Specified Over the Full Military Temperature Range
- Low Power Dissipation 390mW (typ)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock Input voltage	2.5V p–p
Storage temperature Range	–65°C to +150°C
Junction temperature	+175°C

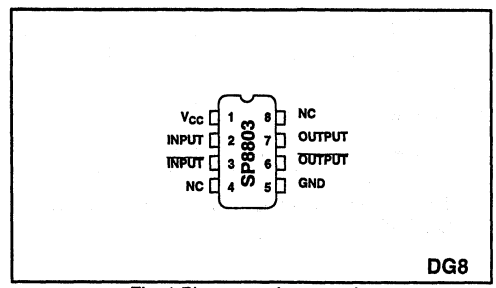


Fig. 1 Pin connections top view

THERMAL CHARACTERISTICS

θja = 150°C/W

ORDERING INFORMATION

SP8803/A/DG Military temperature range

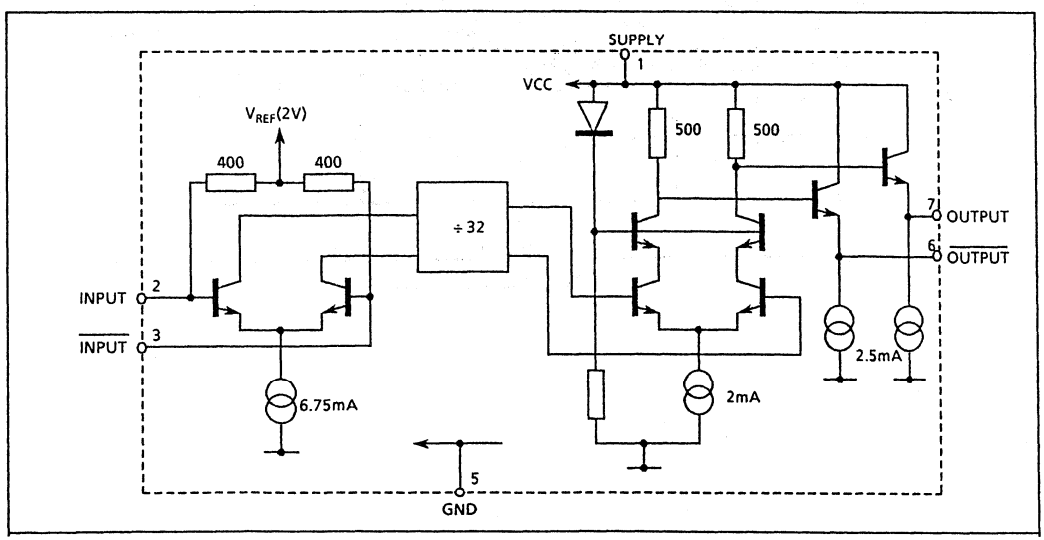


Fig.2 SP8803 Block diagram

ELECTRICAL CHARACTERISTICS

Guaranteed over the temperature range T_{amb} -55°C to +125°C (see note) and supply voltage range 4.75V to 5.25V
Tested at T_{amb} = -55°C and +125°C, V_{CC} = 4.75V and 5.25V.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	1		78	90	mA	V_{CC} = 5V
Input sensitivity	2, 3					RMS sinewave
0.65GHz to 2.8GHz				175	mV	measured in 50Ω
3.3GHz				400	mV	system. see Figs. 3 & 4
Imput impedance (series	2, 3		50		Ω	
equivalent)			2		pF	
Output Voltage with f_{in} = 650MHz	6, 7	.815	1.09	1.36	Vp-p	V_{CC} = 5V
Output Voltage with f_{in} = 3GHz	6, 7		1.03		Vp-p	V_{CC} = 5V load as Fig. 4

NOTE.
Devices must be used with a suitable heatsink to maintain chip temperature below 175°C when operating at T_{amb} > 105°C

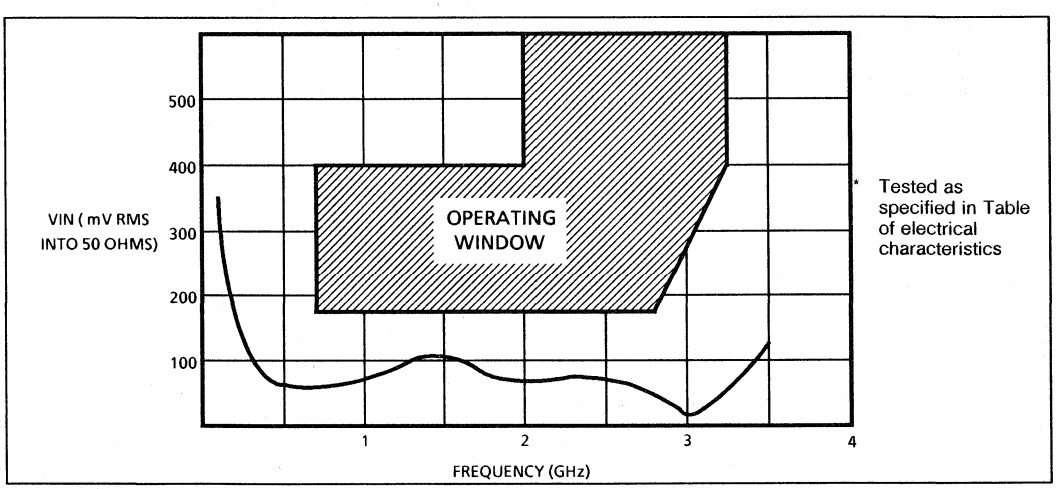


Fig.3 Typical input sensitivity

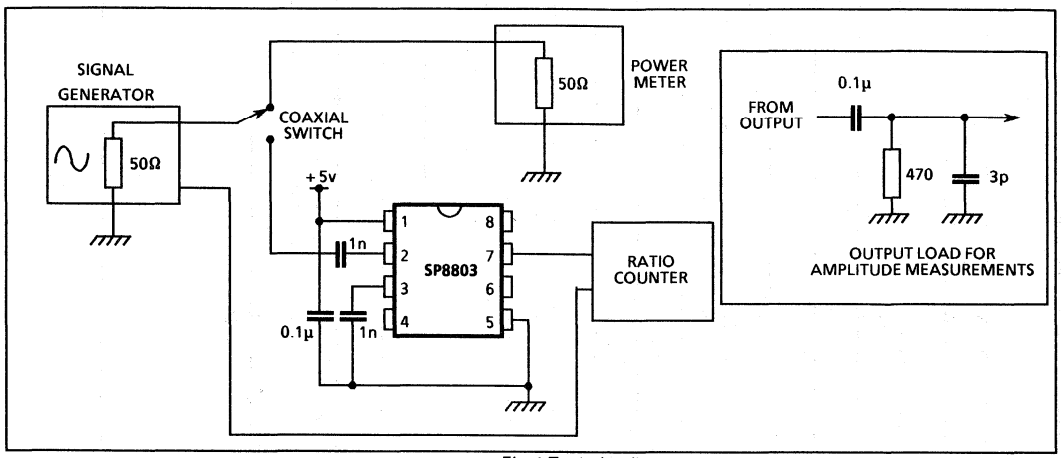


Fig.4 Test circuit

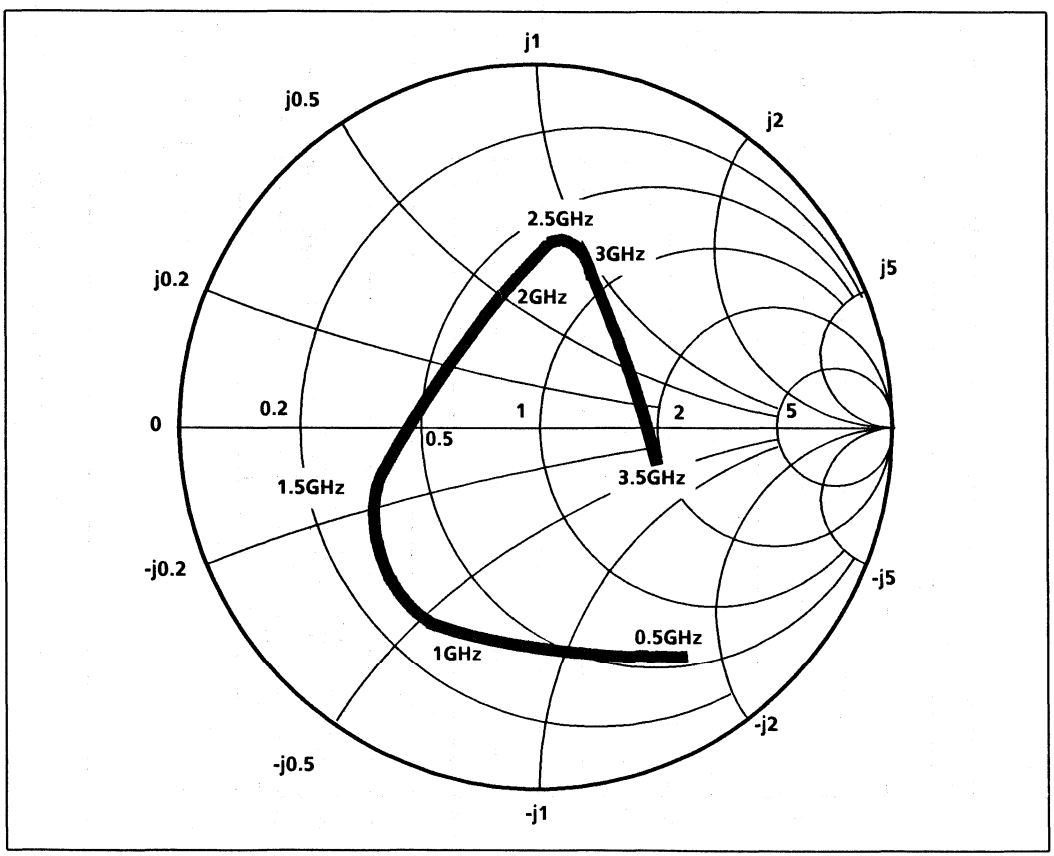


Fig. 5 Typical input impedance

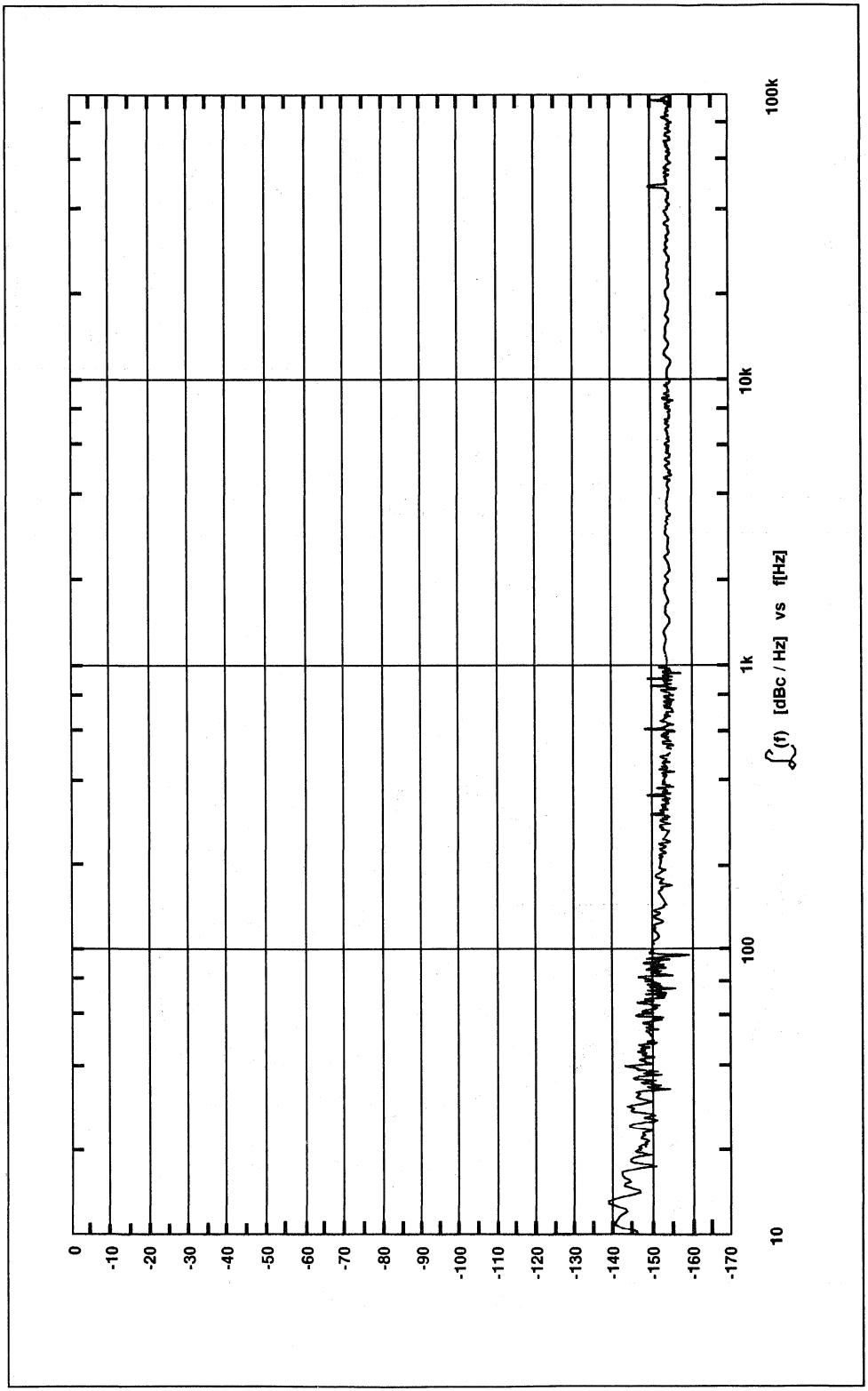


Fig. 6 Typical phase noise of SP8803 at 1GHz carrier

SP8804

3.3GHz ÷4 FIXED MODULUS DIVIDER

(Supersedes May 1991 Professional Products I.C. Handbook)

The SP8804 is one of a range of very high speed low power prescalers for professional and military applications. The device features a complementary output stage with on chip current source for the emitter follower outputs.

FEATURES

- Very High Speed Operation 3.3GHz
- Silicon Technology for low Phase Noise (Typically better than –140dBc/Hz at 10kHz)
- Specified Over the Full Military Temperature Range
- Low Power Dissipation 370mW (typ)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range

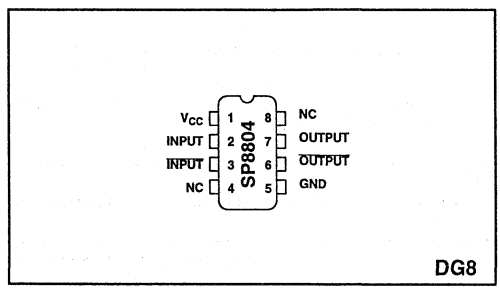


Fig. 1 Pin connections top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock Input voltage	2.5V p–p
Storage temperature Range	–65°C to +150°C
Junction temperature	+175°C

THERMAL CHARACTERISTICS

θja = 150°C/W

ORDERING INFORMATION

SP8804/A/DG Military temperature range
SP8804/AC/DG Military (MIL STD 883C) class B compliant. (Contact GPS for DATA Sheet)

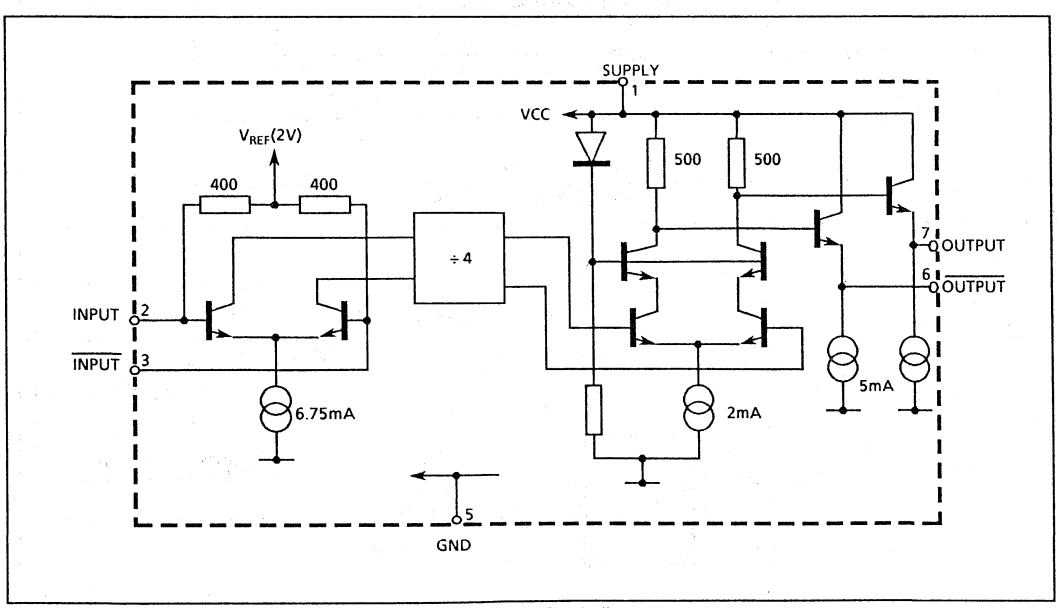


Fig.2 SP8804 Block diagram

ELECTRICAL CHARACTERISTICS

Guaranteed over the temperature range T_{amb} -55°C to +125°C (see note) and supply voltage range 4.75V to 5.25V
Tested at T_{amb} = -55°C and +105°C, V_{CC} = 4.75V and 5.25V.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	1		74	90	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave.
0.65GHz to 2.8GHz				175	mV	measured in 50 ohm system.
3.3GHz				400	mV	see Figs.3&4
Input impedance (series equivalvent)	2,3		50		Ω	
			2		pF	
Output voltage with fin = 1000MHz	6,7	0.8	1		Vp-p	V_{CC} = 5V
Output voltage with fin = 3GHz	6,7		0.25		Vp-p	V_{CC} = 5V Load as Fig. 4

NOTE
Devices must be used with a suitable heatsink to maintain chip temperature below 175°C when operating at T_{AMB} >105°C

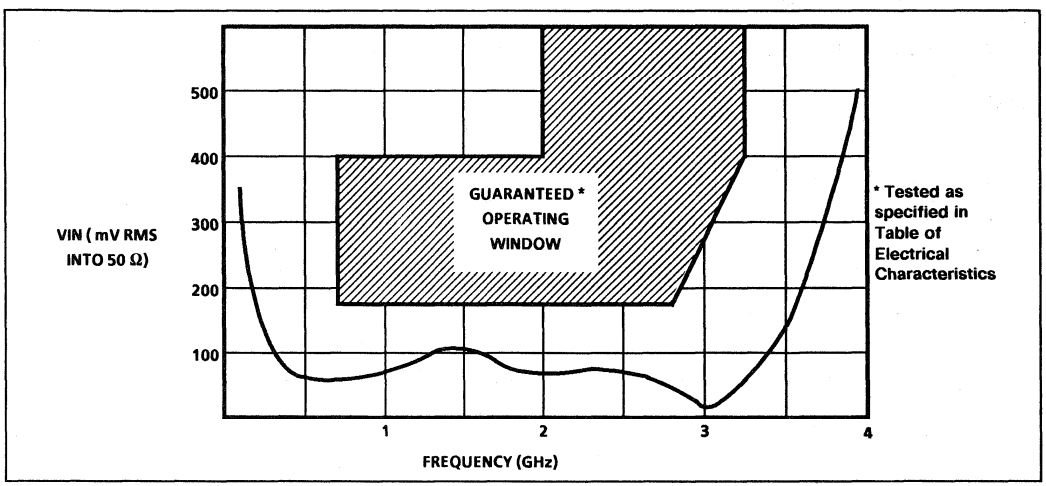


Fig. 3 typical input sensitivity

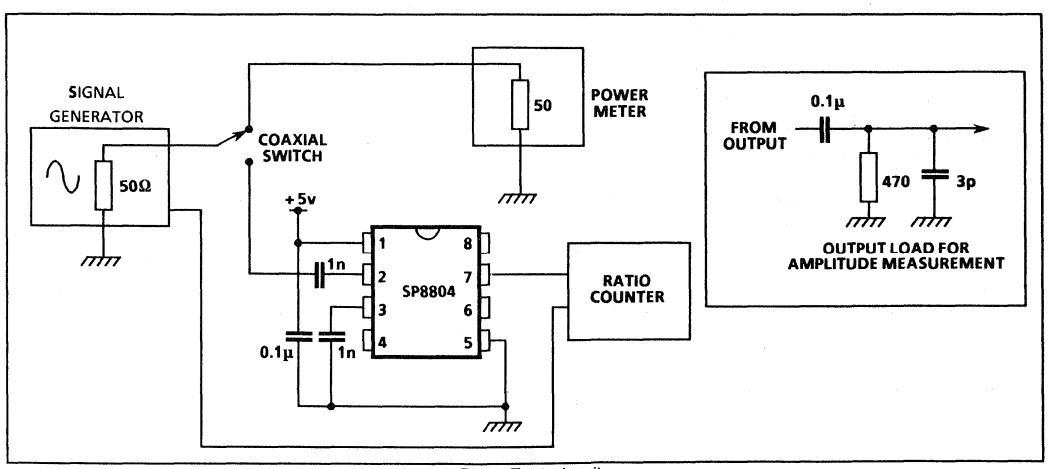


Fig. 4 Test circuit

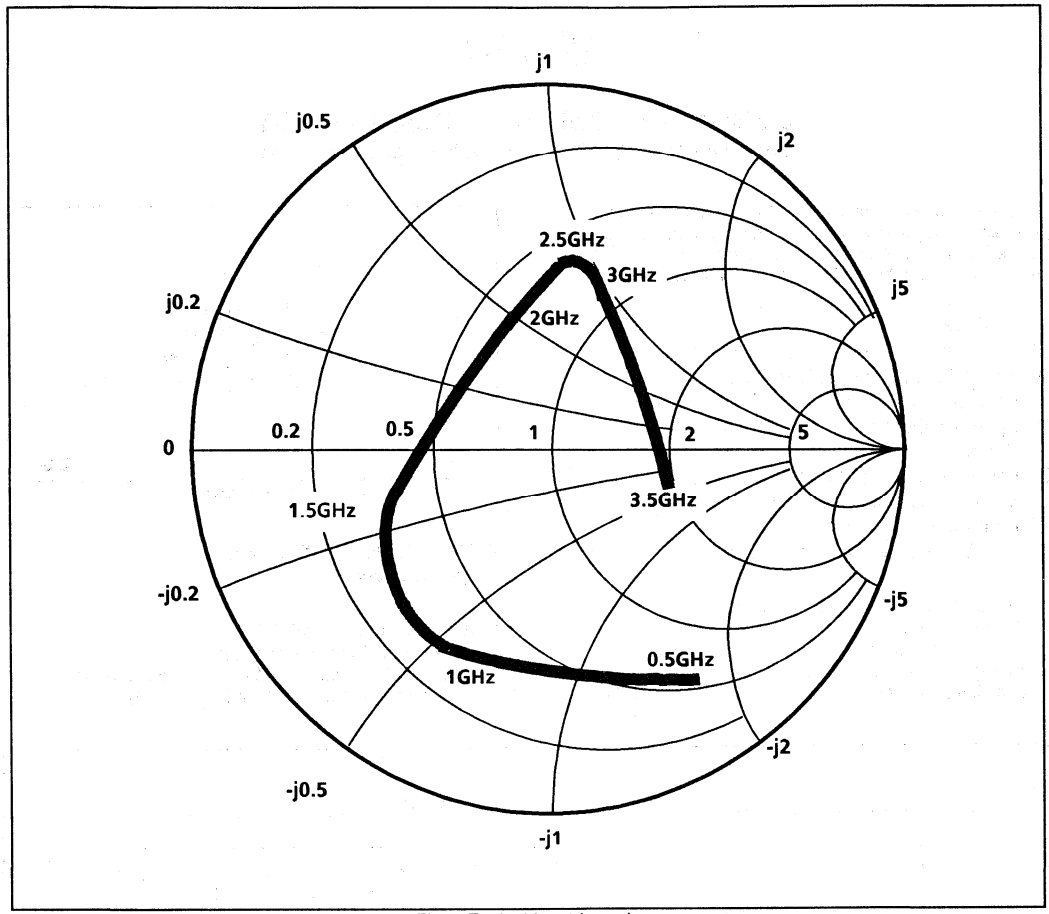


Fig. 5 Typical input impedance

SP8808

3.3GHz ÷ 8 FIXED MODULUS DIVIDER

(Supersedes May 1991 Professional Products I.C. Handbook)

The SP8808 is one of a range of very high speed low power prescalers for professional and military applications. The device features a complementary output stage with on chip current source for the emitter follower outputs.

FEATURES

- Very High Speed Operation 3.3GHz
- Silicon Technology for low Phase Noise (Typically better than –140dBc/Hz at 10kHz)
- Specified Over the Full Military Temperature Range
- Low Power Dissipation 345mW (typ)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock Input voltage	2.5V p–p
Storage temperature Range	–65°C to +150°C
Junction temperature	+175°C

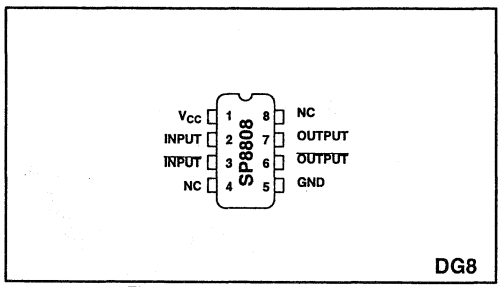


Fig. 1 Pin connections top view

THERMAL CHARACTERISTICS

θja = 150°C/W

ORDERING INFORMATION

SP8808/A/DG Military temperature range
SP8808/AC/DG Military (MIL STD 883C) class B compliant. (Contact GPS for DATA Sheet)

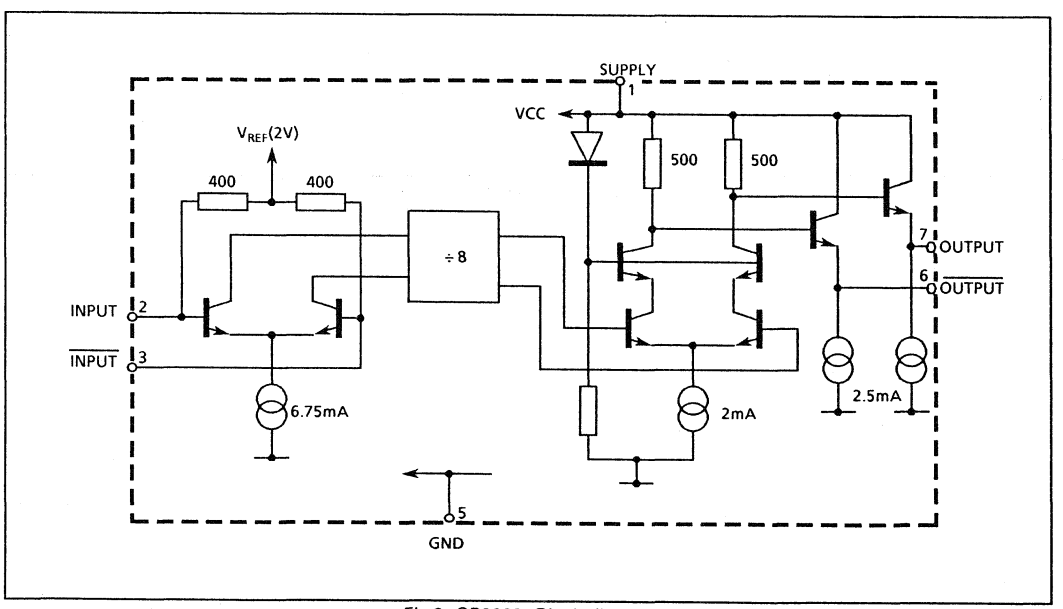


Fig.2 SP8808 Block diagram

ELECTRICAL CHARACTERISTICS

Guaranteed over the temperature range T_{amb} -55°C to +125°C (see note) and supply voltage range 4.75V to 5.25V
Tested at T_{amb} = +110°C and +125°C, V_{CC} = 4.75V and 5.25V.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	1		69	85	mA	V_{CC} = 5V
Input sensitivity	2,3					RMS sinewave.
0.65GHz to 2.8GHz				175	mV	measured in 50 ohm system.
3.3GHz				400	mV	see Figs.3&4
Input impedance (series equivalvent)	2,3		50		Ω	
			2		pF	
Output voltage with fin = 1000MHz	6,7	0.8	1		Vp-p	V_{CC} = 5V
Output voltage with fin = 3GHz	6,7		0.4		Vp-p	V_{CC} = 5V Load as Fig 4

NOTE
Devices must be used with a suitable heatsink to maintain chip temperature below 175°C when operating at T_{AMB} >110°C

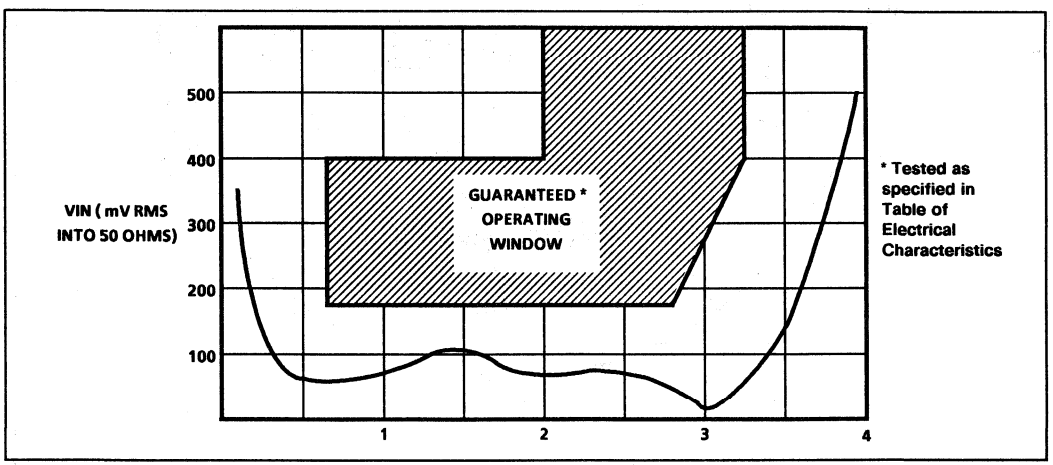


Fig. 3 typical input sensitivity

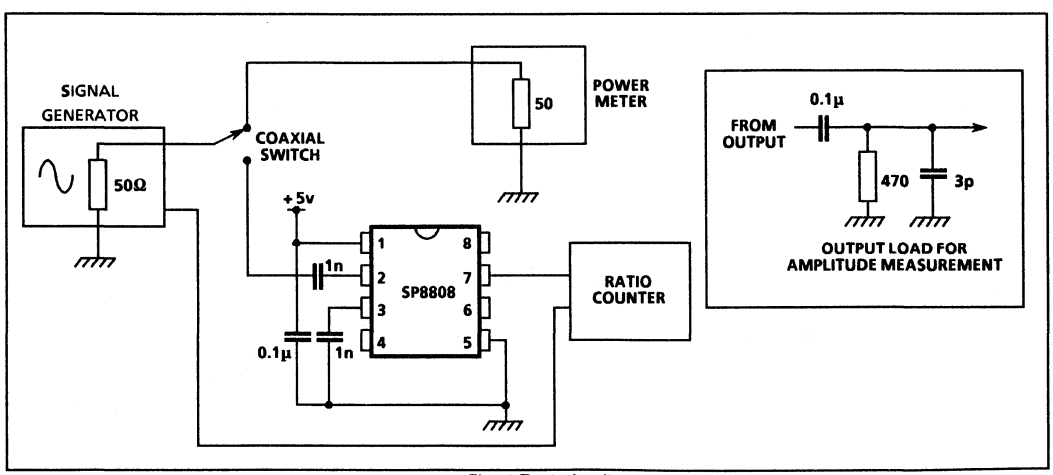


Fig. 4 Test circuit

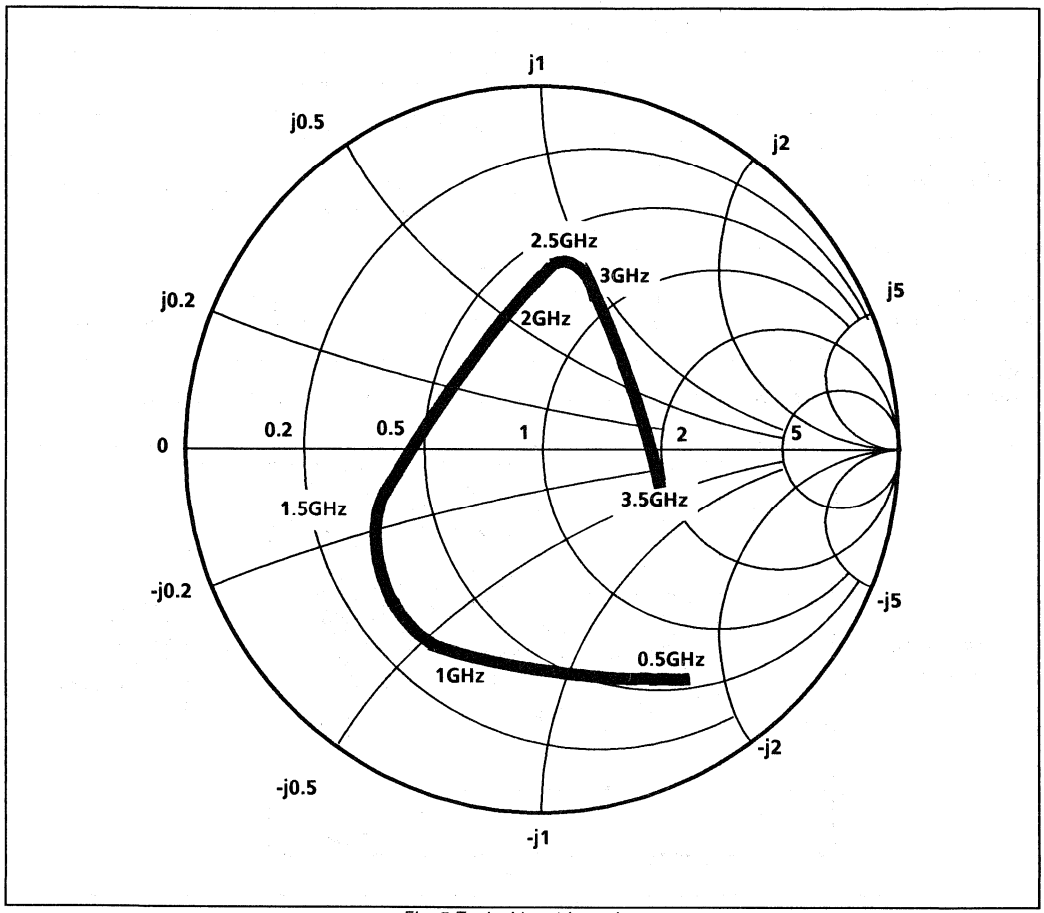


Fig. 5 Typical input impedance

SP8830

1·5GHz÷10 PRESCALER

The SP8830 is one of a range of very high speed low power prescalers for professional and military applications. The device features a complementary output stage with on chip current sources for the emitter follower outputs.

FEATURES

- Very High Speed Operation 1·5GHz
- Silicon Technology for Low Phase Noise (Typically Better Than −140dBc / Hz at 10kHz)
- Very Low Power Dissipation: 150mW (Typ.)
- Single 5V Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range
- Temperature Range: −55°C to +125°C (A Grade)
  −40°C to +85°C (B Grade)

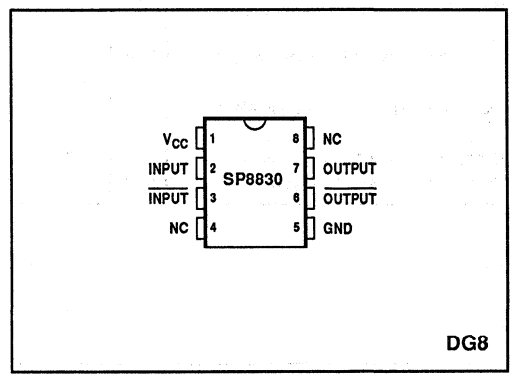


Fig. 1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	6·5V
Clock input voltage	2·5V p-p
Storage temperature range	−65°C to +150°C
Junction temperature	+175°C

ORDERING INFORMATION

SP8830 A DG
SP8830 B DG
SP8830 AC DG

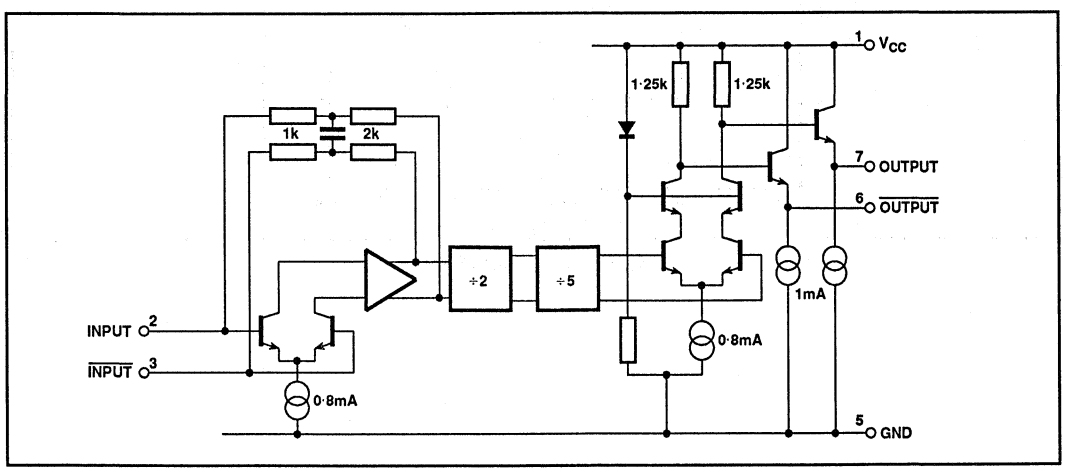


Fig. 2 SP8830 block diagram

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range
Supply voltage, V_{CC} = 4·75V to 5·25V
Temperature, T_{AMB} = −55°C to +125°C (A Grade), −40°C to +85°C (B Grade)

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current, I_{CC}	1		40	50	mA	
Input sensitivity, 100MHz to 1500MHz	2, 3			100	mV	RMS sinewave, measured in 50Ω system. See Figs 3 and 4.
Input impedance (series equivalent)	2, 3		50 2		Ω pF	See Fig. 5
Output voltage with f_{IN} = 100MHz	6, 7	0·7	1		V p-p	
Output voltage with f_{IN} = 1500MHz	6, 7		0·4		V p-p	

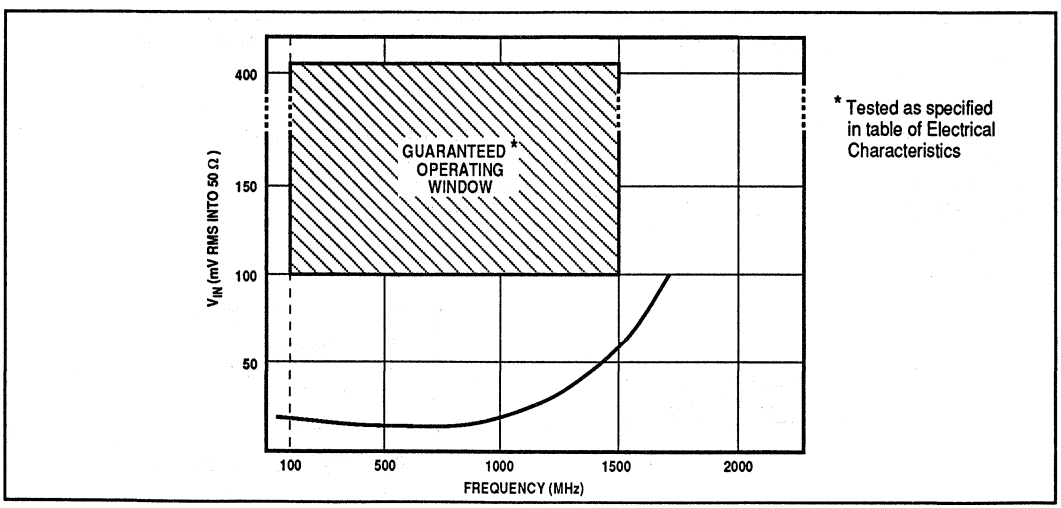


Fig. 3 Typical input sensitivity

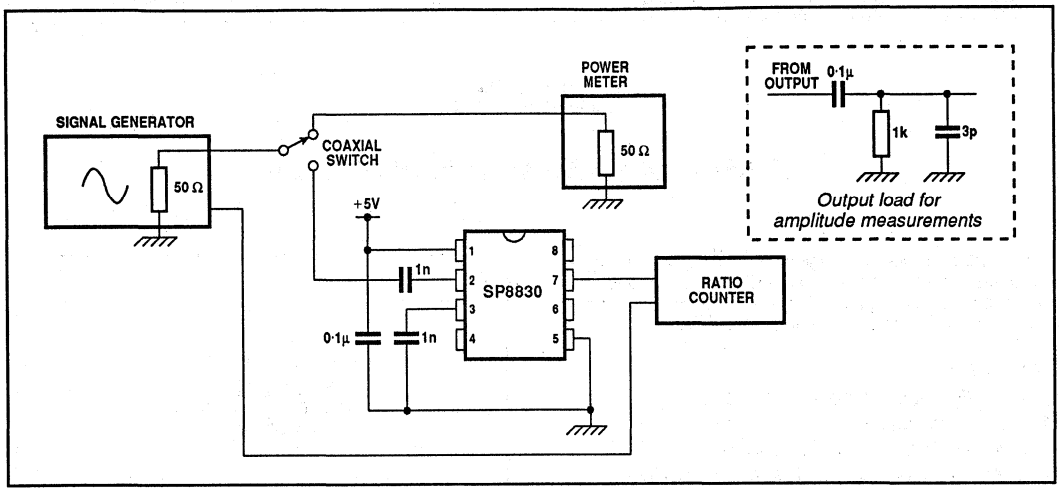


Fig. 4 Test circuit

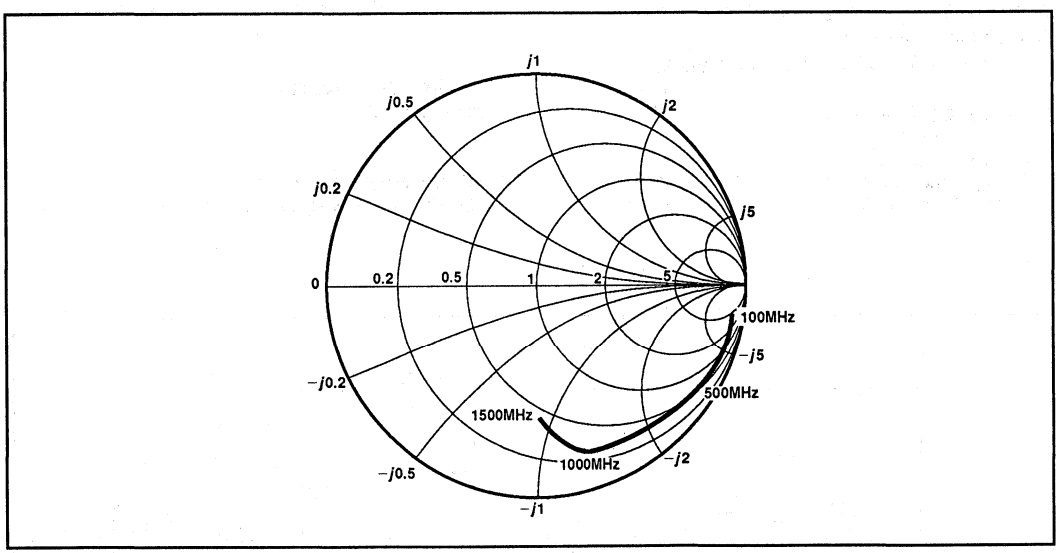


Fig. 5 Typical input impedance, normalised to 50Ω

SP8831

3.5GHz ÷16 FIXED MODULUS DIVIDER

The SP8831 is one of a range of very high speed low power prescalers for professional and military applications. The device features a complementary output stage with on chip current source for the emitter follower outputs.

FEATURES

- Very High Speed Operation 3.5GHz
- Silicon Technology for low Phase Noise (Typically better than –150dBc/Hz at 10kHz)
- Specified Over the Full Military Temperature Range
- Low Power Dissipation 375mW (typ)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock Input voltage	2.5V p–p
Storage temperature Range	–65°C to +150°C
Junction temperature	+175°C

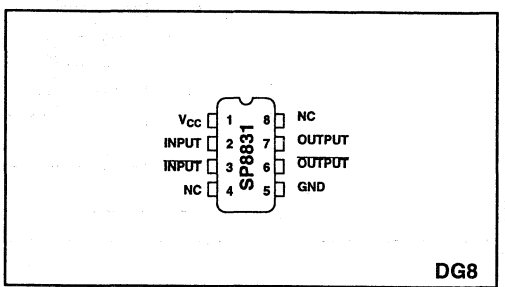


Fig. 1 Pin connections top view

THERMAL CHARACTERISTICS

θja = 150°C/W

ORDERING INFORMATION

SP8831/B/DG Military temperature range

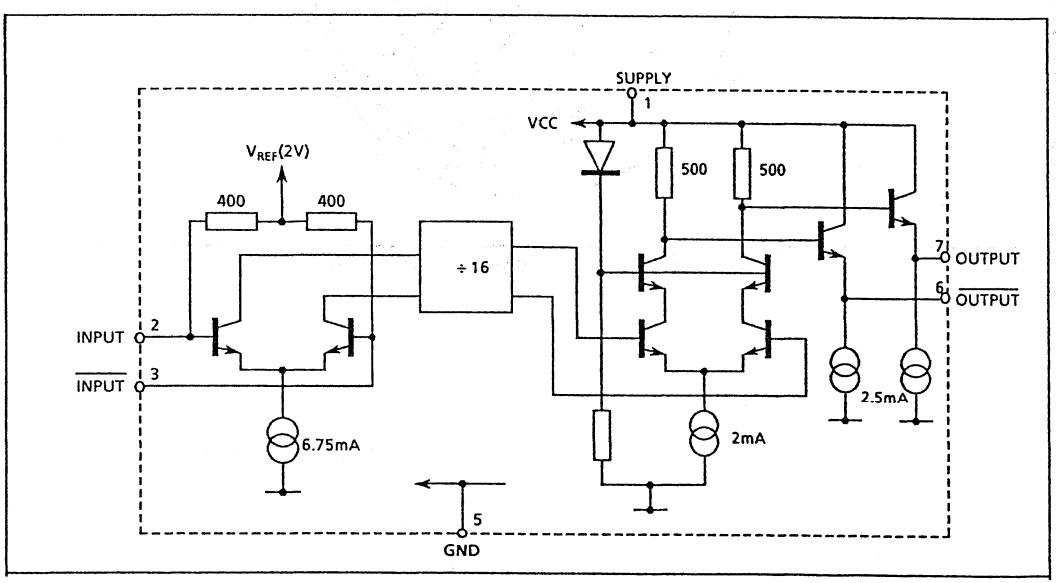


Fig.2 SP8831 Block diagram

ELECTRICAL CHARACTERISTICS

Guaranteed over the temperature range T_{amb} -40°C to +85°C and supply voltage range VCC = 4.75V to 5.25V
Tested at T_{amb} = -40°C and +85°C, V_{CC} = 4.75V and 5.25V.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	1		75	88	mA	V_{CC} = 5V
Input sensitivity 0.65GHz to 3.0GHz 3.5GHz	2, 3			 175 500	 mV mV	RMS sinewave measured in 50Ω system. see Figs. 3 & 4
Input impedance (series equivalent)	2, 3		50 2		Ω pF	
Output Voltage with f_{in} = 650MHz	6, 7	.780	1.04	1.30	Vp-p	V_{CC} = 5V
Output Voltage with f_{in} = 3GHz	6, 7		0.95		Vp-p	V_{CC} = 5V load as Fig. 4

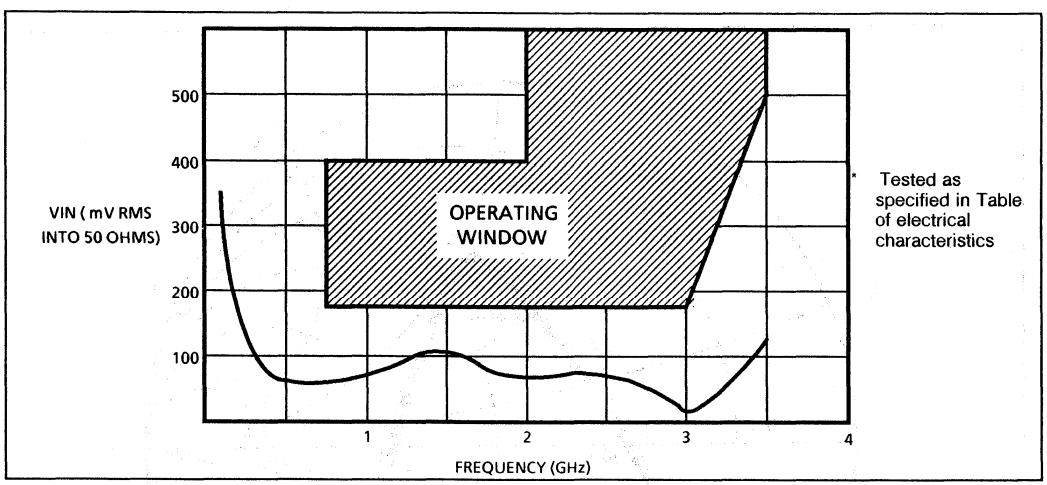


Fig.3 Typical input sensitivity

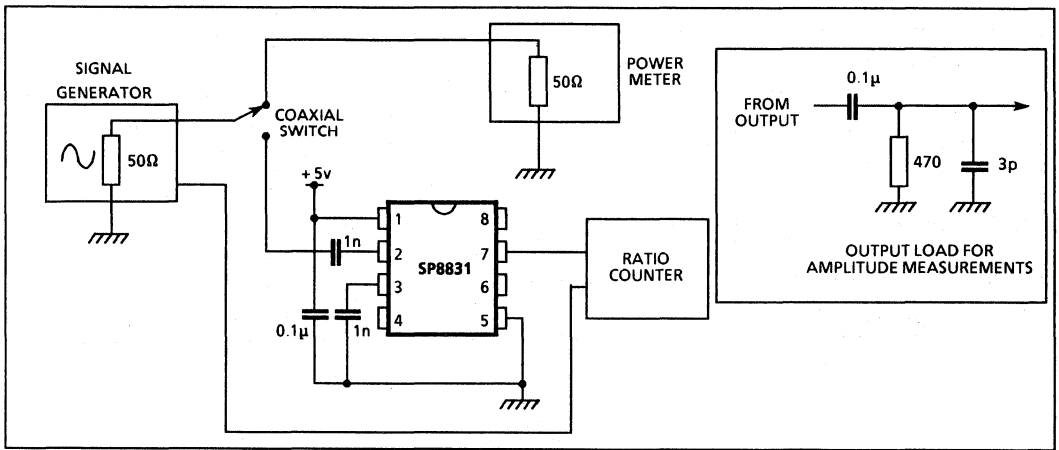


Fig.4 Test circuit

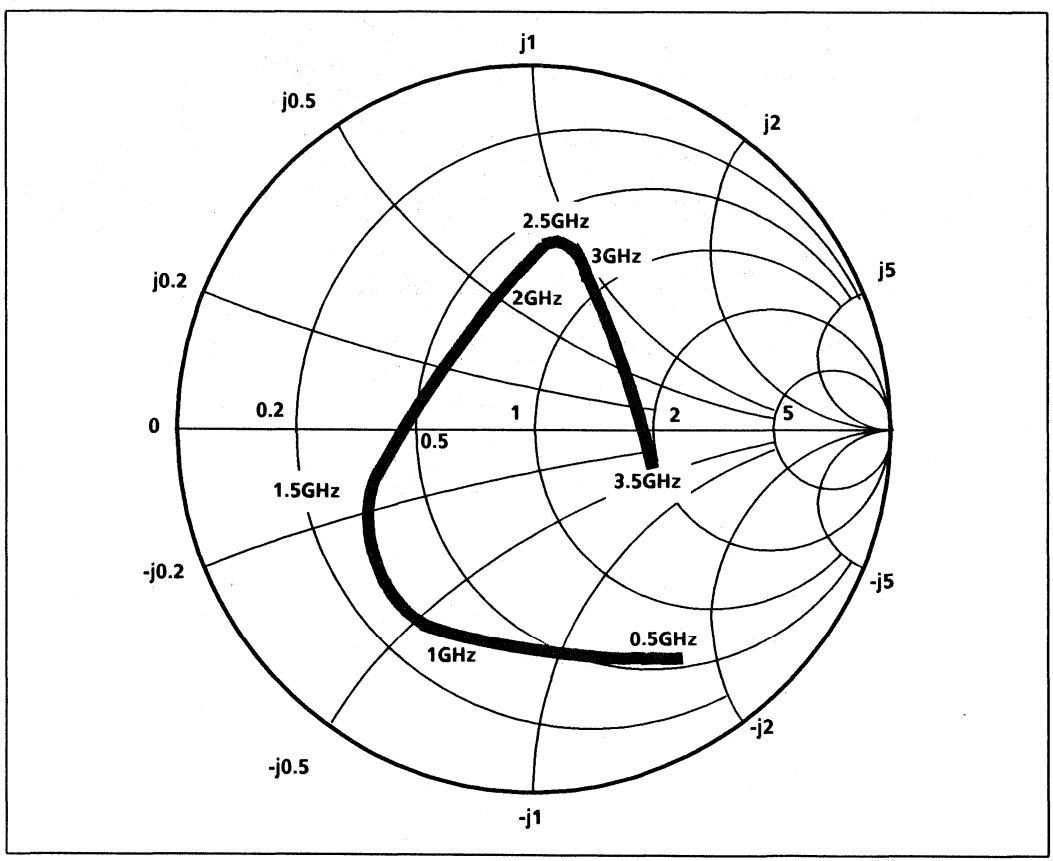


Fig. 5 Typical input impedance

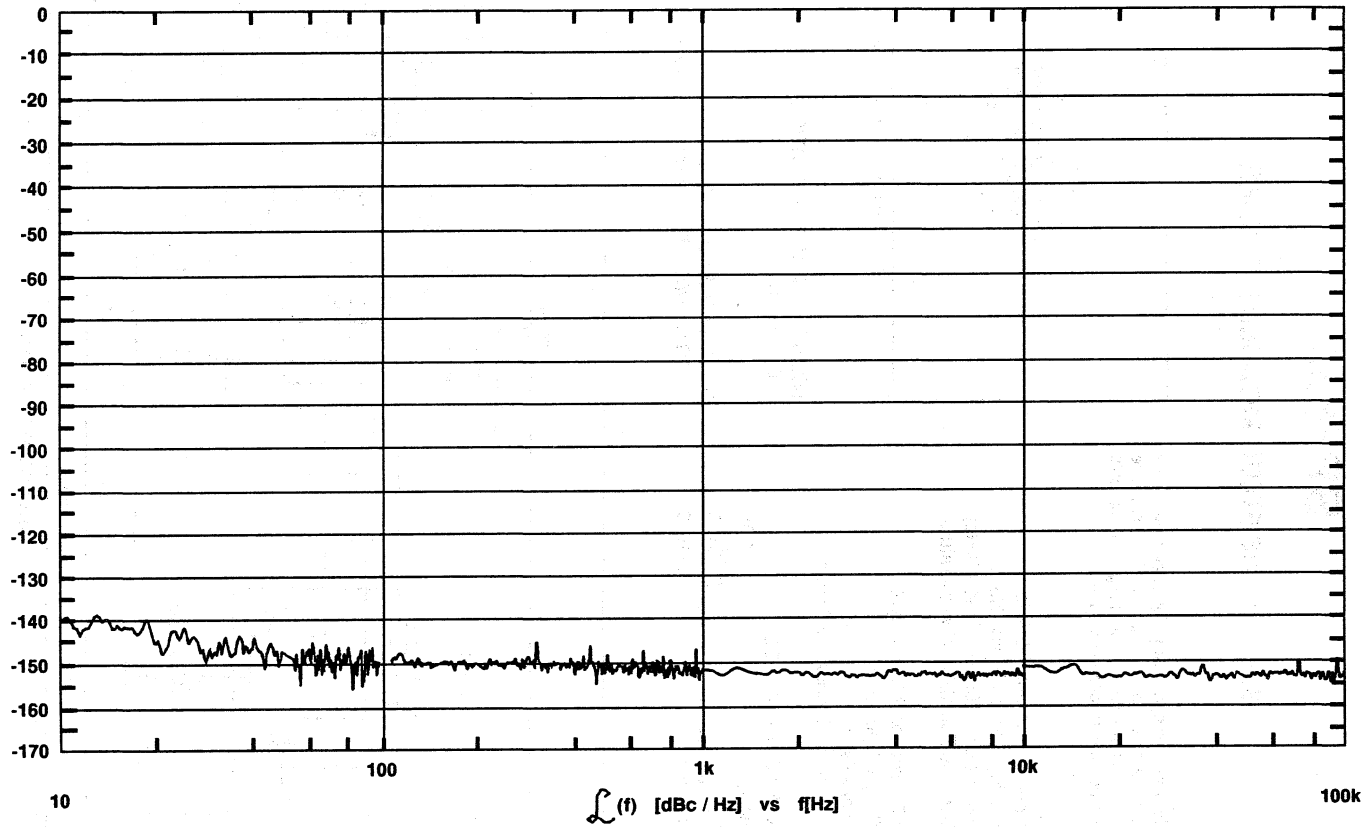


Fig. 6 Typical phase noise of SP8831 at 1GHz carrier

SP8833

3.5GHz ÷16 FIXED MODULUS DIVIDER

The SP8831 is one of a range of very high speed low power prescalers for professional and military applications. The device features a complementary output stage with on chip current source for the emitter follower outputs.

FEATURES

- Very High Speed Operation 3.5GHz
- Silicon Technology for low Phase Noise (Typically better than –150dBc/Hz at 10kHz)
- Specified Over the Full Military Temperature Range
- Low Power Dissipation 375mW (typ)
- 5V Single Supply Operation
- High Input Sensitivity
- Very Wide Operating Frequency Range

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC}	6.5V
Clock Input voltage	2.5V p–p
Storage temperature Range	–65°C to +150°C
Junction temperature	+175°C

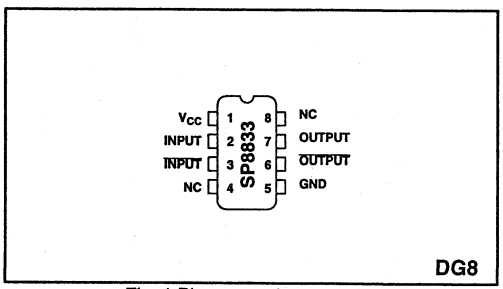


Fig. 1 Pin connections top view

THERMAL CHARACTERISTICS

θja = 150°C/W

ORDERING INFORMATION

SP8833/B/DG Military temperature range

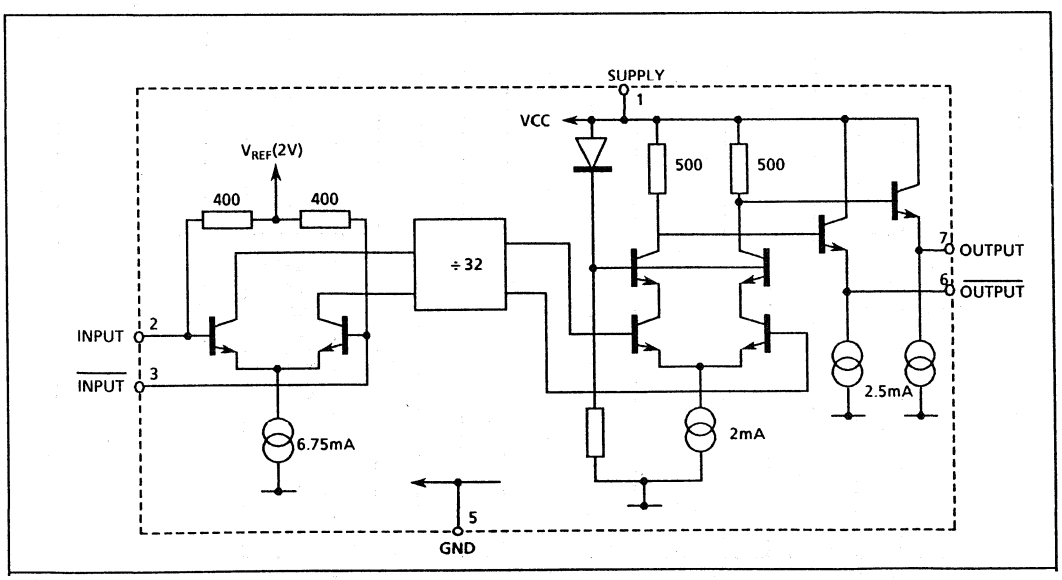


Fig.2 SP8833 Block diagram

ELECTRICAL CHARACTERISTICS

Guaranteed over the temperature range T_{amb} -40°C to +85°C and supply voltage range VCC = 4.75V to 5.25V
Tested at T_{amb} = -40°C and +85°C, V_{CC} = 4.75V and 5.25V.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply current	1		78	90	mA	V_{CC} = 5V
Input sensitivity 0.65GHz to 3.0GHz 3.5GHz	2, 3			 175 500	 mV mV	RMS sinewave measured in 50Ω system. see Figs. 3 & 4
Input impedance (series equivalent)	2, 3		50 2		Ω pF	
Output Voltage with f_{in} = 650MHz	6, 7	.780	1.04	1.30	Vp-p	V_{CC} = 5V
Output Voltage with f_{in} = 3GHz	6, 7		0.95		Vp-p	V_{CC} = 5V load as Fig. 4

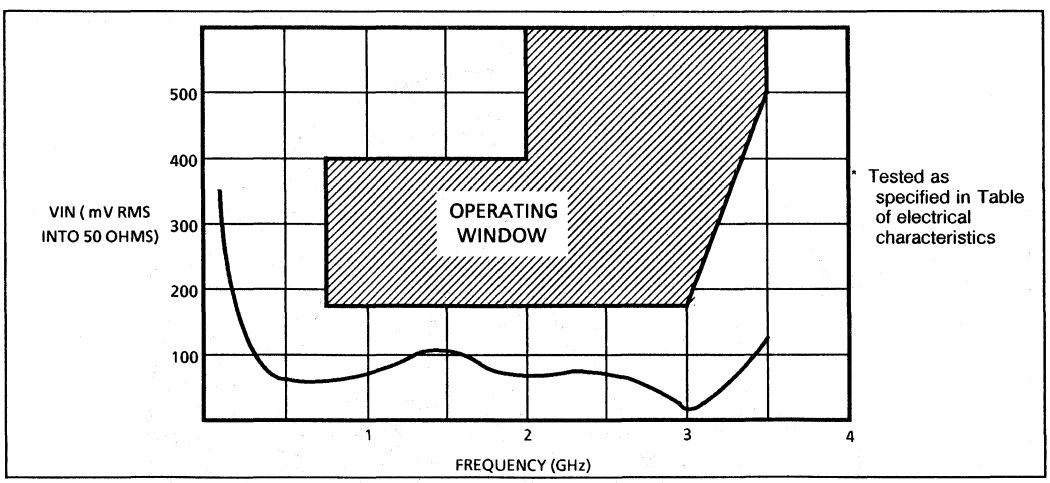


Fig.3 Typical input sensitivity

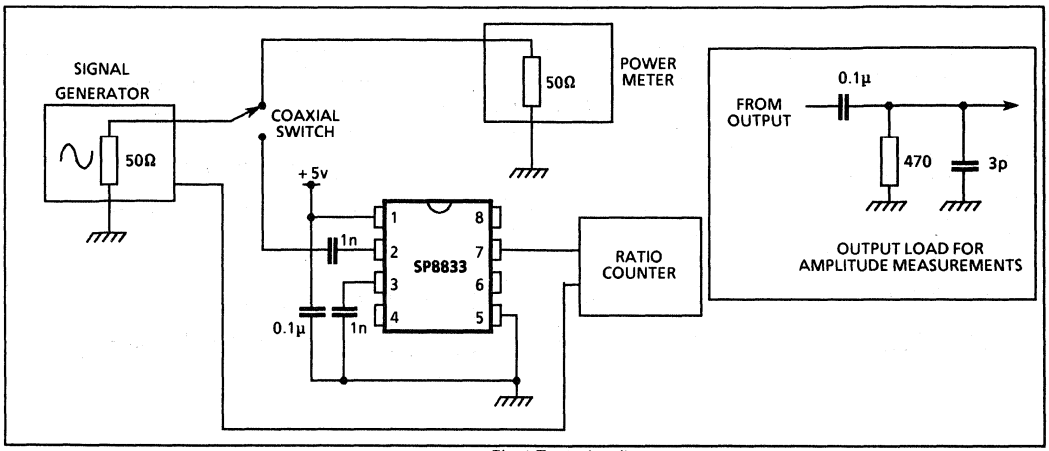


Fig.4 Test circuit

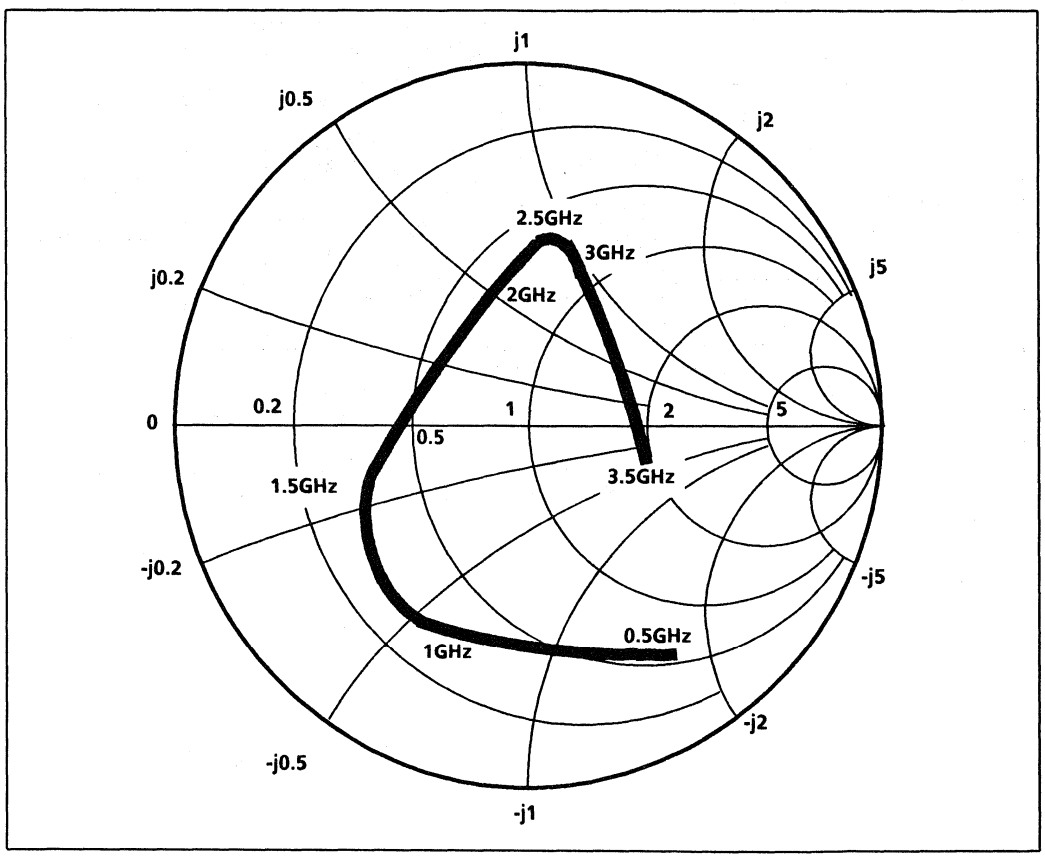


Fig. 5 Typical input impedance

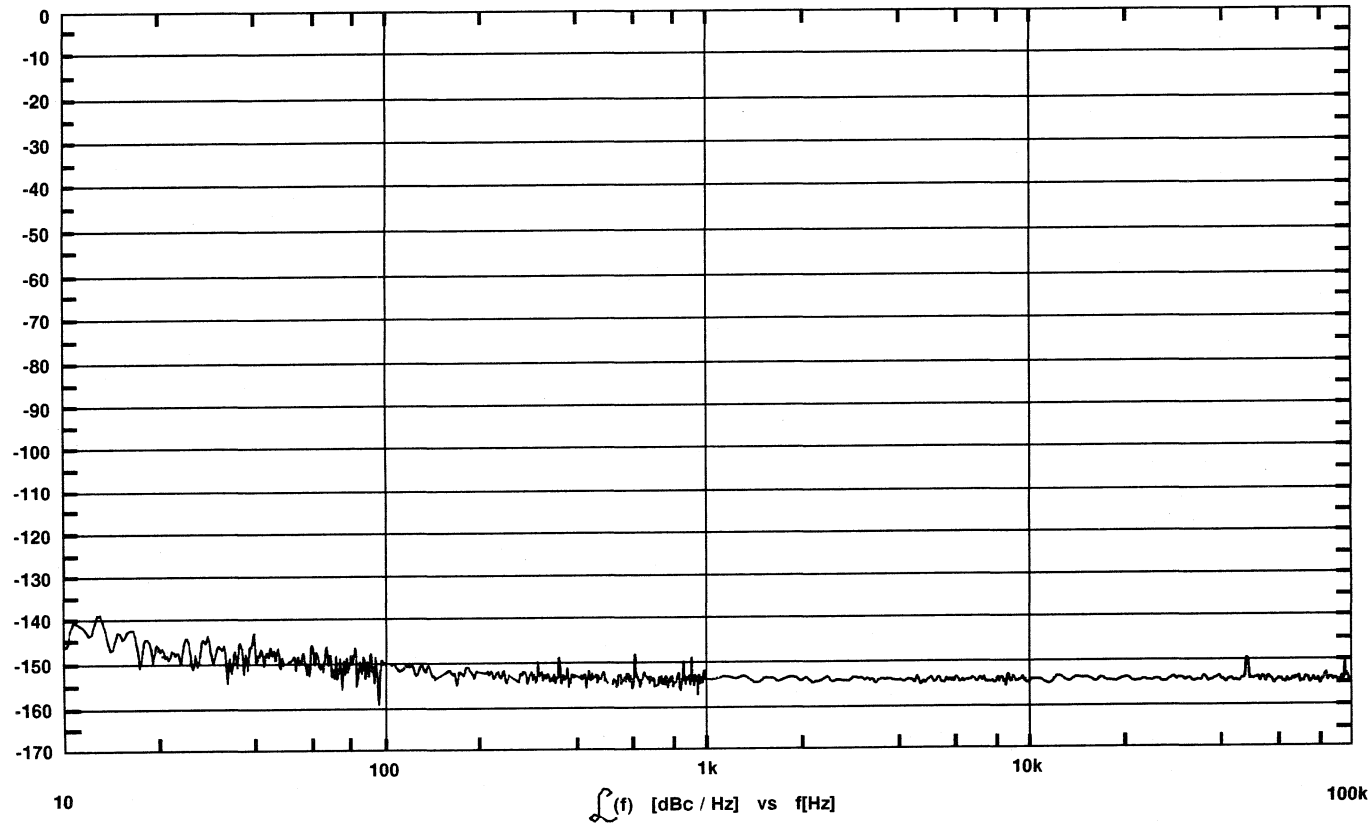


Fig. 6 Typical phase noise of SP8833 at 1GHz carrier

Section 4
Application Notes

GEC PLESSEY
SEMICONDUCTORS

The care and feeding of High Speed Dividers

AN178

Circuit design and layout for high speed dividers operating at frequencies up to 5GHz owe much more to analog RF design techniques than normal digital ones and the limitations on flexibility and component choice inherent in UHF RF design are of paramount importance in successful designs.

PRACTICAL DESIGN CONSIDERATIONS

High speed divider applications require the printed circuit boards to be mechanically designed with two considerations in mind:

(1) Electrical performance
(2) Mechanical and thermal performance.

These two considerations are inter-related; for example, the use of 1/16 inch thick fibreglass PC board may be desirable mechanically, but a 50Ω stripline on this thickness of board is about 5/32 inch wide, and is thus too wide to pass between the pins of an IC.

Most of the heat conducted from a dual-in-line IC package is removed from the bottom of the package. Less than 10 % is conducted out by the leads, and because of the cavity between the chip and lid, relatively little through the top of the package.

For this reason, the use of a double-layer PC board layout is recommended, with a ground plane top surface. Where 1/32 inch thick material is used, a top surface ground plane will add substantially to the heat dissipation capabilities of the board

For use at very high frequencies, consideration must be given to the type of component used. Carbon composition resistors are more resistive at high frequencies than either carbon or metal film types, and are available in very small sizes. Bypass capacitors need to be chosen carefully if they are to act as low impedances, as series inductance leads to an increasing impedance with frequency above the series resonant frequency of the device. As a guide, a 1000pF disc ceramic capacitor with 1/4 inch leads will be self resonant at about 75MHz, and will appear as an inductive impedance of about 22Ω at 800MHz. The use of chip capacitors is recommended above 500MHz, although leaded monolithic ceramic capacitors with suitably short leads are often acceptable.

The use of a ground plane for RF decoupling purposes is often recommended, and can be helpful. However, the danger is that the ground current paths in the plane are not defined very well, and because of this lack of definition, the ground plane can cause unsatisfactory operation. Probably the best method is to return all the bypass capacitors to a single point (as in Fig 1) and return this point to the ground plane.

Also note that in Fig.1 the output load resistors have their grounded ends connected together and a common return used Because the currents in the resistors are in antiphase, cancellation of the inductive effects taken place, and the path followed by the relatively large output currents is controlled. Defining the ground current path is more important in applications like frequency synthesis, where a relatively large part of the system may be on one PCB.

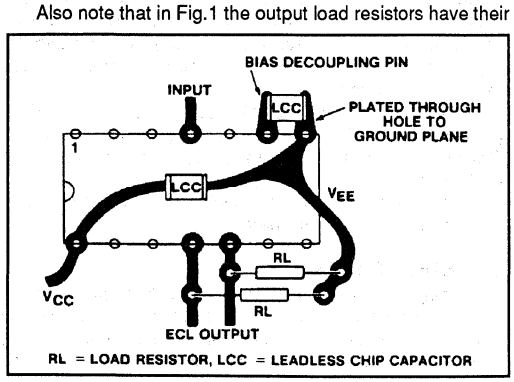


Fig.1 single point grounding

It is well known that the effect of mismatching a transmission line is to cause variations in the voltage along the line. Standard practice at GEC Plessey Semiconductors has been to use a 5:1 attenuator manufactured from 'microdot' resistors as an attenuator feeding a 50Ω sampling oscilloscope or a power meter. Although a high VSWR will exist on the line from the generator to the test fixture, the theory is that the line from the power meter to the attenuator will be a matched line, and so the power measured is 14dB lower than the power at the device input pin. This method has been proved very successful, even if simple, and offers some advantages over the use of hybrids or directional couplers.

The use of a matched 50Ω system can help, and using microstrip techniques, a track with a defined impedance is reasonably practical. The impedance of a microstrip line is given by:

$$Zo = 377\ (L/w)\ (1/\varepsilon r)$$

Where L = dielectric thickness, w = width of track and εr is the relative permeability of the board material.

Some correction factors have to be applied, and typically, on 1/16 inch glass fibre epoxy board, the following sizes provide a guide to track width

100Ω- 1mm
76Ω - 2mm
80Ω - 4mm

These impedances rely on the ground plane on the obverse of the board being complete, and where boards are wave soldered, it may be necessary to make arrangements to prevent blistering.

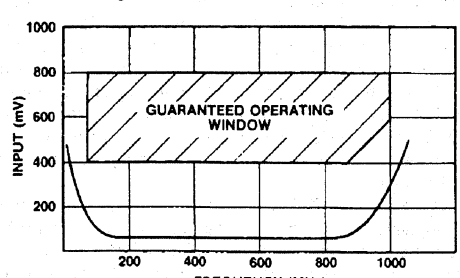


Fig.2 Example of input sensitivity curves

The input level of a divider should be maintained within the guaranteed operating window shown on its data sheet (Fig.2). Excessive input can vary in its effects, from causing permanent damage to miscounting, especially when cold. Running the device at too low a level can cause problems, even though the level is within the 'typical' performance line of the device An ECL output signal on pin 6 of the device in Fig.3 can couple 60mV of signal to the input shown on Fig.2 at 500MHz. Such

a level of coupling can lead to divider jitter if the input signal is low, and it becomes very necessary to keep the inputs and outputs well separated at the higher frequencies. This includes ECL lines to modulus control pins on two modulus dividers.

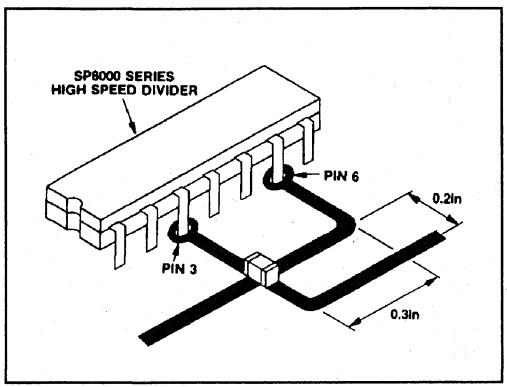


Fig.3 Coupling between parallel tracks

Most dividers are edge triggered, and although they are specified over a frequency range with sine wave input, they will operate to lower frequencies provided a suitably high slew rate is provided on the input signal. This is generally of the order of 100 to 200 volts/microsecond. This should be achieved by shaping of the input signal, for example by limiting rather than by overdriving the device.
The outputs of devices may be of the following forms:

(1) ECL
(2) Open collector TTL
(3) TTL
(4) CMOS

Of these, the ECL output is well defined; some devices require external load resistors and the data sheet should be consulted. Where these external resistors are required, suitable interconnection techniques should be used between them and the device; the resistors should be carefully chosen for their non-inductive properties when output frequencies are very high. Where an ECL output divider drives another divider it is best to AC couple, since few dividers are strictly ECL compatible on their inputs.

Open collector TTL outputs are relatively slow. Although the negative edge is limited in speed by the turn-on time of the output transistor, the rising edge is limited by the external load resistor and capacitance to ground. In practice this means that short narrow tracks are required to the following device, and a minimum 'fan-in' load provided. In addition, open collector TTL should not be used above about 10MHz output frequency.

True TTL outputs are not so limited, because of the active pull-up. Nevertheless, the use of such outputs at frequencies above about 25-30MHz is not recommended, especially into capactive loads. Loads of more than 30pF should not be d riven faster than about 15MHz. Note that the current drawn by true TTL outputs increases with increasing load capacitance.

CMOS outputs are, on the face of it, TTL-compatible. However, investigation will show that the outputs are not guaranteed to meet TTL levels at TTL currents and it is not recommended that CMOS output devices be used to directly drive TTL. Where an interface of this sort is required, an active transistor interface should be used.

Fig.4 shows a circuit for an ECL-TTL interface, using a line receiver. Simple circuits using one or two transistors cannot be guaranteed to work over all the tolerances of ECL output voltages and temperature ranges.

Interfacing to dividers is not difficult if a few simple rules are obeyed. These are:

(1) Observe the input requirements - guaranteed input operating area, and slew rate.
(2) Do not use open collector outputs above 10MHz.
(3) Do not use CMOS outputs to drive TTL.
(4) Use a sensible layout with good components, and sensible values - 0.1 microfarad ceramic capacitors are NOT bypasses at 1.5GHz.

Treating dividers as RF linear devices is probably the best way to ensure successful applications at high frequencies. There is no magic in HF design, only intelligent layout and sensible component choice.

Impedance Matching

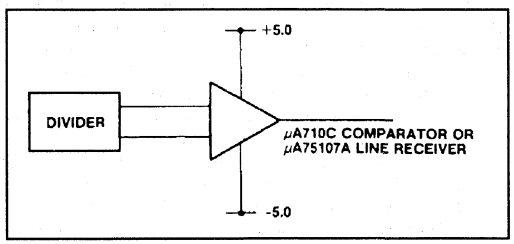


Fig.4 ECL/TTL interface

The use of microstrip techniques has been mentioned already. However, in itself this will not produce a matched network and various possibilities exist to improve the matching at the input of a device. These include Tchebycheff impedance transforming networks, narrow band 'L' matching networks, and at high enough frequencies, the use of transmission lines. Wideband matching is often difficult, and attempts should be made to use networks that have the lowest possible working Q. This is for two reasons: firstly a high Q network will not only be narrow band, but will have the capability of increasing the losses, and secondly, a low Q network is generally more tolerant of component variations.

The greater losses in high Q circuits occur because of the greater circulating current: the loss power is I^2R, so that if the Q is doubled with all else constant, the power loss is increased by 4 times.

The easiest method of determining matching components is by means of the Smith Chart.

THE SMITH CHART

The input impedance of SP8000-series high speed dividers varies as a function of frequency and is therefore specified on the datasheets by means of Smith Charts. The following information is included in this handbook as a guide to their interpretation and use.

Construction of the chart

The chart is constructed with two sets of circles, one set comprising circles of CONSTANT RESISTANCE (Fig. 5) and the other circles of CONSTANT REACTANCE (Fig. 6). The values on these circles are normalised to the characteristic impedances of the system by dividing the actual value of resistance or reactance by the characteristic impedance e.g. in a 50Ω system, a resistance of 100Ω is normalised to a value of 2.0.

By combining Figs. 5 and 6 to form Fig. 7, a chart is produced in which any normalised impedance has a unique position on the chart, and the variation of this impedance with frequency or other parameters may be plotted.

A further series of circles may be plotted on the chart: these are circles of constant VSWR, and represent the degree of mismatch in a system. The VSWR is the ratio of the device impedance to the characteristic impedance, and is always expressed as a ratio greater than 1: thus a 25Ω device in a 50Ω system gives rise to a 2:1 VSWR. These circles of constant VSWR have been added in Fig. 7.

Any point can be represented on the Smith Chart: for example an impedance of 150-*j*75Ω can be represented by a normalised impedance (in a 50Ω system) of 3-*j*1.5 and this point is plotted in Fig. 7 as point A.

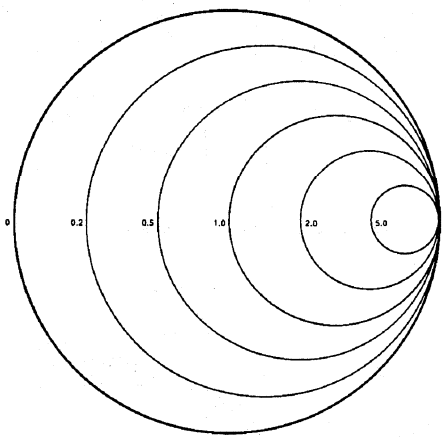


Fig.5 Constant resistance circles

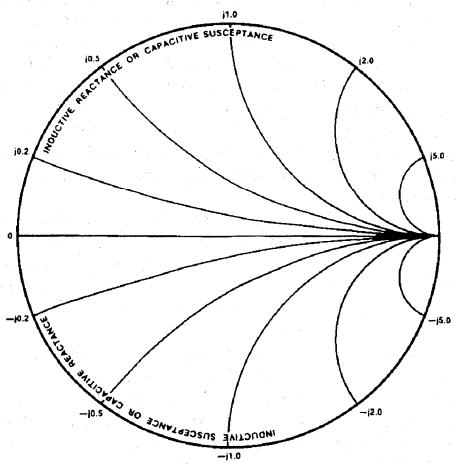


Fig.6 Constant reactance cirles

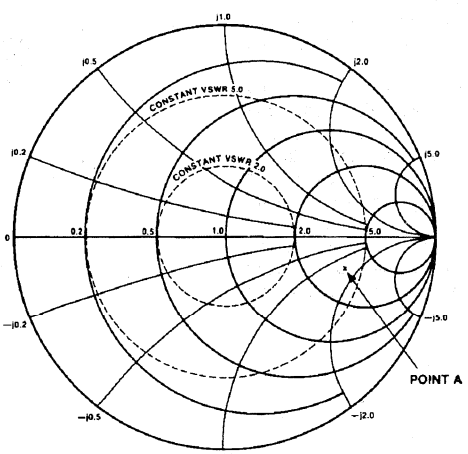


Fig.7 The complete chart

Network calculations

The main application for Smith Charts with integrated circuits is in the design of matching networks. Although these can be calculated by use of the series to parallel (and vice-versa) transforms, followed by the application of Kirchoff's Laws, the method can be laborious. Although the Smith Chart as a graphical method cannot necessarily compete in terms of overall accuracy, it is nevertheless more than adequate for the majority of problems, especially when the errors inherent in practical components are taken into account.

Any impedance can be represented at a fixed frequency by a shunt conductance and susceptance (impedances as series reactance and resistance in this context). By transferring a point on the Smith Chart to a point at the same diameter but 180° away, this transformation is automatically made (see Fig. 8) where A and B are the series and parallel equivalents.

It is often easier to change a series RC network to its equivalent parallel network for calculation purposes. This is because as a parallel network of admittances, a shunt admittance can be directly added, rather than the tortuous calculations necessary if the series form is used. Similar arguments apply to parallel networks, so in general it is best to deal with admittances for shunt components and reactances for series components.

Admittances and impedances can be easily added on the Smith Chart (see Fig. 9) Where a series inductance is to be added to an admittance (i.e parallel R and C), the admittance should be turned into a series impedance by the method outlined above and in Fig 8. The series inductance can then be added as in Fig. 9 (see also Fig. 10).

Point A is the starting admittance consisting of a shunt capacitance and resistance The equivalent capacitive impedance is shown at point B. The addition of a series inductor moves the impedance to point C. The value of this inductor is defined by the length of the arc BC, and in Fig. 10 is -*j*0.5 to *j*0.43 i.e. a total of *j*0.93. This reactance must of course be denormalised before evaluation. Point C represents an inductive impedance which is equivalent to the admittance shown at Point D. The addition of shunt reactance moves the input admittance to the centre of the chart, and has a value of *j*2.0 Point D should be chosen such that it lies on unity impedance/conductance circle: thus a locus of points for point C exists.

This procedure allows for design of the matching at any one frequency. Wide band matching is more difficult and other techniques are needed. Of these, one of the most powerful is to absorb the reactance into a low pass filter form of ladder network: if the values are suitably chosen, the resulting input impedance is dependent upon the reflection coefficient of the filter.

At frequencies above about 400MHz, it becomes practical to use sections of transmission line to provide the necessary reactances, and reference to one of the standard works on the subject is recommended.

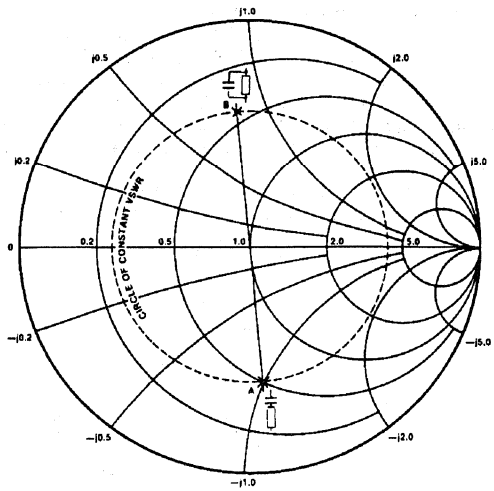


Fig.8 Series reactance to parallel admittance conversion

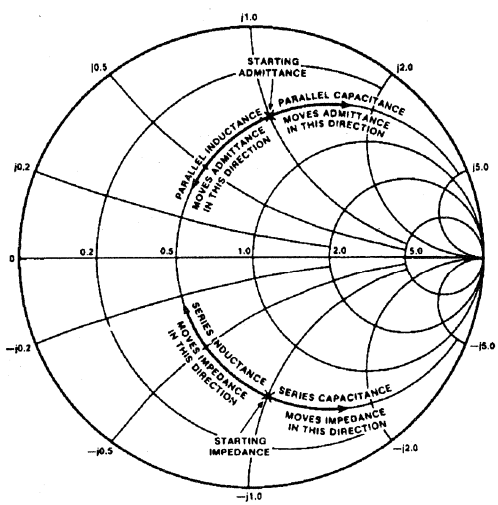


Fig.9 Effects of series and shunt reactance

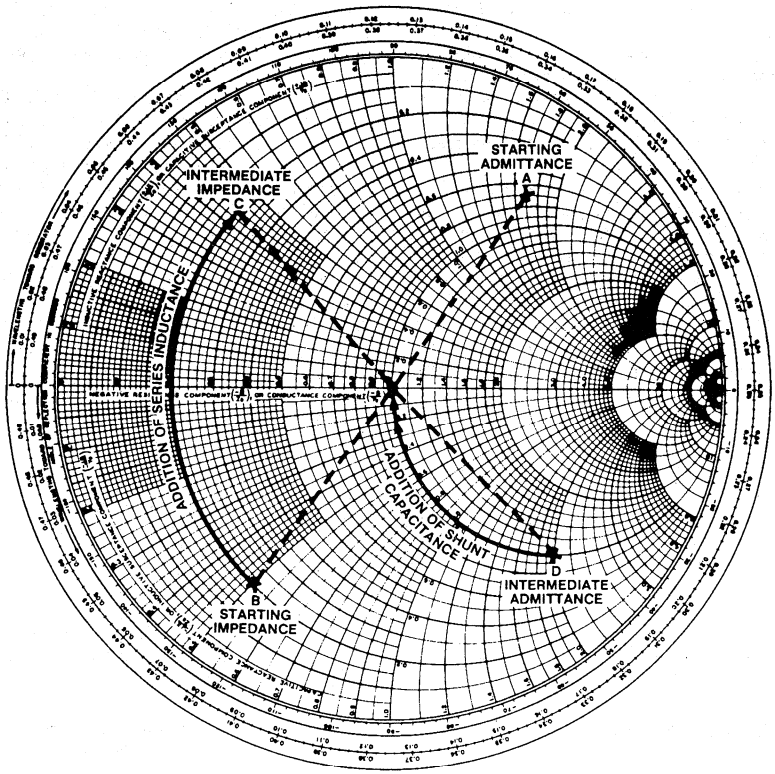


Fig.10 Matching design using the Smith Chart

PHASE NOISE AND DIVIDERS

Phase noise is becoming increasingly important in systems and it is necessary to minimise its effects. First, however, phase noise must be defined.

A spectrally pure signal of a given frequencywould appear on a perfect spectrum analyser display as a single straight line as in Fig 11. If the signal is frequency modulated with a discrete modulation frequency, the result will be a comb of frequencies as in Fig.12, while modulation with noise will produce an output spectrum as in Fig.13. Note that the noise density decreases as the offset from the carrier increases. This effect is the result of the effectively lower modulation index *m.* In the case of a Voltage Controlled Oscillator modulated by white noise, a similar effect will be seen, because for a given deviation f, the modulation index *m, (= 1/fmod) is* greater for lower frequencies than for higher frequencies. Thus the number of sidebands is greater for lower frequencies, and the noise spectral density increases as the carrier is approached.

The causes of phase noise in dividers are not well understood, but the effects of internal noise on the switching point of the various flip-flops cannot be ignored The 1/f noise will obviously inter-relate to the phase noise if this is so, and it is interesting to note that various measurements of Gallium Arsenide dividers suggest performances 20 to 30dB worse than for ECL dividers. Rohde (ref.4) suggests that TTL and CMOS are much better than ECL, although little work has been published in this field, possibly because of the measurement difficulties.

The non-saturating nature of ECL, the fact that the transistors are designed and processed for high speed rather than low noise, and the smaller signal swings than TTL or CMOS, lead intuitively to the conclusion that ECL should be worse than either of these other two logic families. This appears to be the case, while the high 1/f noise knee of Gallium Arsenide devices leads to the high relatively close in phase noise.

Devices with slow output edges, such as open collector TTL output stages may also be expected to be worse, which is again born out in practice.

Minimisation of phase noise requires the use of well filtered supplies, correct input levels and minimisation of noise in level changing circuitry.

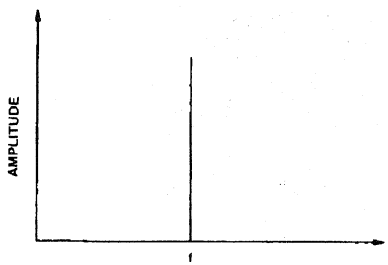


Fig.11 Spectrally pure signal

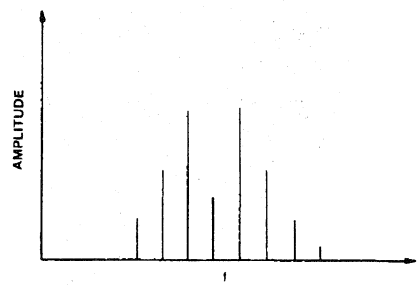


Fig.12 Spectrally pure signal, frequency modulated with single tone

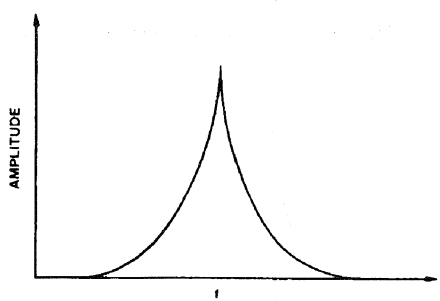


Fig.13 Spectrally pure signal, frequency modulated by noise

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2. Microwave Filters, Impedance - Matching Networks and Coupling Structures, Matthei, Young, Jones, Artech House 1980. SBN 0890060991.
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Intermodulation, Phase Noise and Dynamic Range

The radio receiver operates in a non-benign environment. It needs to pick out a very weak wanted signal from a background of noise at the same time as it rejects a large number to much stronger unwanted signals. These may be present either fortuitously as in the case of the overcrowded radio spectrum, or because of deliberate action, as in the case of Electronic Warfare. In either case, the use of suitable devices may considerably influence the job of the equipment designer.

Dynamic range is a 'catch all' term, applied to limitations of intermodulation or phase noise: it has many definitions depending upon the application. Firstly, however, it is advisable to define those terms which limit the dynamic range of a receiver.

INTERMODULATION

This is described as the *'result of a non linear transfer characteristic'*. The mathematics have been exhaustively treated and Ref.1 is recommended to those interested.

The effects of intermodulation are similar to those produced by mixing and harmonic production, in so far as the application of two signals of frequencies f_1 and f_2 produce outputs of $2f_2 - f_1$ $2f_1 - f_2$, $2f_1$, $2f_2$ etc. The levels of these signals are dependent upon the actual transfer function of the device and thus vary with device type. For example a truly square law device such as a perfect FET, produces no third order products ($2f_2 - f_1$, $2f_1 - f_2$). Intermodulation products are additional to the harmonics $2f_1$, $2f_2$, $3f_1$, $3f_2$ etc. Fig.1 shows intermodulation products diagrammatically.

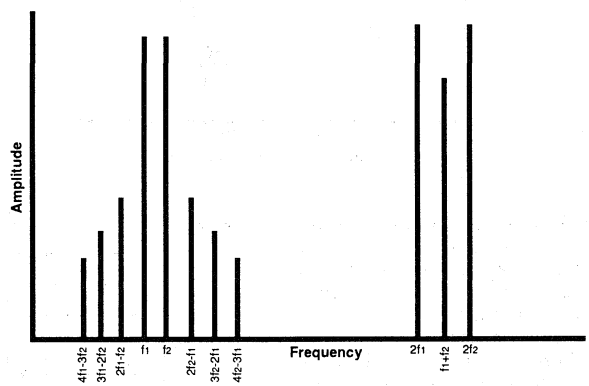

Fig. 1 Intermodulation Products

The effects of intermodulation are to produce unwanted signals and these degrade the effective signal to noise ratio of the wanted signal. Consider firstly the discrete case of a weak wanted signal on 7.010MHz and two large unwanted signals on 7.020 and 7.030MHz. A third order product ($2 \times 7.02 - 7.03$) falls on the wanted signal, and may completely drown it out. Fig.2 shows the total HF spectrum from 1.5 to 41.5MHz and Fig.3 shows the integrated power at the front end of a receiver tuned to 7MHz. It may be seen that just as white light is made up from all the colours of the spectrum, so the total power produced by so many signals approximates to a large wide band noise signal. Now, it has already been shown that two signals, f_1 and f_2, produce third order intermodulation products of $2f_1 - f_2$ and $2f_2 - f_1$. The signals will produce third order products somewhat greater in number, viz: $2f_1 - f_2$, $2f_1 - f_3$, $2f_2 - f_1$, $2f_2 - f_3$, $2f_1 - f_3$, and $2f_3 - f_2$. An increase in the number of input signals will multiply greatly the effects of intermodulation, and will manifest as a rise in the noise floor of the receiver.

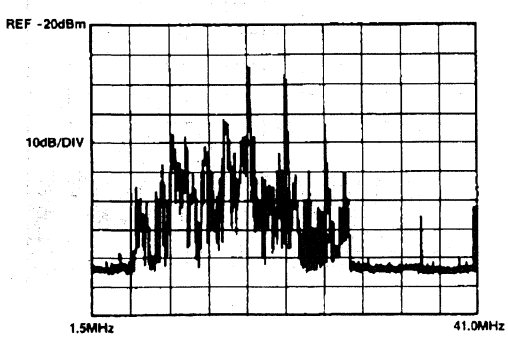

Fig. 2

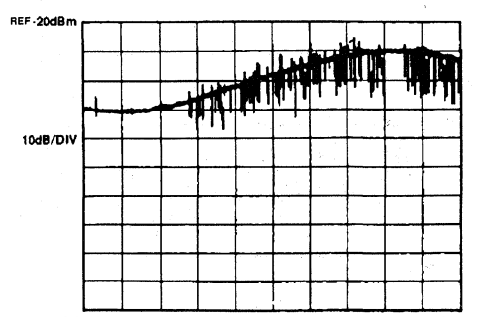

Fig. 3

The amplitude relationships of the third order intermodulation products and the fundamental tones may be derived from Ref.1, where it is shown that the intermodulation product amplitude is proportional to the cube of the input signal level. Thus an increase of 3dB in input level will produce an increase of 9dB in the levels of the intermodulation products. Fig.4 shows this in graphic form, and the point where the graphs of fundamental power and intermodulation power cross is the *Third Order Intercept Point.*

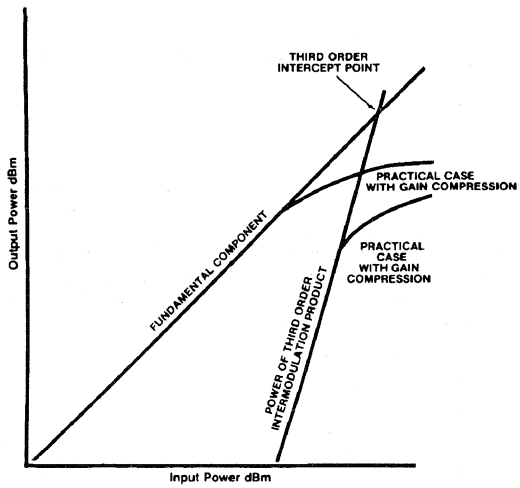

Fig. 4 3rd order intercept

The third order intercept point is, however, a purely theoretical concept. This is because the worst possible intermodulation ratio is 13dB (Ref.2), so that in fact the two graphs never cross. In addition, the finite output power capability of the device leads to *Gain Compression.*

Thus, it is apparent that the intermodulation produced noise floor in a receiver is related to the intercept point. Figs.5, 6 and 7 show the noise floor produced by various intercept points, in a receiver fed from an antenna - a realistic test! Fig.5 shows that a large number of signals are below the noise floor and are thus lost; this represents a 0dBm intercept point. Fig.7 shows a +20dBm intercept noise floor, and it is obvious that many more signals may be received.

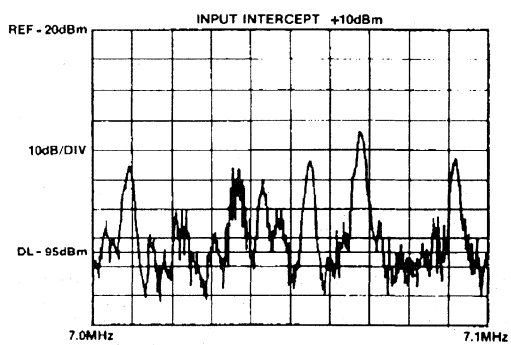

Fig. 6

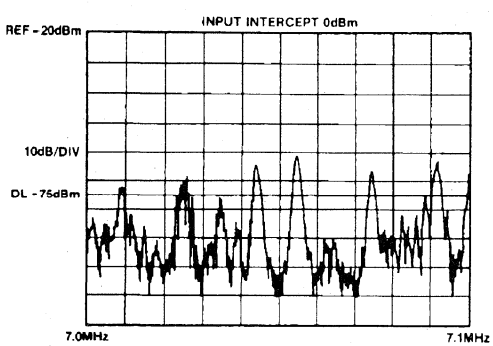

Fig. 5

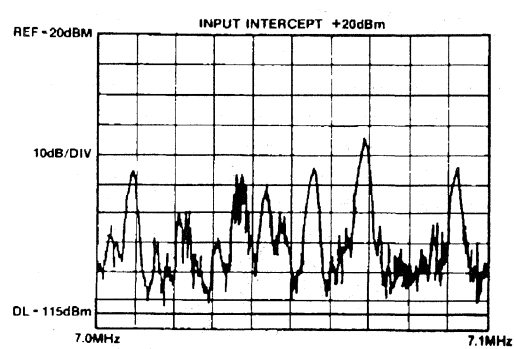

Fig. 7

Because of the rate at which intermodulation products increase with input level (3dB on the intermodulation products for 1dB on the fundamental), the addition of an attenuator at the front end can improve the signal to noise ratio, as an increase in attenuation of 3dB will reduce the wanted signal by 3dB, but the intermodulation will decrease by 9dB. However, it is a fair comment that aerial attenuators are an admission of defeat, as suitable design does not require them!

The concept of dynamic range is often used when discussing intermodulation. Fig.8 shows total receiver dynamic range, which is defined as the spurious Free Dynamic Range. Obviously an intermodulation product lying below the receiver noise floor may be ignored. Thus the usable dynamic range is that input range between the noise floor and the input level at which the intermodulation product reaches the noise floor. In fact

$$DR = \frac{2}{3}(I_3 - NF) \quad \ldots (1)$$

Where DR is the dynamic range in dB
I_3 is the intermodulation input intercept point in dBm
NF is the noise floor in dBm.

Note that in any particular receiver, the noise floor is related to the bandwidth; dynamic range is similarly so related.

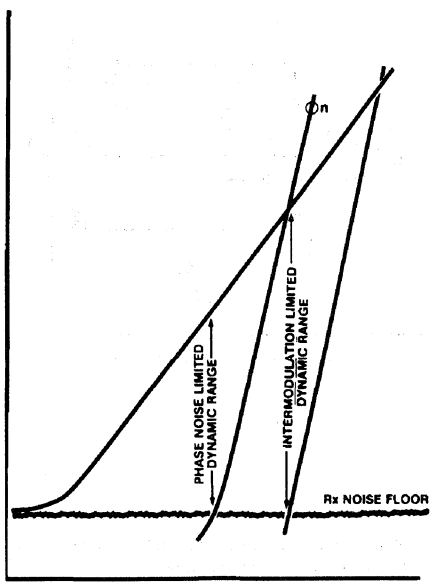

Fig. 8

HF receivers will often require input intercept points of +20dBm or more. The usable noise factor of HF receivers is normally 10-12dB: exceptionally 7 or 8dB may be required when small whip antennas are used. An SSB bandwidth would have a dynamic range from (1) of 1 05.3dB. The same receiver with a 100Hz CW bandwidth would have a dynamic range of 114.6dB and thus dynamic range is quite often a confusing and imprecise term.

Appendix A defines a quantitive method of Intermodulation Noise Floor assessment, developed later than the data in Figs.5 to 7.

VHF receivers require noise figures of 1 or 2dB for most critical applications, and where co-sited transmitters are concerned, signals at 0dBm or more are not uncommon. However, such signals are usually separated by at least 5 % in frequency and filters can be provided. Close-in signals at levels of -20dBm are not uncommon, and dynamic ranges in SSB bandwidths of about 98dB are required.

The achievement of high input intercept points and low noise factors is not necessarily easy. The usual superhet architecture follows the mixer with some sort of filter, frequently a crystal filter, and the performance of this filter may well limit the performance. Crystal filters are not the linear reciprocal two-port networks that theory suggests, being neither linear nor reciprocal It has been suggested that the IMD is produced by ferrite cored transformers, but experiments have shown that ladder filters with no transformers suffer similarly. Thus, although ferrite cored transformers can contribute, other mechanisms dominate in these components. The most probable is the failure of the piezo-electric material to follow Hooke's Law at high input levels, and possibly the use of crystal cuts other than AT could help insofar as the relative mechanical crystal distortion is reduced. The use of SAW filters is attractive, since they are not bulk wave devices and do not suffer to such an extent from IMD; however, it is necessary to use a resonant SAW filter to achieve the necessary bandwidths and low insertion losses.

The design of active components such as amplifiers is relatively straightforward. Amplifiers of low noise and high dynamic range are fairly easy to produce, especially with transformer feedback, although where high reverse isolation is required, care must be taken. Mixers are, however, another matter.

Probably the most popular mixer is the diode ring (Fig.9). Although popular, this mixer does have some drawbacks, which have been well documented. These are:

Insertion loss (normally about 7dB)
High LO drive power (up to +27dBm)
Termination sensitive (needs a wideband 50Ω)
Poor interport isolation (40dB)

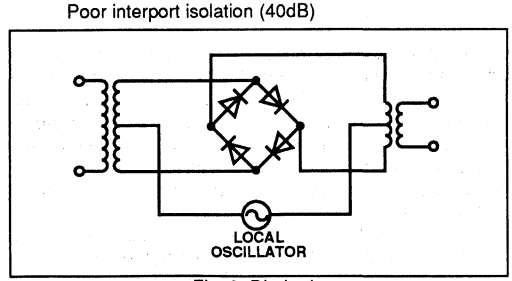

Fig. 9 Diode ring

The insertion loss is a parameter which may be classed merely as annoying, although it does limit the overall noise figure of the receiving system. The high LO drive power means a large amount of DC is required, affecting power budgets in a disastrous way, while termination sensitivity may mean the full potential of the mixer cannot be realised.

For the diode ring to perform adequately, a good termination 'from DC to daylight' is required - definitely at the image frequency (LO ± sig. freq.) - and preferably at the harmonics as well. Finally, interport isolation of 40dB with a +27dBm LO still leaves -13dBm of LO radiation to be filtered or otherwise suppressed before reaching the antenna.

A further problem with the simple diode ring of this form is that the 'OFF' diodes are only oH by the forward voltage drop of the ON diodes. Thus the application of an input which exceeds this OFF voltage leads to the diodes trying to turn ON, giving gain compression and reduced IMD performance.

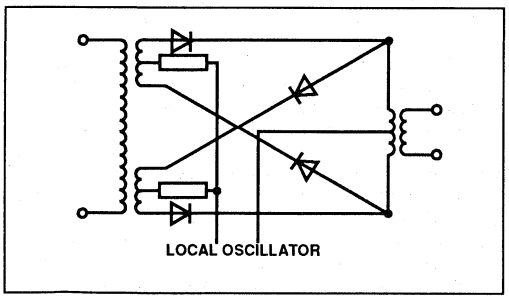

Fig. 10 Resistive loaded high intercept point mixer

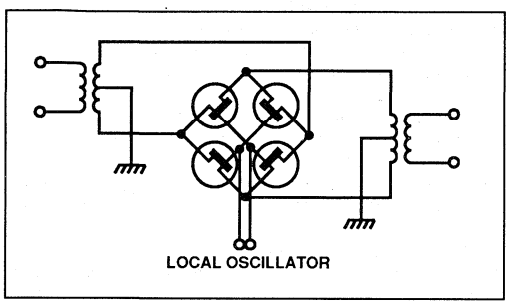

Fig. 11 Quad MOSFET commutative mixer

Fig.10 shows a variation of this in which series resistors are added. The current flow through these resistors increases the reverse bias on the OFF diodes which gives a higher gain compression point: such a mixer can give +36dBm intercept points with a +30dBm of LO drive. Nevertheless, as is common to all commutative mixers, the intermodulation performance is related to the termination, and the LO radiation from the input port is relatively high.

Variations of this form of mixer include the Rafuse Quad MOSFET mixer of Fig.11, which suffers with many of the same problems. Fig.12 shows a dual VMOS mixer capable of good performance, but requiring a large amount of DC power and with limited isolation of the LO injection.

Many advantages accrue to the choice of the transistor tree type of approach (Fig.13). Here the input signal produces a current in the collectors of the lower transistors and this current is commutated by the upper set of switching transistors. Because the current is to a first order approximation independent of collector voltage, the transistor tree does not exhibit the sensitivity to load impedance that the diode ring does, and indeed, by the use of suitable load impedances, gain may be achieved. The non-linearity of the voltage to current conversion in the base emitter junctions of the bottom transistors is the major cause of intermodulation, but by using suitably large transistors and emitter degeneration, very high performances (+32dBm input intercept) can be achieved.

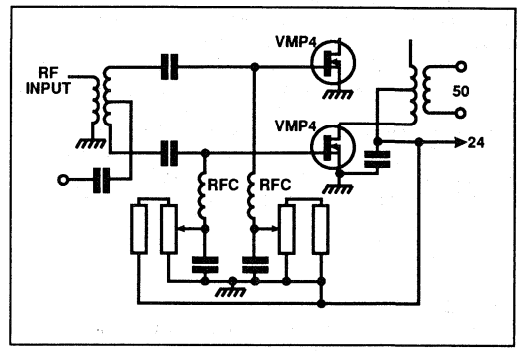

Fig. 12 VMOS mixer

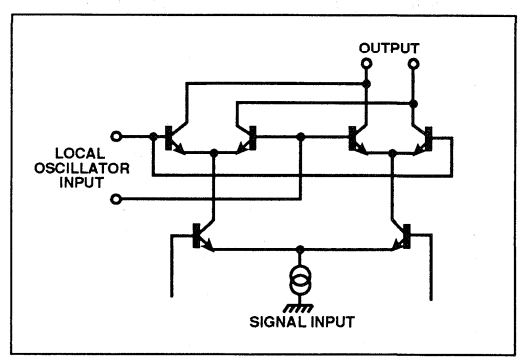

Fig. 13 The transistor tree

PHASE NOISE

The mixing process for the superhet receiver is shown in Fig.14, where an incoming signal mixes with the local oscillator to produce the intermediate frequency. Fig.15 shows the effect of noise modulation on the LO, where the noise sidebands of the LO mix with a strong, off channel signal to produce the IF. This means that the phase noise performance of the LO affects the capability of the receiver to reject off channel signals, and thus the receiver selectivity is not necessarily defined by the signal path filters. This phenomena is referred to as *Reciprocal Mixing,* and has tended to become more prominent with the increased use of frequency synthesisers in equipments.

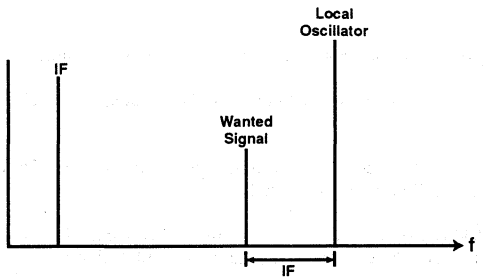

Fig. 14 Superhet mixing

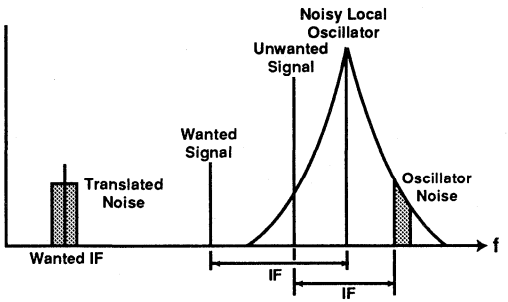

Fig. 15 Reciprocal mixing

The performance level requirements of receivers is dependent upon the application. Some European mobile radio specifications call for 70dB of adjacent channel rejection, equating to some -122dBc/Hz, while an HF receiver requiring 60dB rejection in the adjacent sideband needs -94dBc/Hz at a 500Hz offset. The use of extremely high performance filters in the receiver can be completely negated if the phase noise is poor. For example, a receiver using a KVG XF9B filter with a rejection in the unwanted sideband of 80dB at 1.2kHz, would require a local oscillator with -114dBc/Hz phase noise at 1.2kHz if the filter performance was not to be degraded.

To put these levels in perspective, relatively few signals generators are adequate to the task of being the LO in such a system. For example, 'Industry Standards' like the HP8640B are not specified to be good enough: neither are the HP8642, Marconi 2017/2018, or Racal 9082, all of which are modern, high performance signal generators.

All this suggests that it is very easy to over-specify a receiver in terms of selectivity, and simple synthesisers are not necessarily ideal in all situations.

The ability of the receiver to receive weak wanted signals in the presence of strong unwanted signals is therefore determined not only by the intermodulation capabilities of the receiver, but by phase noise and filter selectivity.

The usual approach to high performance synthesis has used multiple loops for good close-in performance. Notable exceptions are those equipments using fractional N techniques with a single loop. Nevertheless, such equipments not generally specified as highly as multi-loop synthesisers. A vital part of the synthesiser is still the low noise VCO, for which many approaches are possible. This VCO performance should not be degraded by the addition of the synthesiser: careful choice of technologies is therefore essential. For example, Gallium Arsenide dividers are much worse in phase noise production than silicon, and amongst the silicon technologies, TTL is better than ECL.

From equation (1)

$$DR = \frac{2}{3}(I_{p3} - NF)\ \text{dB}$$

where I_{p3} = input intercept point dBm
NF = noise floor dBm

The phase noise governed dynamic range is given by

$$D_{R\Phi} = Pn + 10\log_{10}B\ Db \qquad (2)$$

Where P_n is the phase noise spectral density in dBc/Hz at any offset and B is the IF bandwidth in Hz.

(N.B. This is not quite correct if B is large enough such that noise floor is not effectively flat inside the IF bandwidth).

Ideally the ratio.

$$\frac{DR_{IM}}{DR\Phi}$$

should be 1 in a well designed receiver - i.e. the dynamic range limited by phase noise is equal to the dynamic range limited by intermodulation.

Certain aspects of low noise synthesiser design have been touched upon and Ref.6 provides further information.

The performance of a receiver in terms of its capabilities to handle input signals widely ranging in input level is dependent upon the receiver capability in terms of intermodulation and phase noise. Neglect of either of these parameters leads to performance degradation, and it has been shown that specifications are not only often difficult to meet, but sometimes contradictory in their requirements.

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APPENDIX A

Intermodulation is caused by odd order curvature in the transfer characteristic of a device. If two signals f_1 and f_2 are applied to a device with third order term in its transfer characteristic, the products are given by:

$(\cos f_1 + \cos f_2)^3 = \cos^3 f_1 + 3\cos^2 f_1 \cos f_2 + 3\cos^2 f_2 \cos f_1 + \cos^3 f_2$

from the trig identities $\cos^3 A$, $\cos^2 A$ and $\cos A \cos B$, this is

$^1/_4\cos^3 f_1 + {}^3/_4\cos f_1 + {}^3/_2\cos^2 f_1 \cos f_2 + {}^3/_2\cos f_1 \cos^2 f_2 + {}^3/_4\cos f_2 + {}^1/_4\cos^3 f_2 + {}^3/_4\cos f_2$

(where $f_1 = A$ and $f_2 = B$). Neglecting coefficients, the terms $\cos^2 f_1 \cos f_2$ and $\cos f_1 \cos^2 f_2$ are equal to

$\cos(2f_1 + f_2) + \cos(2f_1 - f_2)$ and

$\cos(2f_2 + f_1) + \cos(2f_2 - f_1)$

By inspection, it may be seen that frequencies off $f_1, f_2, 3f_1, 3f_2$, $(2f_1 \pm f_2)$ and $(2f_2 \pm f_1)$ are present in the output. Of these, only $2f_2 - f_1$, and $2f_1 - f_2$ are close to wanted frequencies f_1 and f_2. The application of three signals f_1, f_2 and f_3, produces a similar answer, in that the resulting products are:

$3f_1, 3f_2, 3f_3, f_1 + f_2 + f_3, f_1 + f_2 - f_3, f_1 - f_2 + f_3, f_1 - f_2 - f_3, f_2 - f_1 + f_3, f_2 - f_1 - f_3, -f_1 - f_2 - f_3, -f_1 - f_2 + f_3$

in addition to the products

$2f_1 \pm f_2, 2f_2 \pm f_1, 2f_2 \pm f_3, 2f_3 \pm f_2, 2f_1 \pm f_3, 2f_3 \pm f_1$

if a greater number of signals are applied such that the input may be represented by:

$\cos f_1 + \cos f_2 + \cos f_3 + \cos f_4 \ldots \cos f_n$

The result from third order curvature can be calculated from:

$(\cos f_1 + \cos f_2 + \cos f_3 + \cos f_4 \ldots \cos f_n)^3$

This expansion produces terms of

$\cos(f_1 \pm f_2 \pm f_3)$, $\cos(f_1 \pm f_2 \pm f_4)$, $\cos(f_1 \pm f_2 \pm f_n)$, etc from which it can be seen that the total number of products is:

$$\frac{n!}{3!(n-3)!} = 4 \times {}^1/_6 n\,(n-1)(n-2)$$

(The factor of 4 appears because each term has four possible sign configurations i.e. $\cos(f_1 + f_2 + f_3)$, $\cos(f_1 + f_2 - f_3)$ etc). This agrees with Ref A1.

By a similar reasoning, n signals produce:

$2n(n-1)$ products of the form $(2f_1 \pm f_2)$ $(2f_2 + f_1)$ etc and n 3rd harmonics.

Thus the total number of intermodulation products produced by third order distortion is:

$$n + 2n(n-) + {}^2/_3 n\,(n-1)(n-2) \qquad (1)$$

Reduction of the input bandwidth of the receiver modifies this. Consider, for example, a receiver with sub-octave filters, rather than the 'wide-open' situation analysed above. In this case, the third harmonics produced by any input signals will not fall within the tune band, as will some of the products such as $f_1 + f_2 + f_3$, $f_1 - f_2 - f_3$, etc. In this case, the total number of intermodulation products is reduced. There are only three possible sets of products of the form $f_1\, f_1 \pm f_2 \pm f_3$, i.e. $f_1 + f_2 - f_3$, $f_1 - f_2 + f_3$ and $f_3 - f_1 - f_2$ which can give products within the band. Note that for products to be considered, they must have an effective input frequency at the receiver mixer equivalent to an on-tune desired signal. In addition, products of the form $2f_1 + f_2$, $2f_2 + f_1$ etc are again out of band. Thus half of the $2n\,(n-1)$ products of this class are not able to cause problems and the total number of products to be considered is now:

$$n(n-1) + {}^1/_2 n\,(n-1)(n-2) \qquad (2)$$

This result does not agree with Barrs (Ref A2) who uses the results in (1). The results in (2) are an absolute worst case, insofar as a number of the intermodulation products are out of band.

(For the purposes of this analysis, IMD in a mixer is assumed to produce an 'on tune' signal. Thus not all the possible intermodulation frequencies appearing in a half octave bandwidth will be able to interfere).

The same arguments apply to narrower front end bandwidths. However, the narrower the front end bandwidth, the higher is the probability that the distribution of signals will produce IMD products outside the band. For example, a receiver with ±2.5% front end bandwidth tuned to 10MHz will accept signals in a band from 9.75 to 10.25MHz. Signals capable of producing a product of the form $2f_1 - f_2$ must have one of the signals (f_1 or f_2) in the band 9.875 - 10.25 for a product to appear on tune. Thus the two signal apparent bandwidth is less than would be expected. Similar constraints apply to the $f_1 + f_2 - f_3$ product.

Similar arguments apply to other orders of curvature. Second order curvature, for example, will not produce any products in band for input bandwidths of less than 2:1 in frequency ratio.

The actual levels of intermodulation produced can be predicted from reference A1. In practice, the situation is that the input signals to a receiver are rarely all of equal unvarying amplitude and assumptions are made from the input intercept points and the input signal density.

If a series of amplitude cells are established for given frequency ranges, such as that in Table 1, then a prediction of the number of intermodulation products for any given number of input signals and amplitudes may be obtained, either from equation (1) or (2) (as applicable) or from Ref A1 (for higher orders). Where the input bandwidth of the receiver is deliberately minimised, the maximum cell size in the frequency domain should be equal to the input bandwidth .

The total input power in each cell is

$$nPav$$

where n is the number of signals and Pav is the average power of each signal.

A worst case situation is to assume that all signals in the cell are equal to the cell upper power limit boundary, e.g. if the cell amplitude range is from -40 to -30dBm, then an assumption that all signals in this cell are at -30dBm is a worst case.

If, however, it is assumed that signals will have a Gaussian distribution of input levels within a cell, then the total input power becomes:

$$Pt = 0.55nP$$

where Pt is the total power
n is the number of signals
P is the power level at the upper boundary of the cell

Because the total IMD power is the sum of all the IMD powers, the average input power is

$$Pav = \frac{0.565nP}{n}$$

The IMD power produced by third order curvature is:

$10 \log_{10} [{}^{1}/_{3} n(2n^2 + 1)]$ Antilog ${}^{1}/_{10}$[Pav- 3(I3- Pav)]dBm

where P_{IM} is the total power of the intermodulation products
I3 is the third order input intercept point

Because the coefficients of the amplitudes of the intermodulation products are (depending on product)

a^3, a^2b, ab^2, abc, b^3

where a, b and c are approximately equal, the use of a^3 as the general coefficient is justified.

From equations (1) or (2) and (3), the total IMD power and number of products may be calculated. As 'n' increase in number, the number of products will mean that the resultant IMD tends more to a noise floor increase in the receiver, thus reducing the effective sensitivity.

The amount of this degradation is such that the noise floor is:

$$\frac{{}^{2}/_{3}\,(0.55nP)^3}{I_3} \quad X \quad \frac{I_3}{(f_{max} - f_{min})} \quad X\,\Delta f$$

where $(f_{max} - f_{min})$ is the bandwidth prior to the first intermodulating stage. Δf is signal bandwidth in a linear system.

The Gaussian Factor of 0.55 is somewhat arbitrary, since errors in this assumption are cubed.

The intermodulation Limited Dynamic Range is

$${}^{2}/_{3}\,(I_3 + 174 - 10 \log_{10} \Delta f - NF)$$

where NF is the Noise Figure in dB.

The effects of Reciprocal Mixing are similar, except that signals may be taken one at a time. The performance is affected by the frequency separation between an 'off-tune' interfering signal and an 'on-tune' wanted signal unless the separation is such that the oscillator noise floor has been reached. Here again, reduction of front end bandwidth reduces the number of signals.

Generally speaking, the effects of reciprocal mixing are limited to close in effects - say within ±50kHz, unless very poor synthesisers are used.

The response at some separation f_0 from the tune frequency is: $(L - 10 \log_{10} 10\Delta f)$dB where L is phase noise spectral density in dBc/Hz and Δf is the IF bandwidth.

This assumes that the spectral density does not change within the receiver bandwidth: Ref A1 shows this to be generally applicable for narrow bandwidths.

The intermodulation free dynamic range is defined as:

${}^{2}/_{3}$[I3 - noise floor] = ${}^{2}/_{3}$[I3 + 174 -10 $\log_{10} \Delta f$ - NF]dB

where I3 is the input 3rd order intercept point in dBm
NF is the noise figure in dB
Δf is the IF bandwidth in Hz

It has been claimed that there is 6dB rejection of phase noise in diode commutative mixers. Thus the relationship between IMD and phase noise can be expressed as:

IMD dynamic range = phase noise dynamic range +6dB = $(L - 10 \log_{10} \Delta f) + 6dB$

Thus at any offset, it is important to ensure that the two dynamic ranges are approximately equal if performance is not be be compromised.

A receiver for example with an input intercept point of +20dBm and input signals of -30dBm will produce an IMD product at -130dBm which, for an HFreceiver with a noise factor of 8dB, will be just above the noise floor, in an SSB bandwidth. The noise floor of the LO will need to be such that the noise is at -133dBm if degradation is not to occur, and this will be produced by a noise floor of -137dBc/Hz in the synthesiser at the frequency separation of the signals in question. Thus the high intermodulation performance may well be compromised by poor phase noise.

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Wideband VHF Antenna Booster using the SL560

AN170-2

The following is a brief description of a 40-260MHz antenna amplifier module suitable for any 50Ω VHF system. The module is constructed on a single sided PCB and layout is not critical as long as the usual precautions for VHF construction are observed

An unusual feature of this module is the use of a transmission line transformer to provide 'noiseless' emitter feedback to the SL560.

The component count is minimal, i.e. 4 resistors, 7 capacitors, 2 inductors, 1 transformer, 1 SL560 IC and 2 diodes. The circuit for this application is shown in Fig.1.

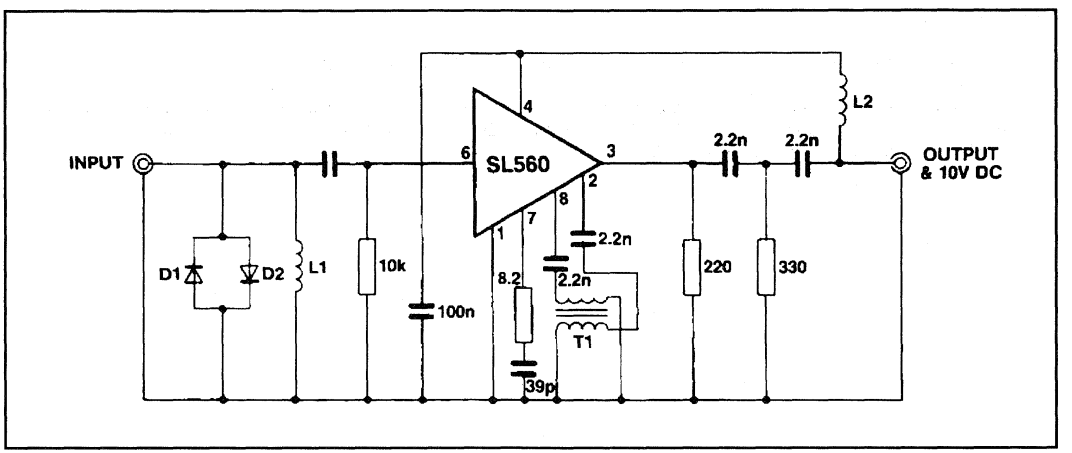


Fig.1

CONSTRUCTION

D_1 and D_2 are any general purpose silicon diodes.
L_1 is 8 turns of 26 gauge, 1/8 inch internal diameter.
L_2 is 20 turns of 26 gauge, 3/16 inch internal diameter.
T_1 consists of two lengths of 34 gauge wire approximately 6 inches in length, twisted together (8 twists/inch) and wound on a 6-hole ferrite bead (Mullard FX1898).
L_1 provides a degree of high pass filtering, some measure of protection against lighting by virtue of the DC path to earth, and it improves input SWR.
Resistor and capacitor values are not critical.
The module is powered through the coaxial cable and requires 10V at 30mA.

PERFORMANCE SPECIFICATION

The gain, 2nd and 3rd order intermodulation intercepts and SWR against frequency is shown in Fig.2. The gain flatness is within 5dB and the noise figure is better than 8dB.

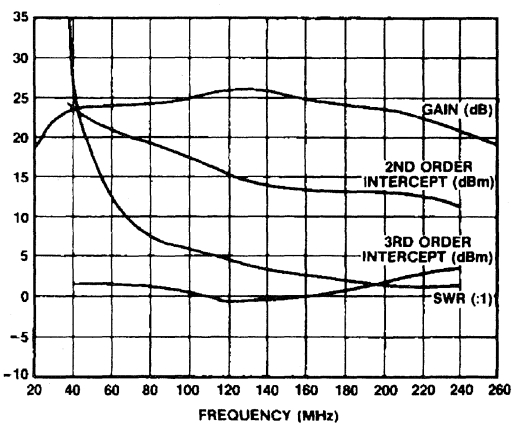


Fig.2

Tuned Amplifier Application for the SL6140

The SL6140 wideband AGC amplifier, when used in a 50Ω system, has a gain of 15dB. By tuning, or matching, the inputs and outputs of the device the gain can be increased. This produces a higher gain amplifier that will work over a limited bandwidth. The bandwidth of the amplifier depends upon the Q factor of the tuned/matching circuits used.

Fig. 1 shows a single ended amplifier with tuned input and output networks.

The input circuit consists of a parallel LC network connected across the differential inputs. The input signal is applied to one input, via a coupling capacitor (C1), the other input being decoupled. The coupling capacitor also forms part of the impedance matching network, matching a 50Ω source with the high impedance of the device (see Smith chart, Fig. 3). The tuned frequency is given by the following equation:

$$f = \frac{1}{2\pi \frac{\sqrt{L \times C \times C1}}{\sqrt{(C + C1)}}}$$

The output circuit consists of a parallel LC network connected from one of the open collector ouputs of the device to V_{CC}. The coupling capacitor (C2) and LC network transforms the 50Ω load to a high impedance load for the open collector outputs of the device, hence improving the gain.

By adjusting C1 and C2 the gain can be optimised, but if too high an impedance is seen by the input or output of the device the circuit may oscillate. L1 and L2 are adjusted to set the tuned frequency.

The high gain is achieved at the expense of bandwidth, so for maximum gain the matching network should be designed to provide the minimum bandwidth necessary for the particular application.

An alternative method of tuning the output of the device is to transformer-couple to the 50Ω load as shown in Fig. 2. The primary winding is connected across the outputs (a centre tap providing V_{CC}) and resonated at the required frequency with a capacitor. This circuit has a 6dB improvement of gain over the previous circuit as both outputs are used.

PCB LAYOUT

For best performance a ground plane should be used with 50Ω source and load. Also the matching network and decoupling capacitors should be placed as close to the device as possible.

If a very high gain, low bandwidth amplifier is required the addition of some shielding between input and output may be necessary to prevent oscillation.

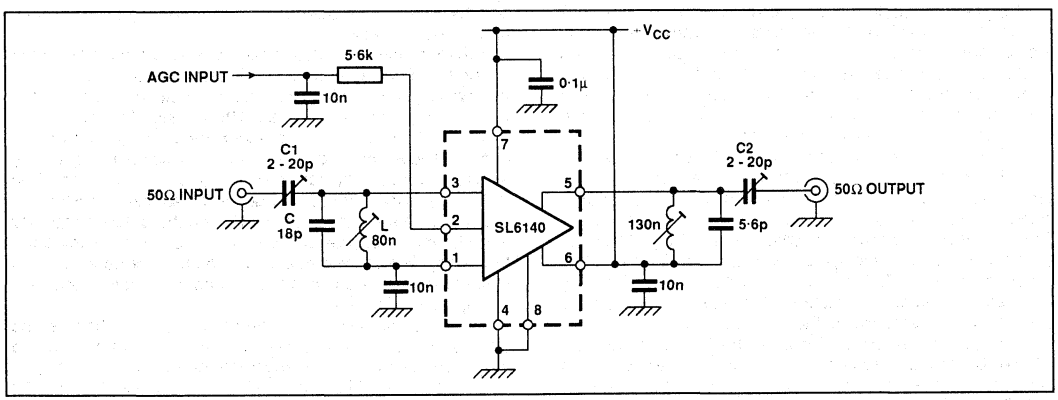


Fig. 1 A 100MHz tuned amplifier application with 35dB power gain (CM pinout)

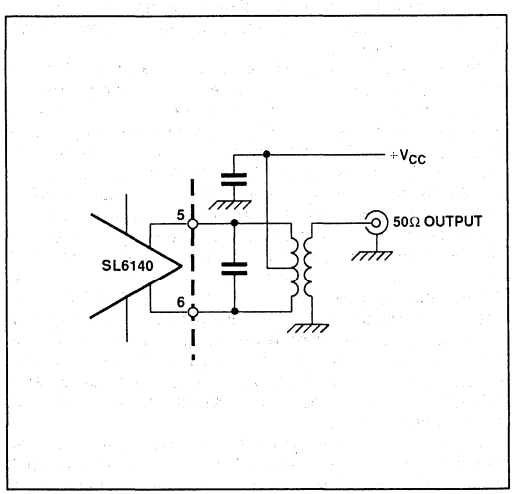


Fig. 2 Differential tuned output

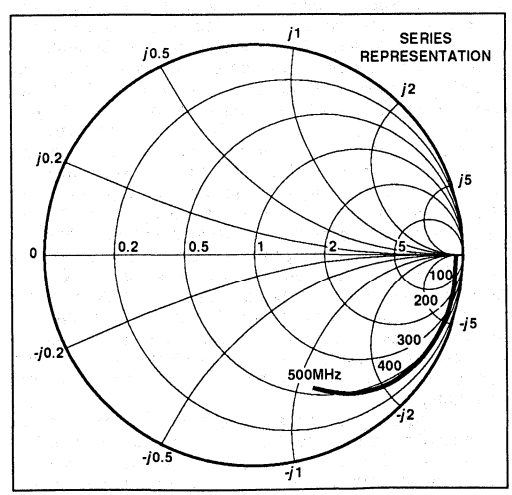


Fig. 3 Input impedance of SL6140 (50Ω normalised)

USING THE SP2002

DIRECT DIGITAL FREQUENCY SYNTHESISER

INTRODUCTION

Direct digital synthesiser products have been available in the form of single chip MOS low frequency designs or as modules for high frequency applications for some years. The SP2002 breaks new ground in providing a single chip design in a 68 lead pin grid array package capable of operating at output frequencies up to 400MHz with a 1600 MHz clock. Included on the chip are dual 8 bit D–A converters and sine and cosine ROM look up tables to provide qadrature output signals. The circuit consumes only 5W from a single 4.5V power supply.

SPURS

The greatest problem experienced when applying a DDS is the presence of unwanted spurious frequencies or spurs in the output spectrum. These spurious frequencies are produced by non linearity in the DAC and by quantisation errors produced by the design of the DDS system. At some frequencies these spurs can appear close to the required carrier and are therefore very difficult to filter out.

Referring to the block diagram in Fig. 1 it will be seen that only the 8 most significant bits of the accumulator are processed so that regardless of the DAC the output voltage generated for any sampled point can only be approximate. This truncation error and any additional inaccuracy introduced by the DAC lead to the generation of spurs in the output spectrum of the DDS. The spur amplitude can be reduced by increasing the number of accumulator bits used to determine the output and by improving the DAC accuracy.

The spur amplitudes produced by the SP2002 tend to be affected by the output rather than the clock frequency. Figs.2a and 2b show the worst case spur levels at an output frequency of 100MHz with a clock frequency of 400MHz and 1600MHz and as can be seen in both cases the worst spur level is very close to the theoretical limit of –48dBc. The worst case spur level remains close to –48dBc at all output frequencies up to about 125MHz but degrades above this frequency to about –45dBc at 200MHz, –40dBc at 300MHz and –31dBc at the maximum output of 400MHz. Worst case spur levels at these frequencies are shown in Figs. 3a, 3b and 3c. The actual input codes and clock frequency used to produce the plots are shown in each case and a calculation will show that the combination of clock input codes does not give the exact 100MHz or 200MHz output. The codes were chosen to give easily observable spurs closely spaced about the carrier.

A difficulty in determining the worst case spur for any output frequency is that there is often a "close in series" and another further out which must both be examined separately to find the spur with the greatest magnitude. This effect can be seen by examining Figs. 3b and 4 which show the "close in" and "far out" spurs at 312MHz output for identical clock and input conditions. In this case the "far out" spur has the greater amplitude.

The frequency of the spurs can be predicted and in systems with reasonably widely spaced channels it is possible by careful choice of clock frequency to ensure a minimum frequency separation of the closest spur at all the required tuning points. Assume a system is required to tune over the frequency range of 100 to 120MHz in 50KHz steps. Using a clock frequency of 1638.4MHz will give a minimum frequency increment using the LSB input of the tuning bus of 0.762939453Hz. Bit 16 of the tuning bus will produce a tuning increment of exactly 50kHz and in order to tune any of the required frequencies between 100 and 120MHz it will not be necessary to use any less significant input bits than bit 16. Since no spurs will be produced closer to carrier than the incremental frequency of the least significant input bit used, this scheme will guarantee no spurs occur less than 50KHz from carrier. By using the DDS in conjunction with a phased locked loop synthesiser as shown in Fig. 5 it is possible to design the PLL so that the loop bandwidth is less than 50kHz thus removing any spurs from the final output. The PLL can also be used to increase the output frequency of the system to any desired value.

When the system requires very close channel spacing the hybrid PLL/DDS approach may not be applicable since very narrow loop bandwidths may be required to suppress the close in spurs generated by use of the low significant bits of the input bus, thus slowing up the loop response time. In these circumstances the use of frequency division using widely available prescalers can provide a better solution. The frequency divider effectively reduces the spur level but has the possible disadvantage of also reducing the output frequency and channel step size at the same time. By combining the frequency division with mixing, the output frequency can be shifted to any desired point in the spectrum but the reduction in step size will remain.

The combination of mixing and dividing is very flexible and an almost infinite range of possibilities exist, but the method may require considerable additional hardware in the shapes of amplifiers and filters to produce a workable system. An experimental circuit designed to explain the technique is shown in Fig. 6. A number of amplifiers not shown in the circuit diagram were required to maintain signal levels at an acceptable amplitude.

The input clock at 1638.4MHz is used to drive the SP2002 and is divided by four to provide the LO signal to the subsequent mixer stages. The chosen operating frequency range for the output is 135–137MHz and to keep the operating frequency of the filters and mixers at practical values the division and mixing is broken down into two parts. Since the total division ratio in the system amounts to 16, the 2MHz at the SP2002 output, requiring the SP2002 to tune between 112 and 144MHz. A low pass filter with cut off frequency just above 144MHz follows the SP2002 to remove any out of band spurious signals and the filtered output is then mixed with the divided clock to produce an IF in the range 521.6 – 553.6MHz. A band pass filter after the mixer removes the image frequency and the output is then divided by four to produce a new IF from 130.4 – 138.4MHz. A second bandpass filter removes the harmonics from the divided output before the mix up and divide sequence is repeated with essential filtering to produce the final output signal.

The spectrum analyser plots shown in Figs.7a and 7b show the unprocessed output from the SP2002 and the final output from the mix and divide system at a suitable spur producing frequency. Greater spur reduction could be obtained by

cascading more mix and divide stages at the expense of frequency coverage.

For any output frequency it is possible to calculate the position of the spurs since they are harmonically related to the output frequency but are imaged back into the DDS bandwidth by the Nyquist limit. Using a clock frequency of 1638.4MHz and with an output frequency of 409.5MHz (close to ¼ of the clock) a series of spurs equally spaced on both sides of the carrier will be observed. (See Fig. 8). The third harmonic of the output frequency (at 1228.5MHz) will produce a spur at 409.9MHz, 400kHz above carrier when folded back from the Nyquist limit at half the clock frequency. The fifth harmonic will produce a spur at 409.1MHz, 400kHz below carrier and the seventh a spur at 410.3MHz, 800kHz above carrier. Continuing this process for the odd order harmonics will produce the characteristic comb of spurs of gradually diminishing amplitude spaced at 400kHz intervals shown in Fig. 8.

As more bits are programmed and the tuned frequency becomes closer to ¼ of the clock, the separation of the spurs becomes less until eventually they become merged with the carrier due to the limited resolution of the spectrum analyser. The crowding of the spurs close to the carrier at output frequencies close to integer divisions of the clock frequency (1/4, 1/3 etc) makes these the best points to measure the spur amplitude.

FREQUENCY SWEEP OR "CHIRP" GENERATION

One of the most important applications for direct digital synthesis is the generation of frequency sweep or "chirp" waveforms where the input programming data is incremented between two values by repeatedly adding a fixed number. The design requirements for an accumulator for DDS applications are different from those encountered in computing since in a DDS, the accumulated result must always be available at a fixed time interval. In computing the correct value can be made available at a varying time interval without affecting the accuracy of the final result.

A full parallel adder working at 1600MHz would be very difficult to design because in the worst case the carry would need to propagate through the logic of 31 accumulator stages in one clock cycle. To overcome this problem a pipelined accumulator is used in the SP2002, a partial block diagram being shown in Fig. 9. In this design, the carry from each stage is clocked into a d type flip flop and added to the sum from the next most significant stage one clock pulse later. A pipelined accumulator of this type introduces a progressive delay in processing input data of one clock cycle per bit, starting from the most significant input. A change to the least significant bit requires 30 clock cycles to propagate through the accumulator and produce a correct result whereas the most significant bit requires only one. Whilst the input data remains static, the accumulator produces a correct result at each clock pulse, but when the input data changes, the accumulator can give an incorrect result for a number of clock cycles up to 30 depending on the numbers involved in the change of input data. The result of this pipelining is that any frequency change requiring more than one input bit to change will not result in a perfectly phase coherent transition unless the input data is applied with a delay opposite to that introduced by the accumulator. For many applications the resulting glitch will be insignificant but for applications such as fast chirp generators where a smooth sweep is required, some additional hardware to produce the required input delay will be necessary.

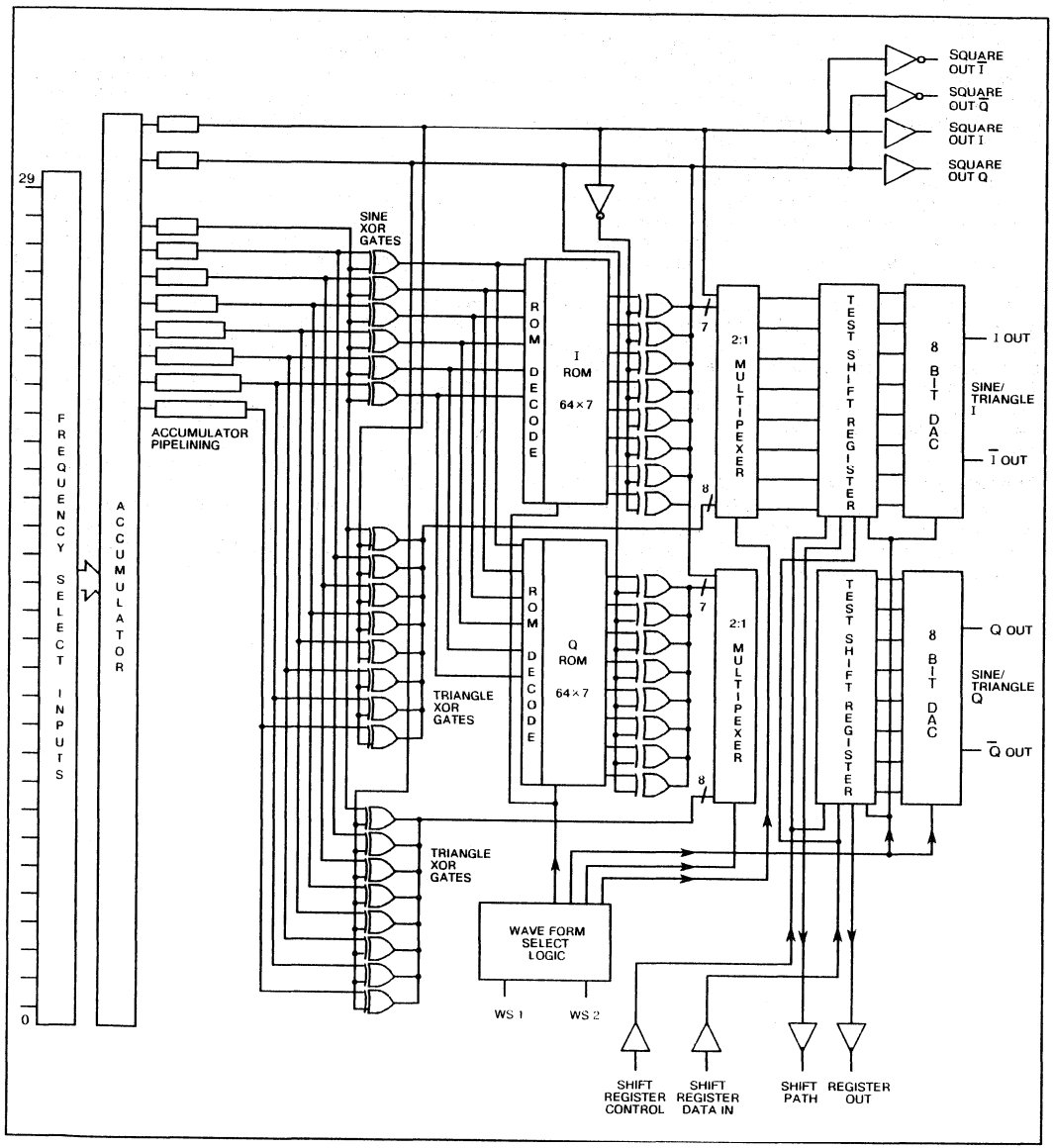


Fig.1 Simplified Block Diagram of SP2002

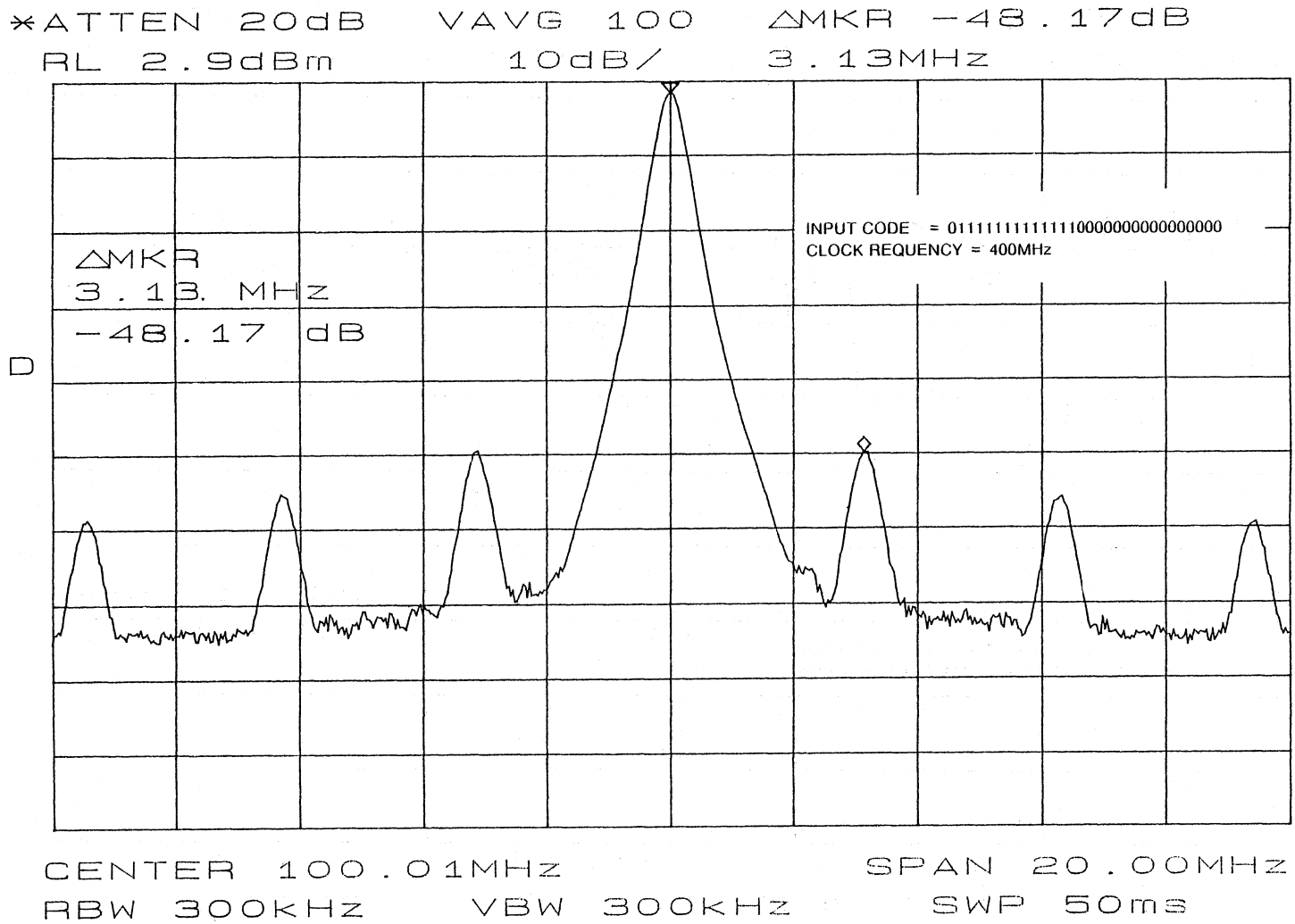

*ATTEN 20dB
VAVG 100
ΔMKR −48.17dB
RL 2.9dBm
10dB/
3.13MHz
ΔMKR
3.13. MHz
−48.17 dB
INPUT CODE = 01111111111111000000000000000
CLOCK REQUENCY = 400MHz
CENTER 100.01MHz
SPAN 20.00MHz
RBW 300KHz
VBW 300KHz
SWP 50ms

Fig. 2a

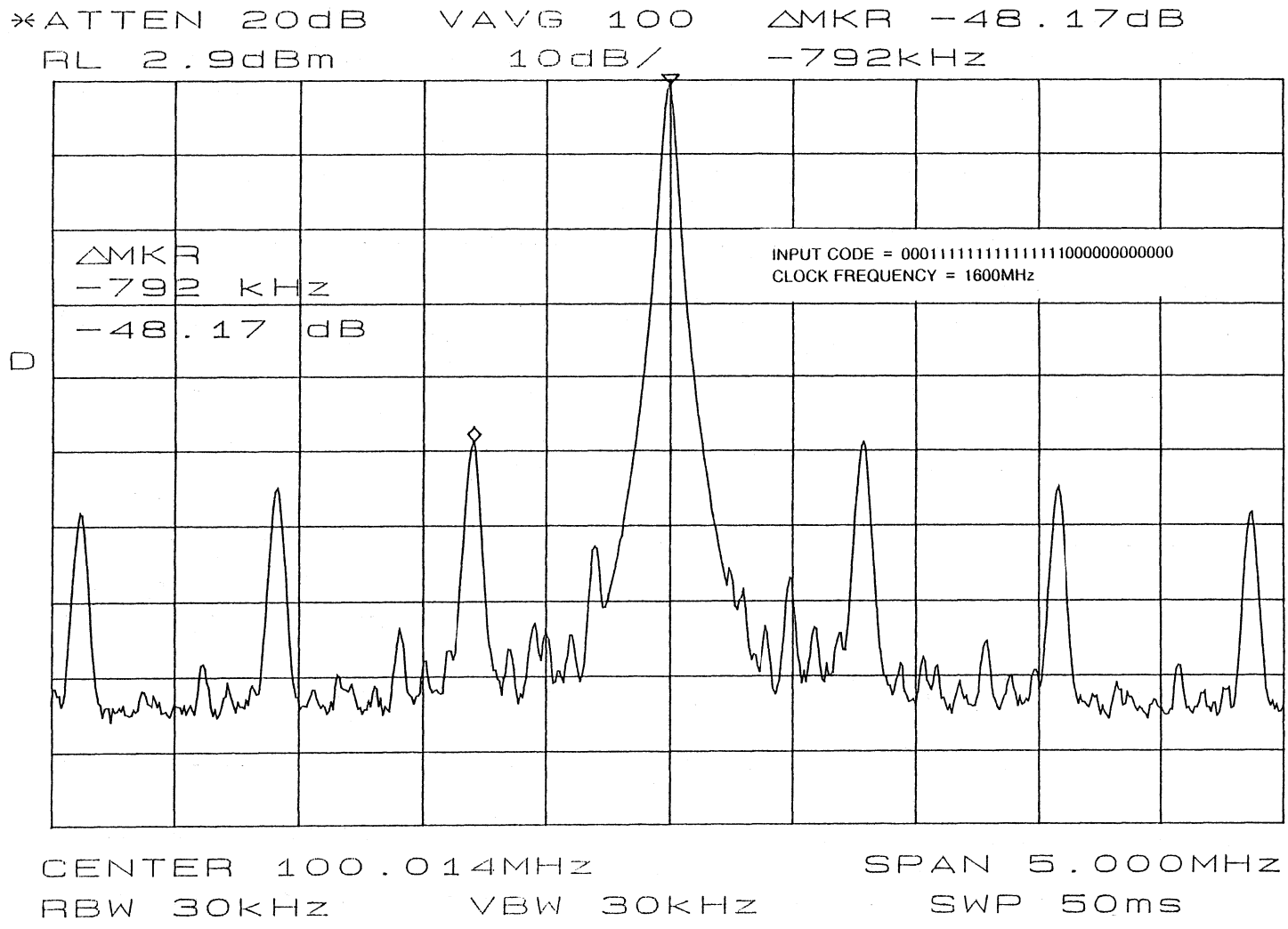

*ATTEN 20dB
VAVG 100
ΔMKR −48.17dB
RL 2.9dBm
10dB/
−792kHz
ΔMKR
−792 kHz
−48.17 dB
INPUT CODE = 00011111111111111111000000000000
CLOCK FREQUENCY = 1600MHz
D
CENTER 100.014MHz
SPAN 5.000MHz
RBW 30kHz
VBW 30kHz
SWP 50ms

Fig. 2b

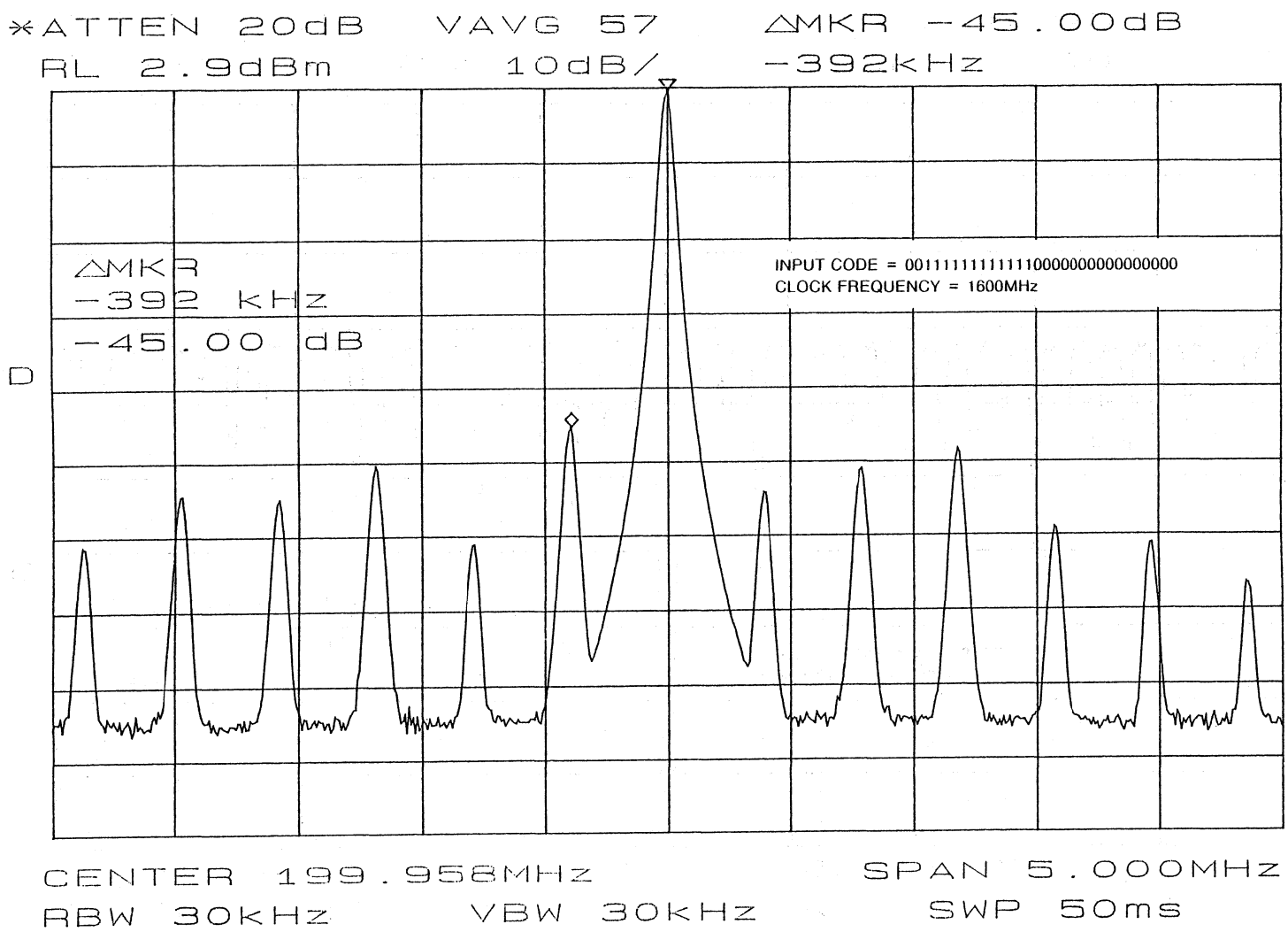

*ATTEN 20dB
VAVG 57
ΔMKR -45.00dB
RL 2.9dBm
10dB/
-392kHz
ΔMKR
-392 kHz
-45.00 dB
INPUT CODE = 00111111111111000000000000000
CLOCK FREQUENCY = 1600MHz
D
CENTER 199.958MHz
SPAN 5.000MHz
RBW 30kHz
VBW 30kHz
SWP 50ms

Fig. 3a

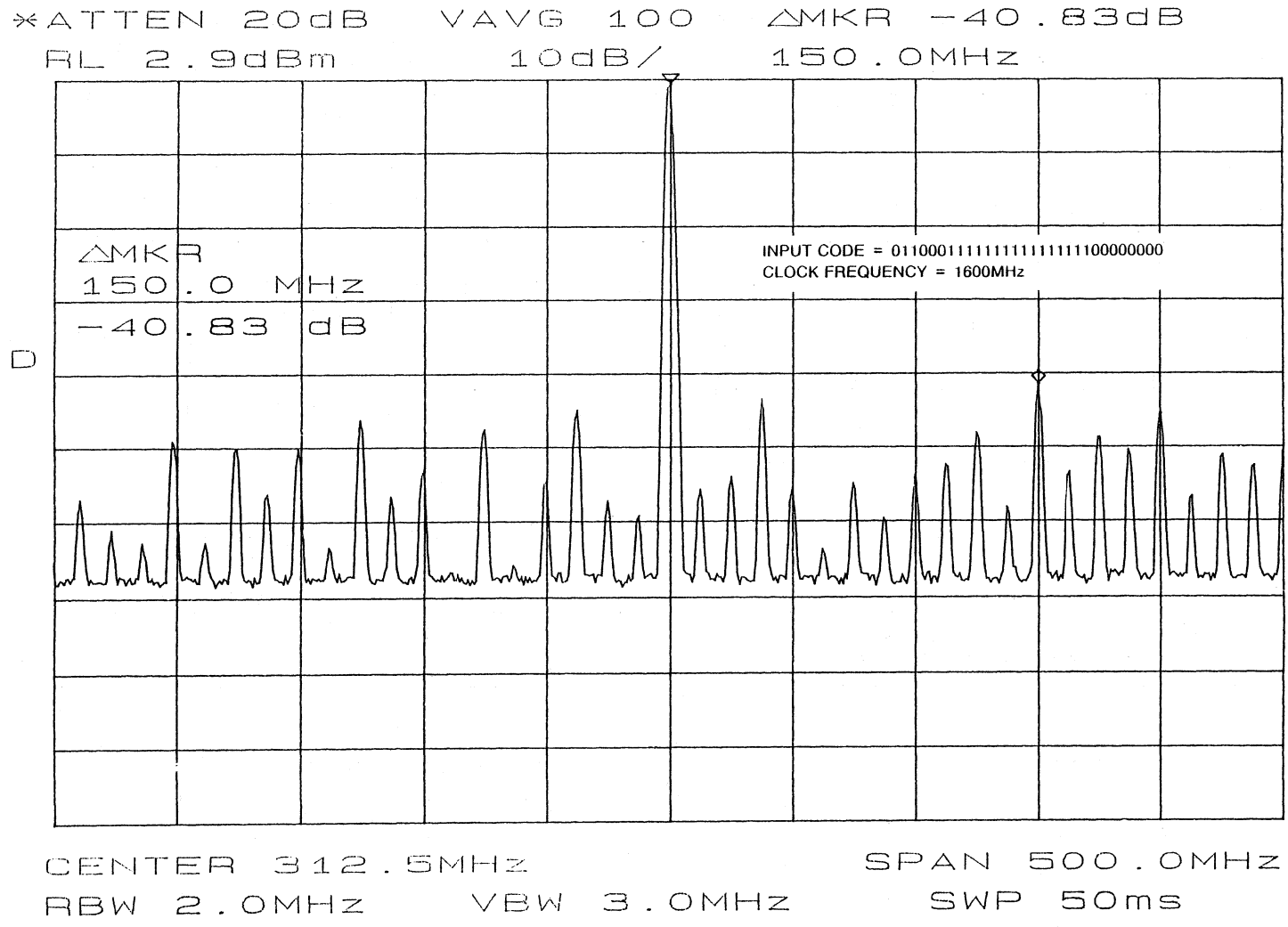

*ATTEN 20dB
VAVG 100
ΔMKR −40.83dB
RL 2.9dBm
10dB/
150.0MHz
ΔMKR
150.0 MHz
−40.83 dB
INPUT CODE = 01100011111111111111100000000
CLOCK FREQUENCY = 1600MHz
CENTER 312.5MHz
SPAN 500.0MHz
RBW 2.0MHz
VBW 3.0MHz
SWP 50ms

Fig. 3b

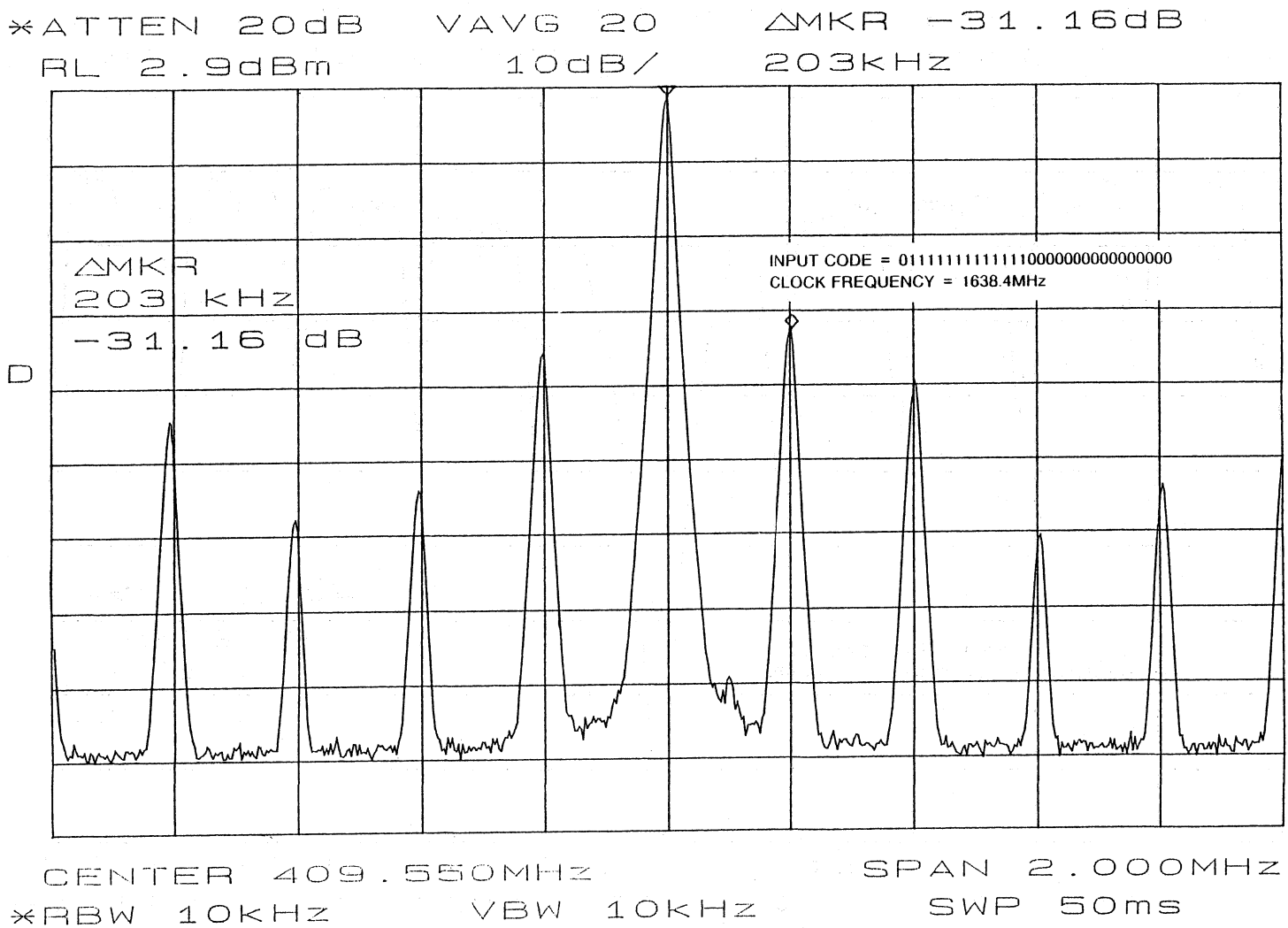

*ATTEN 20dB
VAVG 20
ΔMKR −31.16dB
RL 2.9dBm
10dB/
203kHz
ΔMKR
203 kHz
−31.16 dB
D
INPUT CODE = 01111111111111000000000000000
CLOCK FREQUENCY = 1638.4MHz
CENTER 409.550MHz
SPAN 2.000MHz
*RBW 10kHz
VBW 10kHz
SWP 50ms

Fig. 3c

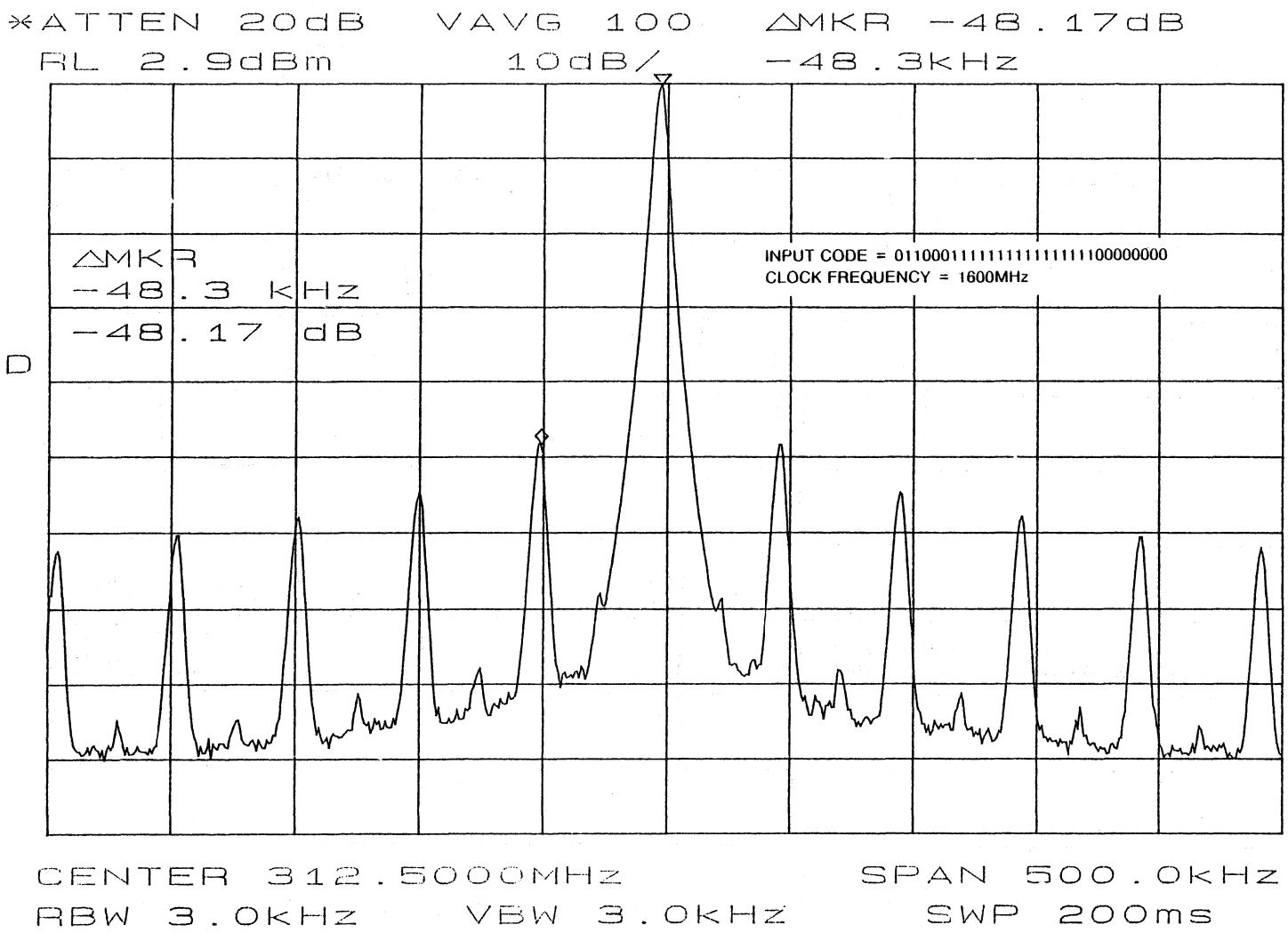

*ATTEN 20dB
VAVG 100
ΔMKR −48.17dB
RL 2.9dBm
10dB/
−48.3kHz
ΔMKR
−48.3 kHz
−48.17 dB
D
INPUT CODE = 01100011111111111111111100000000
CLOCK FREQUENCY = 1600MHz
CENTER 312.500MHz
SPAN 500.0kHz
RBW 3.0kHz
VBW 3.0kHz
SWP 200ms

Fig. 4

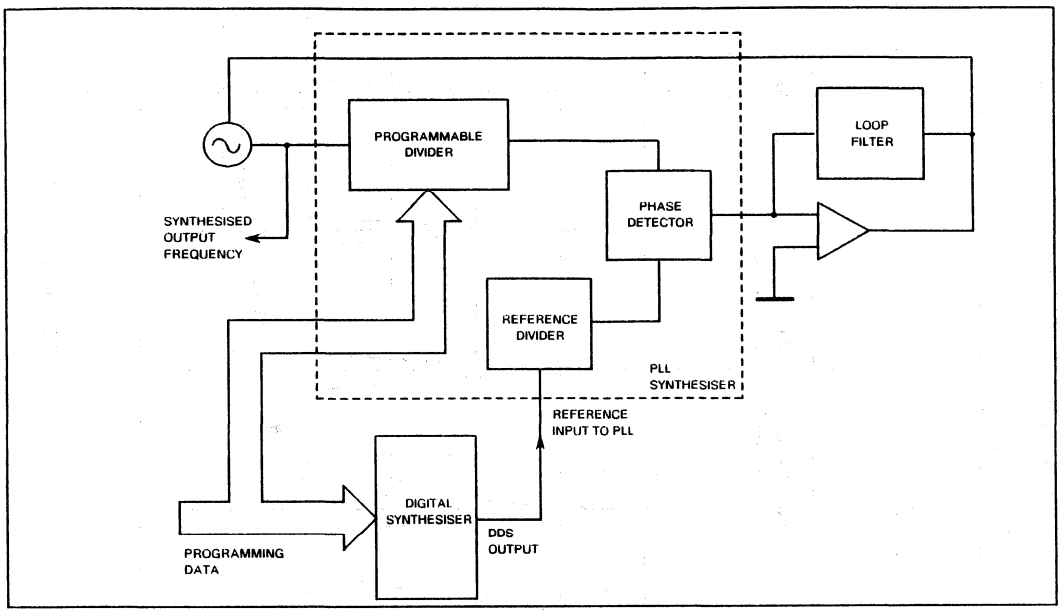


Fig.5 Hybrid PLL/Direct Digital Synthesiser

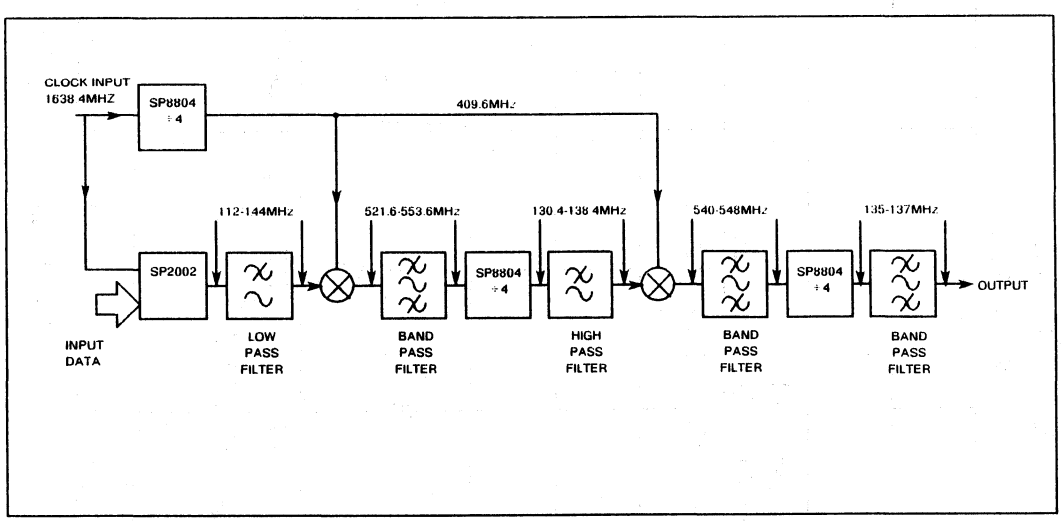


Fig.6 Experimental Mix up and Divide Spur Reduction System Block Diagram

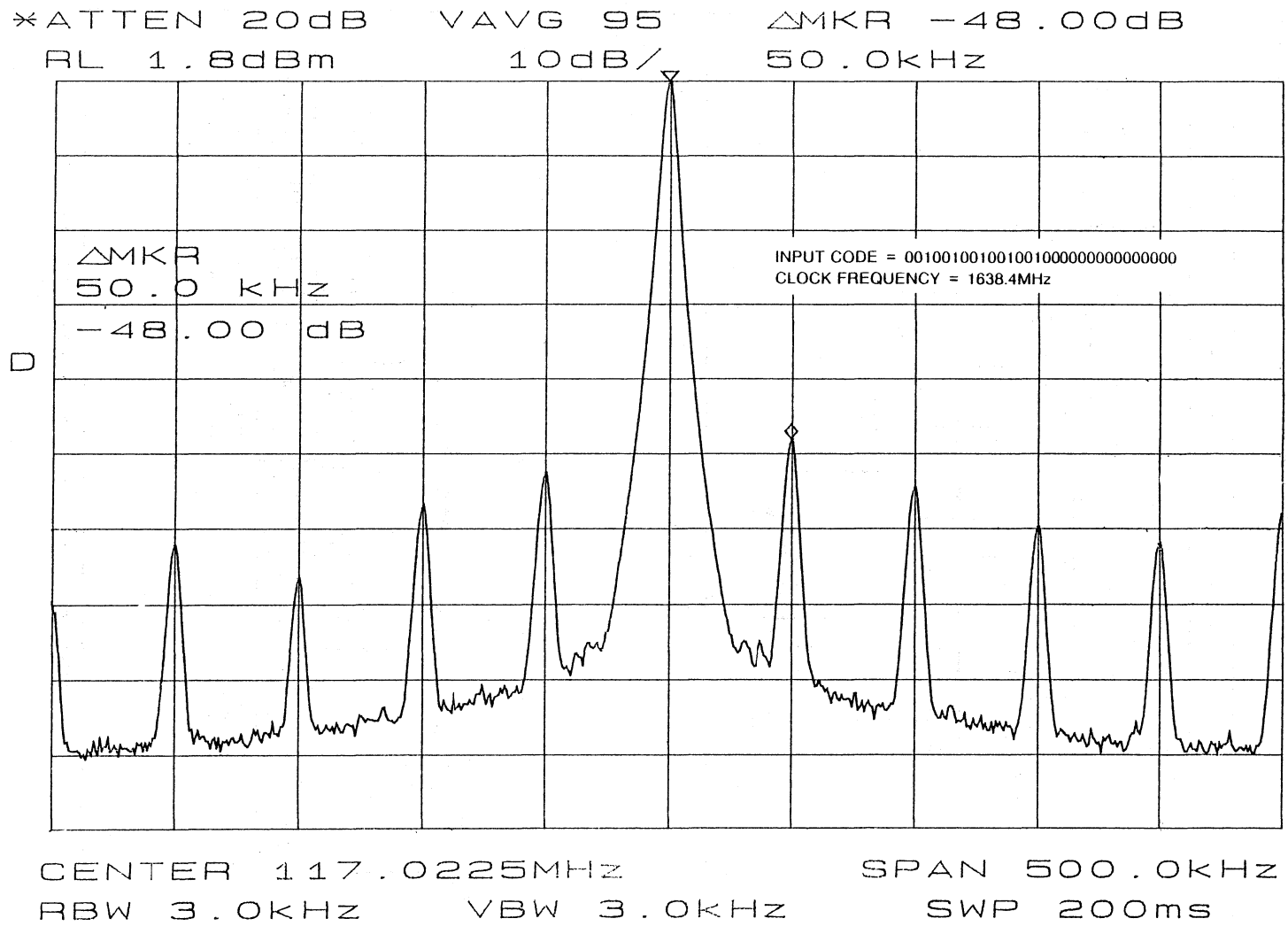

*ATTEN 20dB
VAVG 95
ΔMKR −48.00dB
RL 1.8dBm
10dB/
50.0kHz
ΔMKR
50.0 kHz
−48.00 dB
INPUT CODE = 00100100100100100000000000000000
CLOCK FREQUENCY = 1638.4MHz
CENTER 117.0225MHz
SPAN 500.0kHz
RBW 3.0kHz
VBW 3.0kHz
SWP 200ms

Fig. 7a

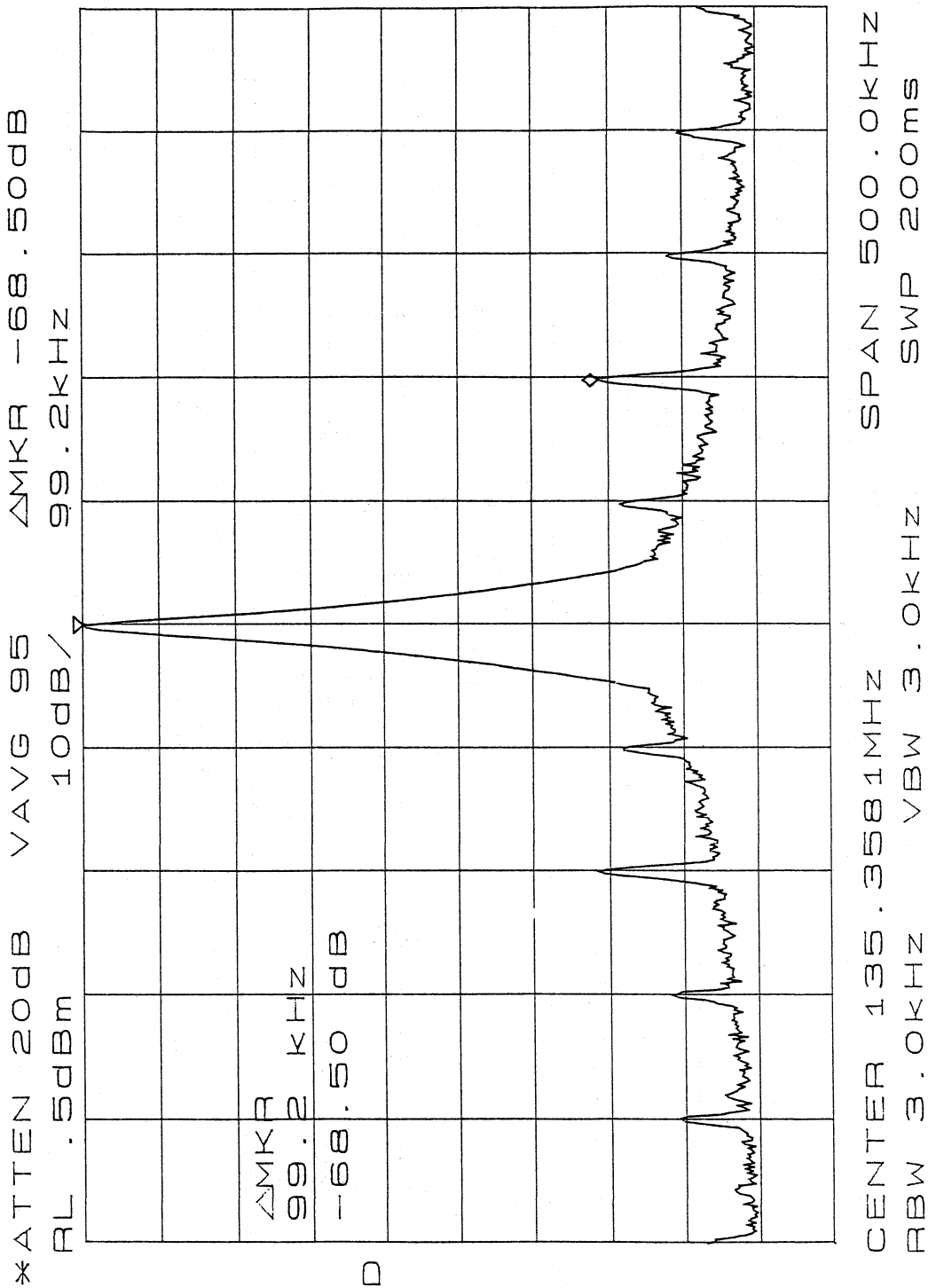


Fig. 7b Output from spur reduction system

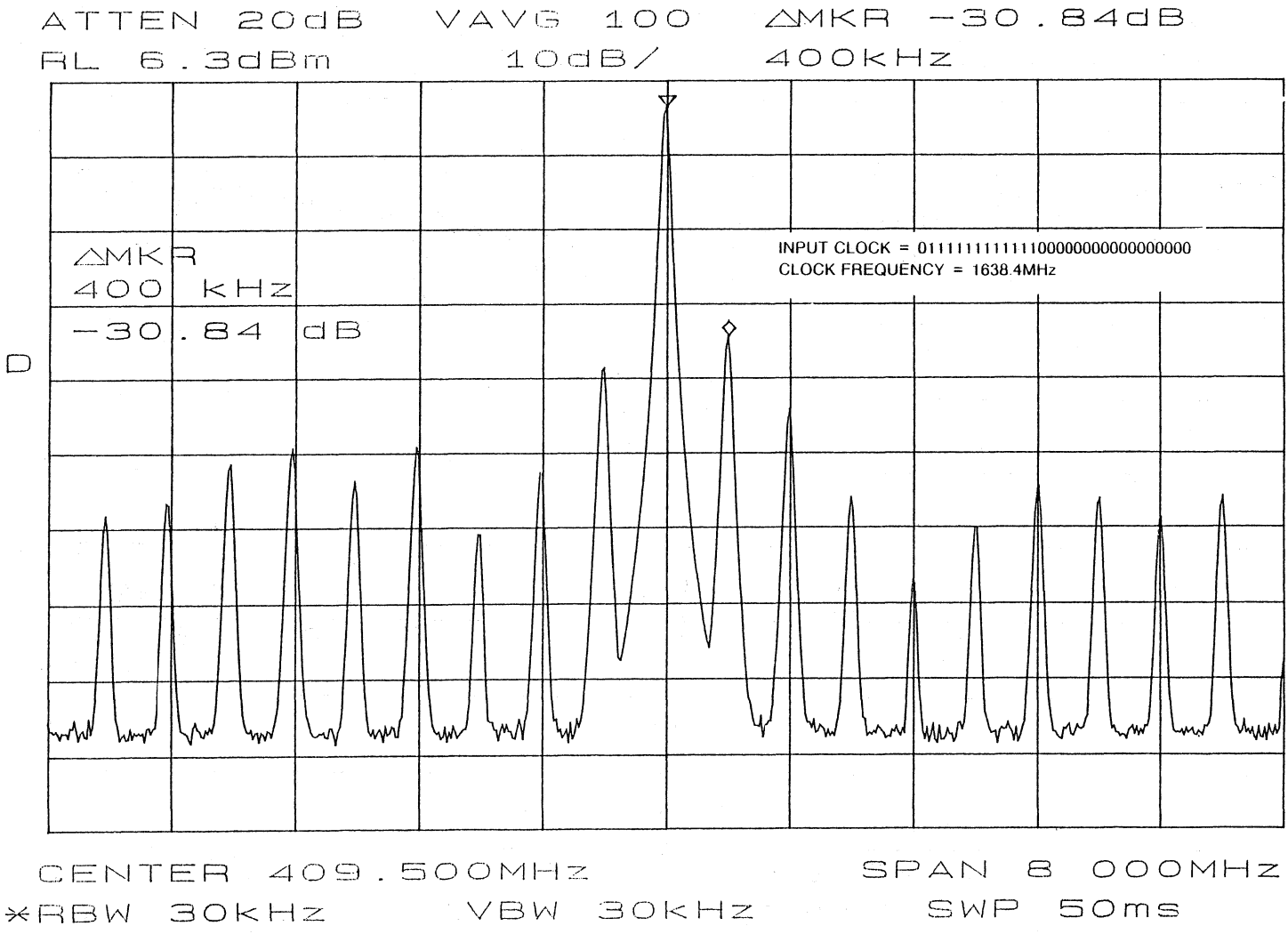

ATTEN 20dB
VAVG 100
ΔMKR −30.84dB
RL 6.3dBm
10dB/
400kHz
ΔMKR
400 kHz
−30.84 dB
D
INPUT CLOCK = 01111111111110000000000000000
CLOCK FREQUENCY = 1638.4MHz
CENTER 409.500MHz
SPAN 8 000MHz
*RBW 30kHz
VBW 30kHz
SWP 50ms

Fig. 8

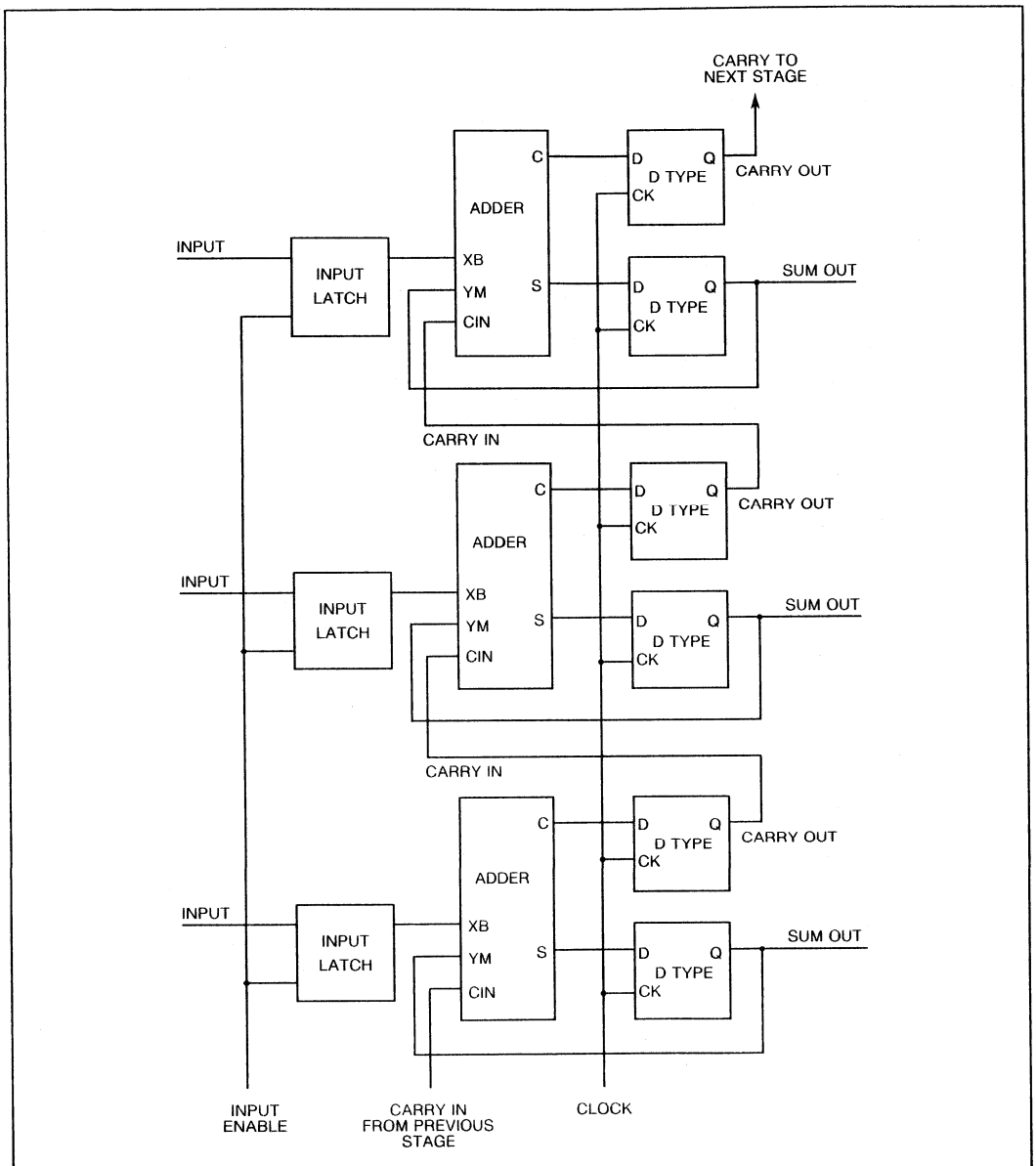


Fig. 9 Organisation of Pipelined Accumulator

Section 5

MIL-STD-883 Class B

GEC Plessey Semiconductors is in conformance with the requirements of MIL-STD-883 Notice 11 paragraph 1.2.1 and can supply product requiring the use of this standard.

Approval has been issued by DGNQA against DEF-STD 05-21 (equivalent to AQAP1) and by NSI to BS9000. A number of detailed device approvals to BS9300 and BS9400 have been granted.

The following pages detail the manufacturing procedures required to conform to MIL-STD-883 Class B.

GEC PLESSEY
SEMICONDUCTORS

Screening procedures

MIL-STD-883 Class B

Stage/Operation	MIL-STD-883 Methods and Comments
Wafer processing	GPS process
Circuit probe test	To GPS probe test spec.
Chip separation	GPS process
Chip inspection and selection	Method 2010 condition B
Chip bond and inspect	GPS process
Wire bond and inspect	GPS process
Internal visual	Method 2010 condition B
Customer source inspection	Optional extra
Encapsulation	GPS process
Temperature cycling	Method 1010 condition C
Constant acceleration	Method 2001 condition E, Y1 only
Seal test	Method 1014
Visual inspection	For catastrophics, as Method 5004
Interim electrical test	To device spec. with read and record, as Method A
Burn-in test	Method 1015, 168 hours at 125°C
Post burn-in electrical	As interim electrical, as Method 5004
PDA calculations	Subgroup 1 min. 5% max.
Final electrical test	100% subgroups 1, 2, 3, 4, 5, 6, 7, 8, 9,10 and 11, as device spec. and Method 5004
Code	As device spec
Seal test	Method 1014 (as necessary)
External visual	Method 2009
Form inspection lot	As MIL-M-38510
Select samples for conformance test	As Method 5005
Group A tests	Subgroups 1, 2, 3, 4, 5, 6, 7, 8, 9,10 and 11, as device spec. and Method 5005
Group B tests	Subgroups 2, 3 and 5 (devices classified as static sensitive) as device spec. and Method 5005
Group C tests	Subgroup 1 as per device spec. and Method 5005 (generic data may be used if available)
Group D tests as device spec. and Method 5005	Subgroups 1, 2, 3, 4, 5, 6, 7, and 8 (generic data may be used if available)
Prepare data package	
Inspect devices, pack and ship with data and C of C	As required

Conformance testing

MIL-STD-883 Class B Method 5005.11
Group A Electrical Tests

Subgroup	MIL-STD-883 Methods and Comments	LTPD	Sample Size
1	Static tests at +25°C	2	116
2	Static tests at maximum rated operating temperature	2	116
3	Static tests at minimum rated operating temperature	2	116
4	Dynamic tests at +25°C	2	116
5	Dynamic tests at maximum rated operating temperature	2	116
6	Dynamic tests at minimum rated operating temperature	2	116
7	Functional tests at +25°C	2	116
8	Functional tests at max. and min. operating temperatures	2	116
9	Switching tests at +25°C	2	116
10	Switching tests at maximum rated operating temperature	2	116
11	Switching tests at minimum rated operating temperature	2	116

All non-destructive. Performed on each inspection lot as per MIL-M-38510 3.1.3.8

MIL-STD-883 Class B Group B Electrical Tests

Subgroup	Test	Method	Sample Size	Destructive/ Non-desctrucive
2	(a) Resistance to solvents	2015	4	D
3	(b) Solderability	2022 or 2003	3	D
5	(a) Bond strength	2011	4	D

Performed on each inspection lot as per MIL-M-38510 3.1.3.8

MIL-STD-883 Class B Group C Electrical Tests

Subgroup	Test	Method	Sample Size	Destructive/ Non-desctrucive
1	(a) Steady state life test (b) End point electrical parameters	1005	45	ND

Generic test data may be used for Group C tests

MIL-STD-883 Notice 4 Page 3 Clause 17

'... Group C and D shall have been completed on date codes within 52 weeks **prior** to the date code of product being submitted for acceptance. Group C data shall be on a die in the same microcircuit **group**...with the same **material, design** and **process** and from the same **plant** as the die represented.'

MIL-STD-38510F Page 5 Clause 3.1.3.13

'Microcircuit group. Microcircuits which are designed to perform the same type of basic **circuit function**...within a given **circuit technology** (e.g. ...ECL...Linear, Hybrid, MOS) which are designed for the same supply, bias and signal voltages and for input/output compatibility and which are fabricated by use of the same basic **die construction and metallization**; the same **die attach** method; and by use of bonding interconnects of the same size, material and attachment method.'

Conformance testing (continued)

MIL-STD-883 Class B Group D Electrical Tests

Subgroup	Test	Method	Sample Size	Destructive/ Non-desctrucive
1	(a) Physical dimensions	2016	15	ND
2	(a) Lead integrity (b) Seal (1) Fine (2) Gross	2010 1014	15 15	D D
3	(a) Thermal shock (b) Temperature cycling (c) Moisture resistance (d) Seal (1) Fine (2) Gross (e) Visual examination (f) End point electrical parameters	1011 1010 1004 1014	15	D
4	(a) Mechanical shock (b) Vibration, variable frequency (c) Constant acceleration (d) Seal (1) Fine (2) Gross (e) Visual examination (f) End point electrical parameters	2002 2007 2001 1014	15	D
5	(a) Salt atmosphere (b) Seal (1) Fine (2) Gross (c) Visual examination	1009 1014	15	D
6	(a) Internal water vapour content	1018	5	D
7	(a) Adhesion of lead finish	2025	15	D
8	(a) Lid torque	2024	5	D

Generic test data may be used for Group D tests

MIL-STD-883 Notice 4 Page 3 Clause 17

'... Group C and D shall have been completed on date codes within 52 weeks **prior** to the date code of product being submitted for acceptance. Group D data shall be on the same package type...and from the same **plant** as the die represented.'

MIL-STD-38510F Page 5 Clause 3.1.3.12

'Package type. A package type is a package which has the same **case outline, configuration**...(the physical shape of the case outline not including dimensions)..., **materials** (including bonding wire and die attach), **piece parts** (excluding preforms which differ only in size), and **assembly processes**.'

Packaging and coding

Lead finish

Devices will be supplied with the following lead finishes as standard:

Package Type	Lead Finish (MIL-M-38510 3.5.6.3.2)
Metal Can (CM)	Gold plate over Nickel plate
Sidebrazed Ceramic DIL (DC)	
Leadless Chip Carrier (LC)	
Ceramic DIL (DG)	Hot slder dip over Tin plate

ESD protection

GEC Plessey Semiconductors considers all devices to be sensitive to electrostatic discharge to varying degrees (but at least to category A). All units are therefore marked with the equilateral triangle ESD sensitivity indicator.

In addition, all devices are packaged and shipped in conductive material or packaged in anti-static material with an external field shielding barrier in accordance to MIL-M-38510.

Device marking

All devices are marked with the following coding:

1. GPS logo or 'GPS' (manufacturer's identity).
2. ESD sensitivity indicator (equilateral triangle).
3. Date code (per MIL-M-38510).
4. Assembley lot identifier. Suffix letter added to date code indicating lot identity within production week.
5. Device type number - 'AC' indicating a MIL-STD-883 Class B compliant device.
6. Process/Assembly site identifier (two-letter code). Initial letter 'S' indicates GPS Swindon UK Wafer Process site. Second letter 'J' indicates GPS Swindon assembly site.
7. Pin 1 identifier. This may be either a package notch or dot for dual-in-line packages, gold corner for leadless chip carriers or tab for metal can packages.

Section 6
Package Outlines

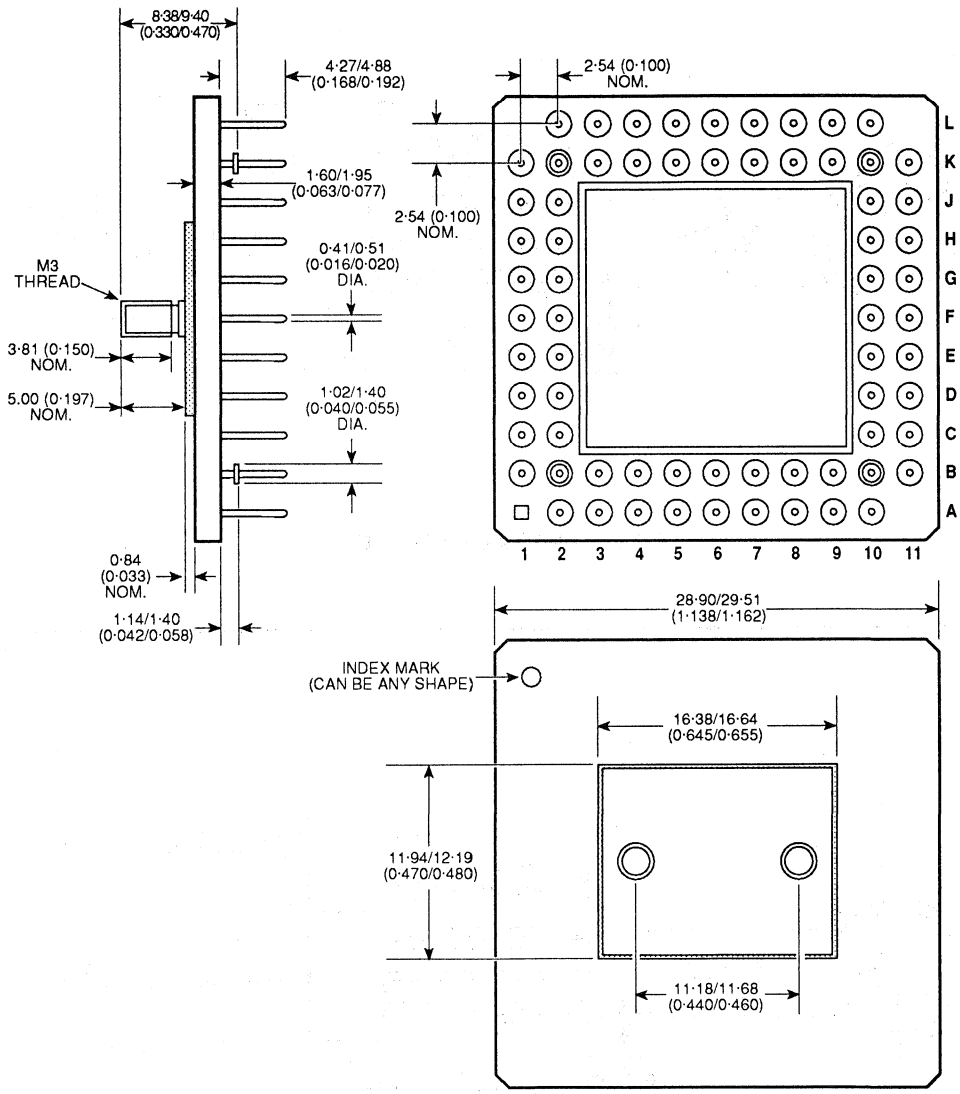
Dimensions are shown thus: mm (in).
For further package information, please contact your local Customer Service Centre.

GEC PLESSEY
SEMICONDUCTORS

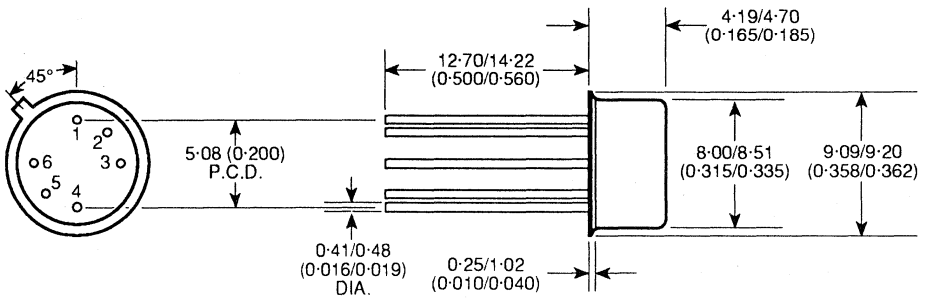
Package Codes

Package codes for the integrated circuits detailed in this handbook are given below. Dimensioned outline drawings are given in Section 6.

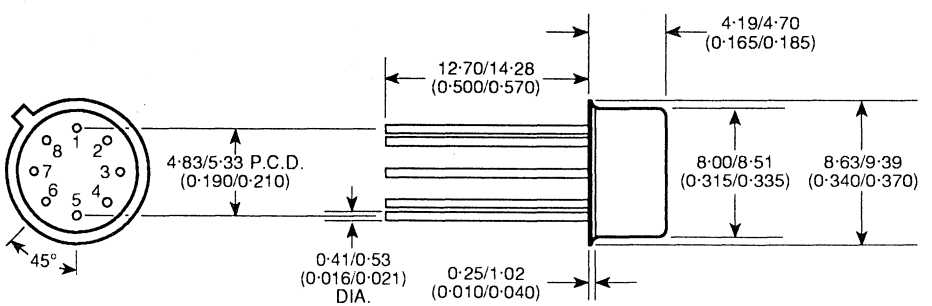
Code	Type	Description
AC	PGA	Pin Grid Array, multi-layer ceramic, metal sealed lid, through board.
CM	TO-n	Cylindrical multi-lead metal can.
DC	DILMON	Dual-in-line, multi-layer ceramic, sidebrazed leads, metal sealed lid, through board.
DG	CERDIP	Dual-in-line, ceramic body, Alloy 42 leadframe, glass sealed, through board.
DP	PLASDIP	Dual-in-line, Copper or Alloy 42 leadframe, plastic moulded, through board.
HG	Quad Cerpack	Glass sealed ceramic chip carrier, J-formed leads on four sides, surface mount.
HP	PLCC	Plastic moulded chip carrier, J-formed leads on four sides, surface mount.
LC	Leadless Chip Carrier	Four sided, leadless, multi-layer ceramic, metal sealed lid, surface mount.
MC	Small Outline	Dual-in-line, multi-layer ceramic, brazed 'Gullwing' formed leads, metal sealed lid, surface mount.
MP	Small Outline	Dual-in-line, plastic moulded, 'Gullwing' formed leads, metal sealed lid, surface mount.



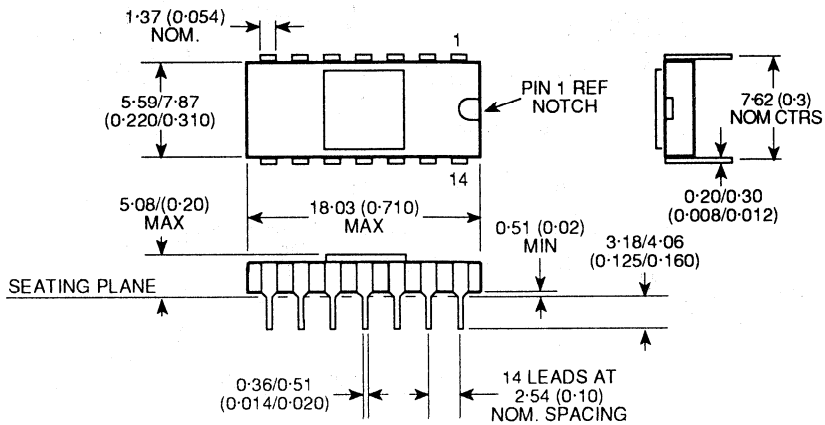
68-PIN GRID ARRAY - AC68 (POWER)



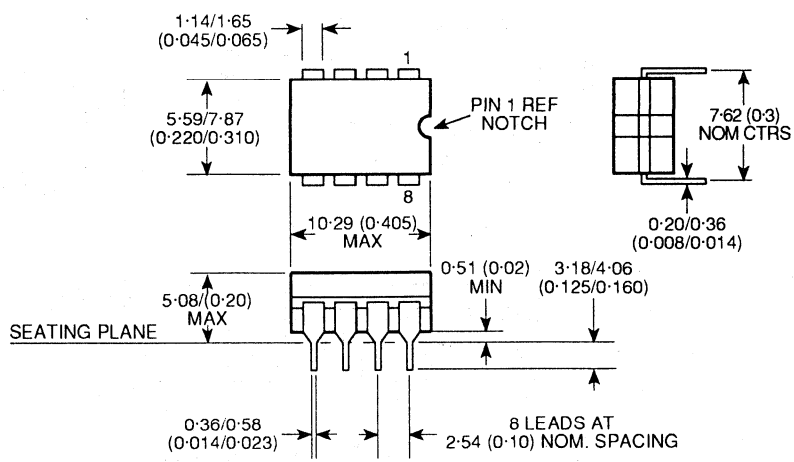
6-LEAD METAL CAN - CM6



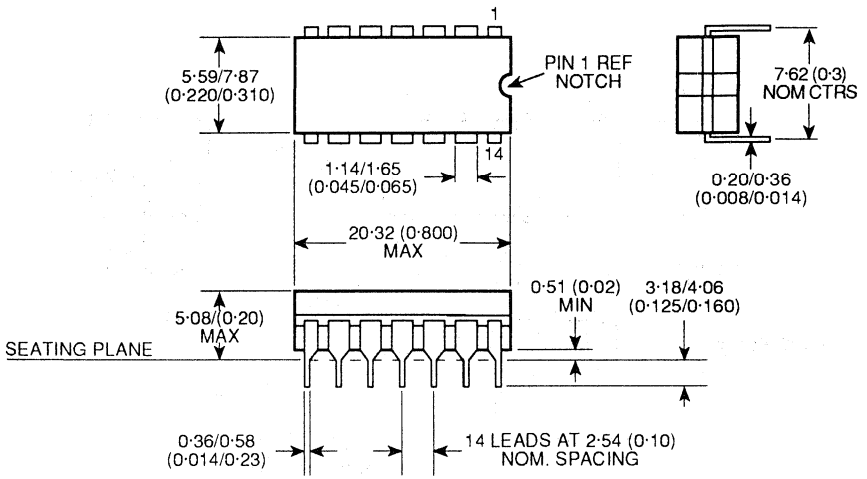
8-LEAD METAL CAN - CM8



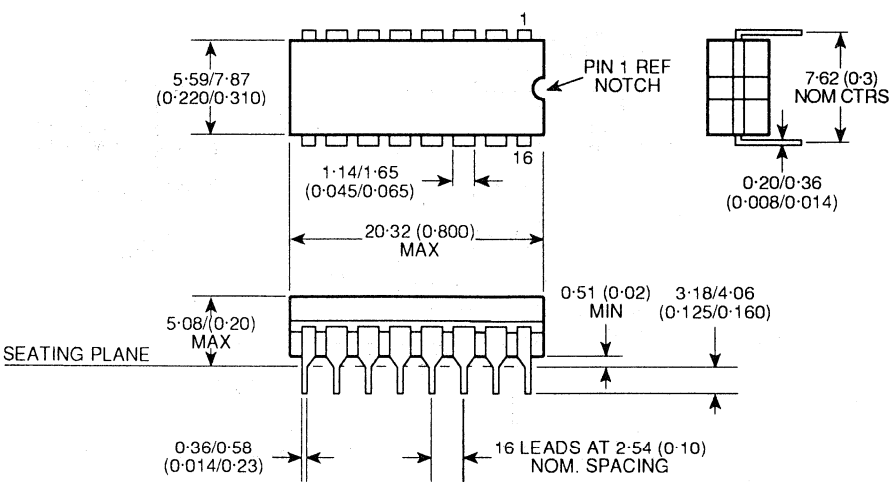
14-LEAD SIDEBRAZED CERAMIC DIL - DC14



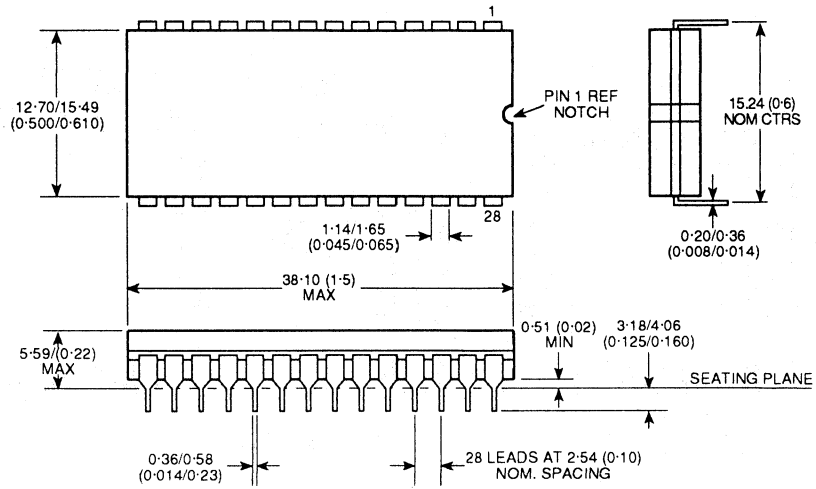
8-LEAD CERAMIC DIL - DG8



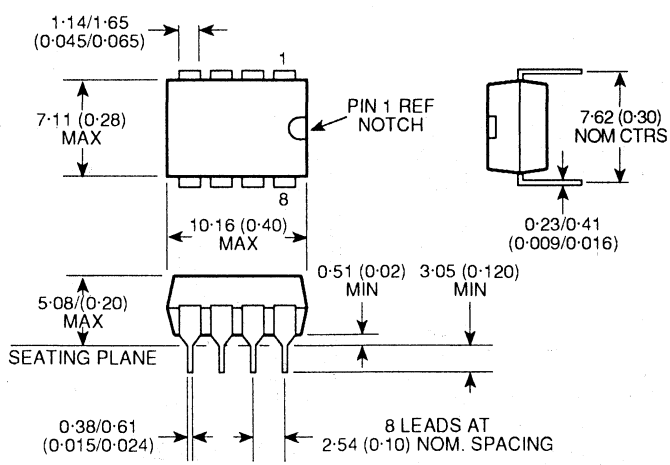
14-LEAD CERAMIC DIL - DG14



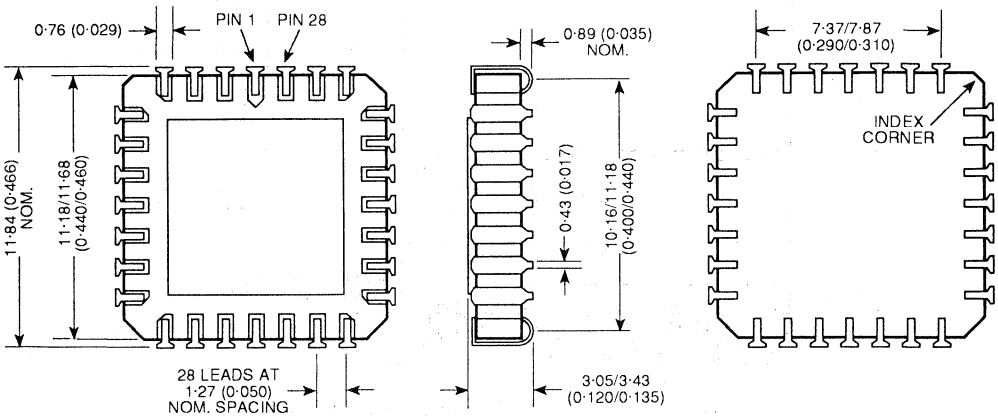
16-LEAD CERAMIC DIL - DG16



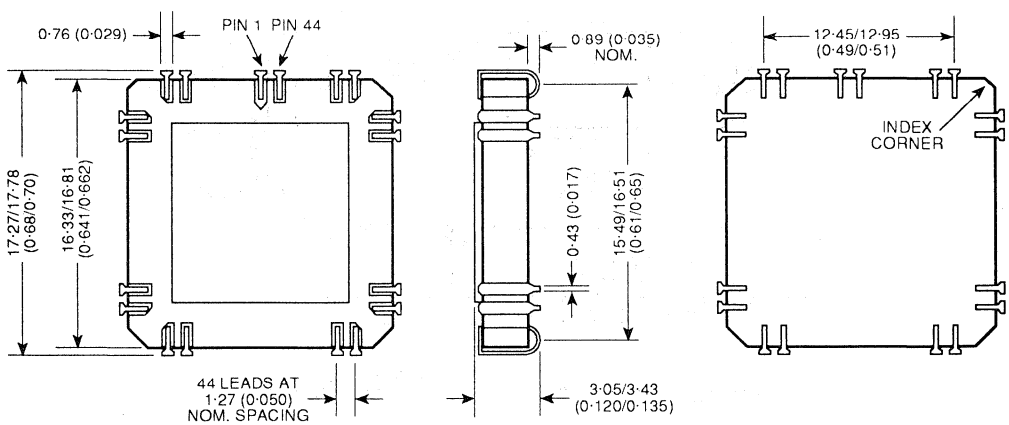
28-LEAD CERAMIC DIL - DG28



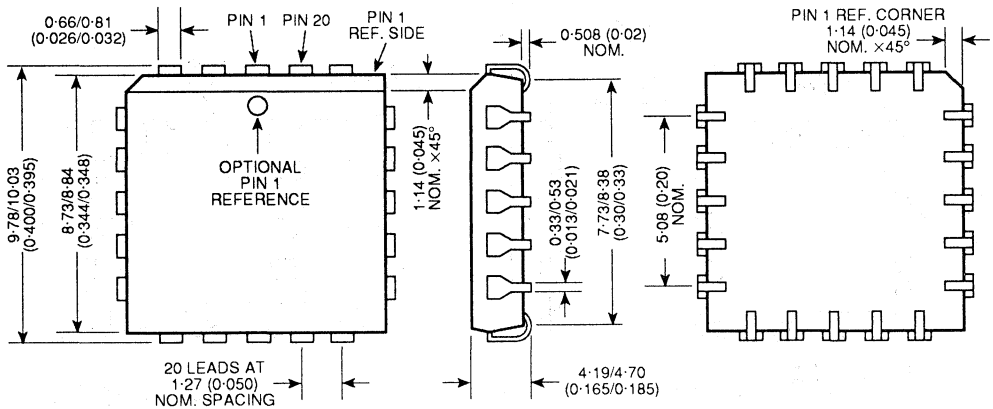
8-LEAD PLASTIC DIL - DP8



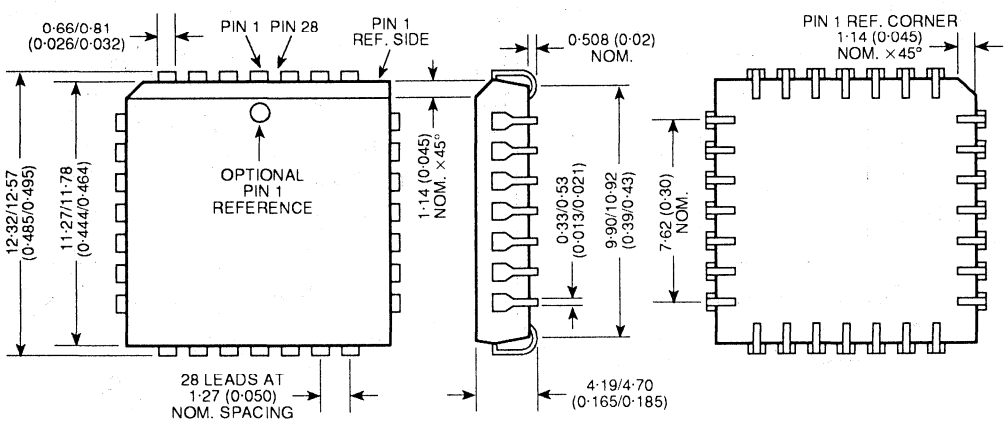
28-PIN LEADED CHIP CARRIER - HC28



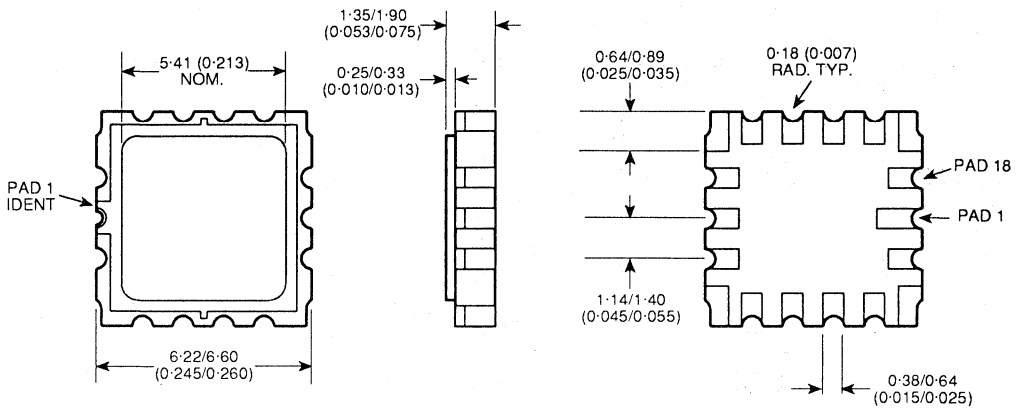
44-PIN LEADED CHIP CARRIER - HC44



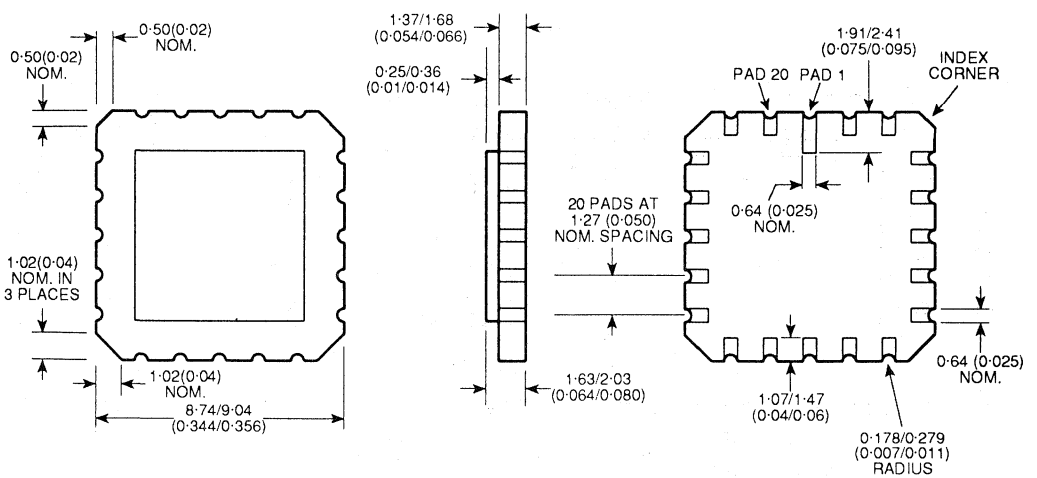
20-LEAD QUAD PLASTIC J LEAD - HP20



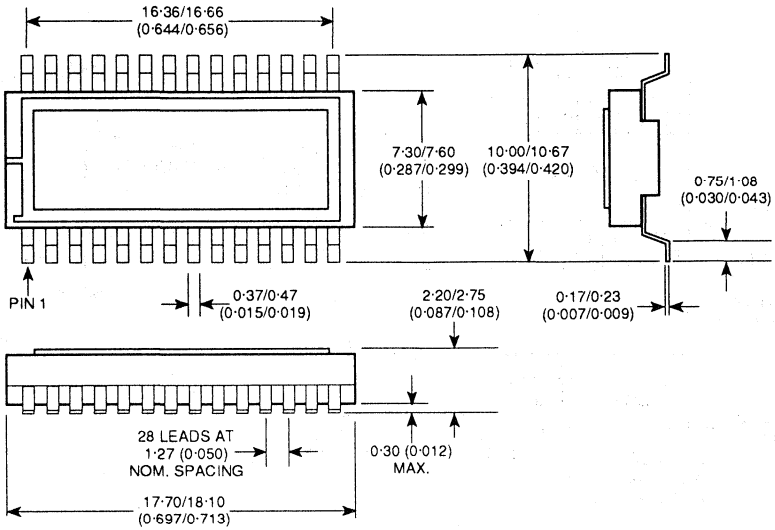
28-LEAD QUAD PLASTIC J LEAD - HP28



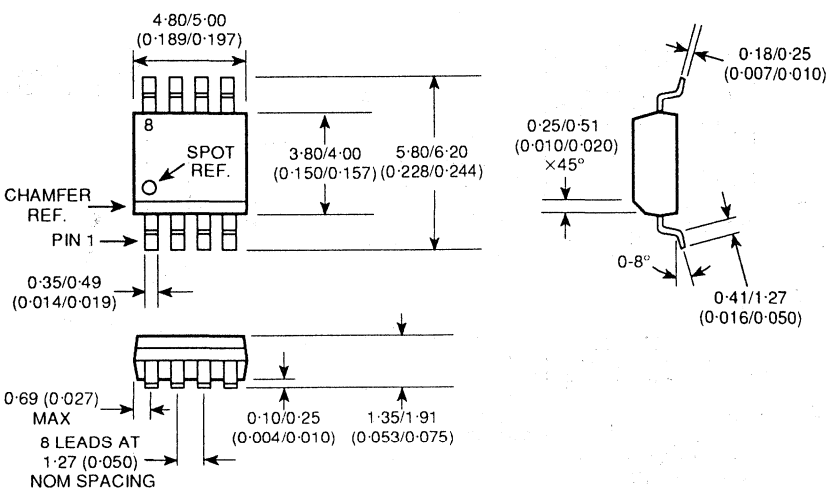
18-PIN LEADLESS CHIP CARRIER - LC18
(HERMETIC)



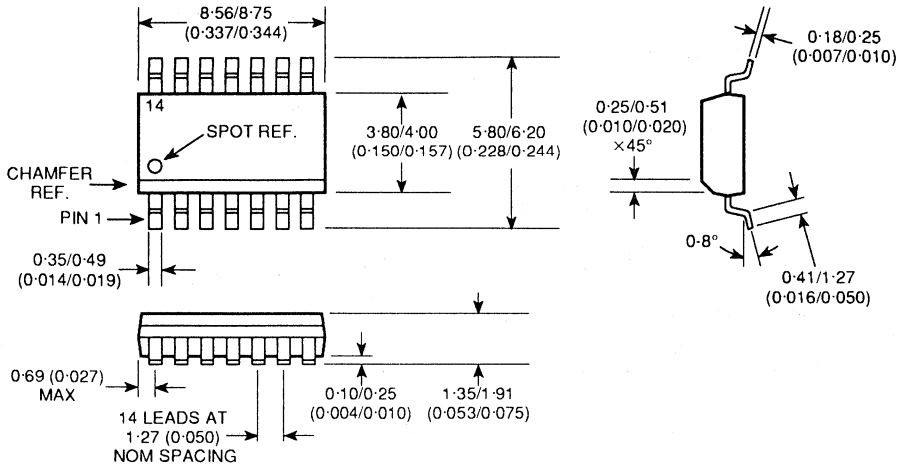
20-PIN LEADLESS CHIP CARRIER - LC20
(HERMETIC)



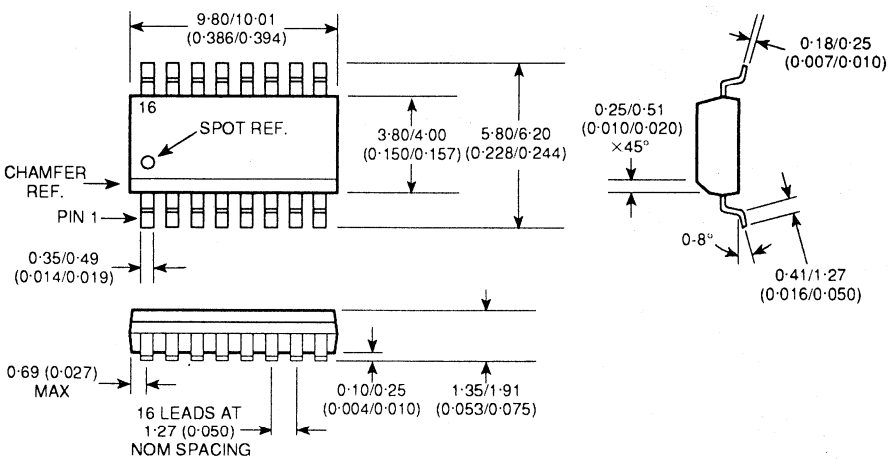
28-LEAD MINIATURE CERAMIC DIL - MC28



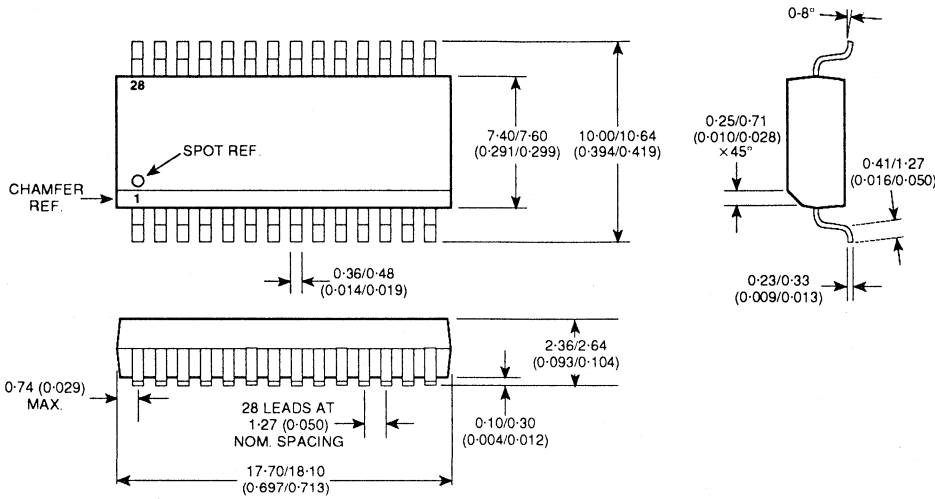
8-LEAD MINIATURE PLASTIC DIL - MP8



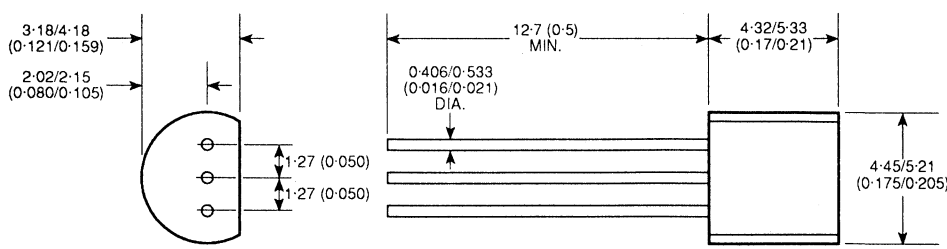
14-LEAD MINIATURE PLASTIC DIL - MP14



16-LEAD MINIATURE PLASTIC DIL - MP16



28-LEAD MINIATURE PLASTIC DIL - MP28



3 LEAD PLASTIC - TO-92

Section 7
GPS Locations

GEC PLESSEY
SEMICONDUCTORS

Headquarters Operations

UNITED KINGDOM	Cheney Manor, Swindon, Wiltshire, United Kingdom, SN2 2QW. Tel: (0793) 518000 Fax: 0793 518411
NORTH AMERICA	P O Box 660017, 1500 Green Hills Road, Scotts Valley, California 95067-0017, USA. Tel:(408) 438 2900 Fax: (408) 438 5576

Customer Service Centres

FRANCE & BENELUX	Z.A. Courtaboeuf, Miniparc-6, Avenue des Andes, Bat. 2-BP 142, 91944, Les Ulis Cedex A. France.Tel: (1) 64 46 23 45. Fax: (1) 64 46 06 07
GERMANY, AUSTRIA and SWITZERLAND	Ungererstraße 129, 80805 Munchen 40, Germany. Tel: 089/36 0906-0. Fax: 089/36 0906-55
ITALY	Via Raffaello Sanzio, 4, 20092 Cinisello Balsamo (MILAN). Tel: (02) 66040867. Fax: (02) 66040993.
JAPAN	CTS Kojimachi Building (4th Floor), 2-12, Kojimachi, Chiyoda-ku, Tokyo 102. Tel: (03) 5276-5501. Fax: (03) 5276-5510.
NORTH AMERICA	P O Box 660017, 1500 Green Hills Road, Scotts Valley, California 95067-0017, USA. Tel: (408) 438 2900. Fax: (408) 438 7023
SOUTH EAST ASIA	No. 3 Tai Seng Drive, GEC Building, Singapore 1953. Tel: (65) 3827708. Fax: (65) 3828872
SWEDEN	Katarina Bangata 79, 116 42 Stockholm. Tel: 46 8 7029770. Fax: 46 8 6404736
TAIWAN, ROC	Room 503, 5F, 131 Min-Sheng E Road, Sec 3, Taipei. Tel: 886 2 5461260. Fax: 886 2 7190260
UK, EIRE, DENMARK, FINLAND and NORWAY	Unit 1,Crompton Road,Groundwell Industrial Estate, Swindon, Wilts, U.K., SN2 5AF. Tel: (0793) 518510. Fax: (0793) 518582. **Power Division** Carholme Road, Lincoln, U.K., LN1 1SG. Tel: (0522) 510500. Fax: (0522) 510550

North American Sales Offices

NATIONAL SALES	P O Box 660017, Scotts Valley, CA 95067-0017. Tel: (408) 438-2900. ITT Telex: 4940840. Fax: (408) 438-5576.
EASTERN	Two Dedham Place, Suite 1, Allied Drive, Boston, MA 02026. Tel: (617) 320-9790. Fax: (617) 320-9383.
WESTERN	1735 Technology Drive, Suite 100, San Jose, California 95110. Tel: (408) 451-4700. Fax: (408) 451-4710.
ARIZONA/NEW MEXICO	4635 South Lakeshore Drive, Tempe, AZ 85282. Tel: (602) 491-0910. Fax: (602) 491-1219.
SOUTH CENTRAL	9330 LBJ Freeway, Ste. 665, Dallas, TX 75243. Tel: (214) 690-4930. Fax: (214) 680-9753.
NORTHWEST	7935 Datura Circle West, Littleton, CO 80120. Tel: (303) 798-0250. Fax: (303) 730-2460.
DIXIE and FLORIDA	668 N. Orlando Ave., Suite 1015 B, Maitland, FL 32751. Tel: (407) 539-1700. Fax: (407) 539-0055. 385 Commerce Way, Longwood, FL 32750. Tel: (407) 339-6660. Fax: (407) 339-9355.
SOUTHWEST	2600 Michelson Drive, Suite 830, Irvine, CA 92715. Tel: (714) 852-3900. Fax: (714) 852-3910.
DISTRIBUTION SALES	1500 Green Hills Road, Scotts Valley, CA 95066. Tel: (408) 438-2900. ITT Telex: 4940840. Fax: (408) 438-7023.
CANADA	3608 Boul. St. Charles, Suite 9, Kirkland, Quebec, H9H 3C3. Tel: (514) 697-0095. Fax: (514) 694-7006.

Semi-Custom Design Centres

AUSTRALIA	Unit 1, 38 South Street, Rydalmere, NSW 2116, Australia. Tel: 612 638 1888. Fax: 612 638 1798.
FRANCE & BENELUX	Z.A. Courtaboeuf, Miniparc-6, Avenue des Andes, Bat.2-B.P. No.142 91944 Les Ulis Cedex A, France.Tel: (1) 64 46 23 45. Fax: (1) 64 46 06 07.
ITALY	Via Raffaello Sanzio, 4, 20092 Cinisello Balsamo (MILAN). Tel: (02) 66040867. Fax. (02) 66040993.
GERMANY	Ungererstraße 129, D 80805 Munchen 40. Tel: (089) 3609 06 0. Fax: (089) 3609 06 55.
JAPAN	CTS Kojimachi Building (4th Floor), 2-12, Kojimachi, Chiyoda-ku, Tokyo 102. Tel: (03) 5276-5501. Fax: (03) 5276-5510.
N AMERICA: Canada	**Alberta Microelectronics Center,** 3553 31st St., N.W., Calgary, Alberta T2L2K7. Tel: (403) 289-2043. **Microstar Technologies,** 7050 Bramelea Rd., #27A Mississaugo, Ontario L5SITI Canada. Tel: (416) 671-8111
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Colorado, USA	**Analog Solutions,** 5484 White Place, Boulder, CO 80303. Tel: (303) 442-5083.
Illinois, USA	**Frederikssen & Shu Laboratories, Inc.,** 531 West Golf Rd., Arlington Heights, IL 60005. Tel: (312) 956-0710.
UNITED KINGDOM	Cheney Manor, Swindon, Wiltshire SN2 2QW. Tel: (0793) 518000. Fax: (0793) 518411. Tweedale Way, Hollinwood, Oldham, Lancashire OL9 7LA. Tel: 061 682 6844. Fax: 061 688 7898. Doddington Road, Lincoln LN6 3LF. Tel: 0522 500500. Fax : 0522 500550.

North American Representatives

ALABAMA	**Electramark, Inc.,** 500 Wynn Drive, Suite 521, Huntsville, AL 35816. Tel: (205) 830-4400 Fax: (205) 830-4406.
ARIZONA	**Fred Board Associates,** 7353 E, 6th Avenue, Scottsdale, AZ 85251. Tel: (602) 994-9388. Fax: (602) 994-9477.
CALIFORNIA	**Gary Chilcote & Associates,** P.O. Box 1795, 1902 Quite Ranch Road, Fallbrook, CA 92028. Tel: (619) 728 7678.Fax: (619) 728 3738. **Jones & McGeoy,** 5100 Campus Drive, Suite 300, Newport Beach, CA 92660. Tel: (714) 724 8080. Fax: (714) 724 8090.
CONNECTICUT	**Stone Components,** 123 Commerce St., Clinton, CT 06413. Tel: (203) 669-4344. Fax: (203)669-9958.
FLORIDA	**American Micro Sales,** 1325 N. Congress Ave., Ste 204, West Palm Beach, FL 33401. Tel: (407) 689 3860.Fax: (407) 689 3168. **American Micro Sales,** 274 Wilshire Blvd., Ste 241, Casselberry, FL 32707. Tel: (407) 831 2505. Fax: (407) 831 1842. **American Micro Sales,** P.O. Box 399, 1033 Rosetree Lane, Tarpon Springs, FL 34688/9. Tel: (813) 938 3073. Fax: (407) 831 1842.
GEORGIA	**Electramark, Inc.,** 6030-H Unity Drive, Norcross, GA 30071. Tel: (404) 446-7915. Fax: (404) 263 6389
ILLINOIS	**Micro Sales, Inc.,** 901 West Hawthorn Drive, Itasca, IL 60043. Tel: (708) 285-1000. Fax: (708) 285-1008.

INDIANA	**Leslie M. DeVoe,** 4371 E. 82nd St., Suite D, Indianapolis, IN 46250. Tel: (317) 842-3245. Fax: (317) 845-8440.
IOWA	**Lorenz Sales,** 5270 N. Park Place N.E., Cedar Rapids, IA 52402. Tel: (319) 377-4666. Fax: (319) 377-2273.
KANSAS	**Lorenz Sales, Inc.,** 8645 College Blvd., Suite 220, Overland Park, KS 66210. Tel: (913) 469-1312. Fax: (913) 469-1238. **Lorenz Sales, Inc.,** 1530 Maybelle, Wichita, KS 67212. Tel: (316) 721-0500. Fax: (316) 721-0566.
MARYLAND	**Walker Associates,** 1757 Gablehammer Road, Westminster, MD 21157. Tel: (410) 876-9399. Fax: (410) 876-9285. **Walker Associates,** 169 Queen Anne Bridge Road, Mitchellville, MD 20716. Tel: (410) 249-7145.
MASSACHUSETTS	**Stone Components,** 2 Pierce Street. Framingham, MA 01701. Tel: (508) 875-3266. Fax: (508) 875-0537. **Stone Components,** 10 Atwood Road, Newburyport, MA 01950. Tel: (508) 462-1079.
MICHIGAN	**Greiner Associates Inc.,** 15224 E. Jefferson Avenue, Grosse Point Park, MI 48230. Tel: (313) 499-1088. Fax: (313) 499-0665.
MINNESOTA	**High Technology Sales,** 4801 West 81st Street, Suite 115, Bloomington, MN 55437. Tel: (612) 844-9933. Fax: (612) 844-9930.
MISSOURI	**Lorenz Sales, Inc.,** 10176 Corporate Square Dr., Suite120, St. Louis, MS 63121. Tel: (314) 997-4558. Fax: (314) 997-5829.
NEBRASKA	**Lorenz Sales,** 2801 Garfield Street, Lincoln, NE 68502. Tel: (402) 475-4660. Fax: (402) 474-7094. **HLM Assoc.,** 333 Littleton Raod, Parsippany, NJ 07054. Tel: (201) 263-1535. Fax: (201) 263-0914.
NEW HAMPSHIRE	**Stone Components,** 436 S. Baboosic Lake Rd., Merrimack, NH 03054. Tel: (603) 429-3462. Fax: (603) 429-3462.
NEW YORK	**HLM Assoc.,** 64 Mariners Lane, Box 328, Northport, NY 11768. Tel: (516) 757-1606. Fax: (516) 757-1636. **Regan Compar,** 3301 Country Club Road, Endwell, NY 13760. Tel: (607) 754-2171 Fax: (607) 754-4270. **Regan Compar,** 214 Dorchester Avenue, Syracuse, NY 13202. Tel: (315) 432-8232. Fax: (315) 432-8238. **Regan Compar,** 37A Brookhill Lane, Rochester, NY 14625. Tel: (716) 271-2230. Fax: (716) 381-2840.
OHIO	**Scott Electronics, Inc.,** 3131 S. Dixie Dr., Suite 200, Dayton, OH 45434. Tel: (513) 294-0539. Fax: (513) 294-4769. **Scott Electronics, Inc.,** 30 Alpha Park Drive, Cleveland, OH 44143. Tel: (216) 473-5050. Fax: (216) 473-5055. **Scott Electronics, Inc.,** 916 Eastwind Dr., Westerville, OH 43081. Tel: (614) 882-6100. Fax: (614) 882-0900. **Scott Electronics, Inc.,** 10901 Reed Hartman Hwy., Suite 301, Cincinnati, OH 45242. Tel: (513) 791-2513. Fax: (513) 791-8059.
PENNSYLVANIA/ NEW JERSEY	**Metz-Jade Associates, Inc.,** 7 Wynnewood Rd, Suite 203, P.O.Box 276, Wynnewood, PA 19096. Tel: (215) 896-7300. Fax: (215) 642-6293.
TEXAS	**Oeler & Menelaides, Inc.,** 8430 Meadow Rd., Suite 224, Dallas, TX 75231. Tel: (214) 361-8876. Fax: (214) 692-0235. **Oeler & Menelaides, Inc.,** 8705 Shoal Creek Rd., #103, Austin, TX 78758. Tel: (512) 453-0275. Fax: (512) 453-0088.
WISCONSIN	**Micro Sales, Inc.,** 210 Regency Ct., Suite L101, Waukesha, WI 53186-0545. Tel: (414) 786-1403. Fax: (414) 786-1813.
CANADA	**GM Assoc. Inc.,** 7050 Bramalea Road, Mississauga, Ontario L5S 1T1 (Toronto). Tel: (416) 671-8111. Fax: (416) 671-2422. **GM Assoc. Inc.,** 3860 Cote-Vertu, St. Laurent, Quebec H4R 1N4. Tel: (514) 335-9572. Fax: (514) 335-9573.

GM Assoc. Inc., 301 Moodie Dr., Nepean, Ontario K2H 9CR (Ottawa).
Tel: (613) 820-3822. Fax: (613) 820-7633.
GM Assoc. Inc., 300-3665 Kingsway, Vancouvr, BC V5R 5W2.
Tel: (604) 439-3383. Fax: (604) 439-8479.

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Tel: 612 638 1888. Fax: 612 638 1798.

AUSTRIA — **Eurodis Electronics GmbH,** Lamezanstrasse 10, A-1232 Wien.
Tel: 1 610620. Fax: 1 61062151.

BULGARIA — **Macro Sofia,** 116 Geo Miller Str, Bl 57 AP70, 1574 Sofia. Tel/Fax: 359 2 708140.

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Tel: (613) 727-8325. Fax: (613) 727-9489.
Semad (Corp.), 85 Spy Court, Markham, Ontario L3R 4Z4.
Tel: (416) 475-8500. Fax: (416) 475-4158.
Semad, 243 Place Frontenac, Pointe Claire, Que H9R 4Z7.
Tel: (514) 694-0860. Fax: (514) 694-0965.
Semad, 6815 8th St. N.E., Ste. 175, Calgary, Alberta T2E 7H7.
Tel: (403) 252-5664 Fax: (604) 420-0124.
Semad, 8563 Government St, Burnaby, BC V3N 4S9.
Tel: (604) 420-9889. Fax: (604) 420-0124.

CHINA — **Gain Tune Ltd,** Room 709, Oriental Building, 39 Jianshe Road,
Shenzen, China.Tel: 755-2284970. Fax: 755-2284971.
World Peace Industrial Co Ltd, Room 709, Oriental Building, 39 Jianshe Road,
Shenzen, China.Tel: 755-2284970. Fax: 755-2284972.

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Tel: 42 2 3112182. Fax: 42 2 24310335.

DENMARK — **Scansupply A/S,** Gladsaxevej 356, DK-2860 Soeborg.
Tel: 45 39 66 50 90. Fax: 45 39 66 50 40.
Scansupply A/S, Marselisborg Havnevej 36, 8000 Arhus C.
Tel: 45 86 12 77 88. Fax: 45 86 12 77 18.

EASTERN EUROPE — **FA Bernhart GmbH,** Melkstattweg 27, PO Box 1628, D 8170 Bad Toelz., Germany.
Tel: 80 41 41 676 Fax: 80 41 71 504 Tx: 526246 FABD.

FRANCE — **3D:**
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Fax: 1 64 47 00 84.
3 rue Berthelot, 69627 Villeurbanne CEDEX. Tel: 72 35 22 00. Fax: 72 34 67 72.
Z.I. du terroir, rue de l'industrie, 31140 Saint Alban.
Tel: 61 37 44 00. Fax: 61 37 44 29.
Parc Club du golf, Batiment 1, 13856 Aix-en-Provence CEDEX 3. Tel: 91 61 80 20.
Omnitech Sertronique:
C.A. de Montheard, 11 rue Edgar-Brant, 72016 Le Mans CEDEX.
Tel: 43 86 74 74. Fax: 43 86 74 86.
165 boulevard de Valmy, Batiment Evolic 1, 92706 Colombes.
Tel: 1 46 13 07 80. Fax: 1 46 13 07 90.
ZAC des Petites Landes, 44470 Thouare-sur-Loire. Tel: 40 68 06 07.
Fax: 40 68 06 72.
99 boulevard de l'Artillerie, 69007 Lyon. Tel: 72 73 11 87. Fax: 72 73 18 00.
37 rue Saint-Eloi, 76000 Rouen. Tel: 35 88 00 38. Fax: 35 15 06 22.
18/20 rue Cabanis, 59007 Lille. Tel: 20 33 21 97. Fax: 20 56 00 49.
Parc Cadera, Batiment F, 33700 Bordeaux. Tel: 56 34 46 00. Fax: 56 34 47 13.

GERMANY	**AS Electronic Vertriebs GmbH,** In den Garten 2, D-61352 Bad Homburg. Tel: 06172 458931. Fax: 06172 42000.
	Astronic GmbH, Gruenwalder Weg 30, D-82041 Deisenhofen. Tel: 089 6130303. Fax: 089 6131668.
	Micronetics GmbH, Dieselstrasse 12, D-71272 Renningen. Tel: 07159-925830. Fax: 07159-9258355.
	Weisbauer Elektronik GmbH, Heiliger Weg 1, D-44135 Dortmund. Tel: 0231 579547. Fax: 0231 577514.
GREECE	**Impel Ltd.,** 30 Rodon Str, Korydallos, Piraeus, Greece. Tel: 010 30 1 49 67815. Tlx: 213835. Fax: 01 49 54041.
HONG KONG	**Gain Tune Ltd,** Room 809, 8th Floor, Hunghom Commercial Centre, Tower B, 37-39 Ma Tau Wai Road,Hunghom, Kowloon, Hong Kong. Tel: 852-3654860. Fax: 852-7641129.
HUNGARY	**Macro Group,** Etele ut 68,Budapest 1115. Tel: 36 1 2698110/1853111. Fax: 36 1 1850061.
INDIA	**Mekaster Telecom PVT Ltd.,** 908 Ansal Bhawan, 16 Katuba Ghandi Marg, New Delhi, 100 001 India Tel: 11 3312110 Fax: 11 3712155.
ITALY	**Adelsy - Divisione della Generalmusic SpA,** Via Novara 570, 20153 Milano. Tel: 02 3810310. Fax: 02 38002988.
	Eurelettronica SpA, Via E. Fermi 8, 20090 Assago (MI). Tel: 02 457841. Fax: 02 4880275.
	Fanton Srl, Milano - Torino - Bologna - Firenze - Roma - Padova. Tel: 02 48912963. Fax: 02 4890902.
JAPAN	**Cornes & Company Ltd.,** 2-5-12 Higashi-Kanda, Chiyoda-ku. Tokyo 101. Tel: 3-5821-1651. Fax: 3-5821-1904.
	Cornes & Company Ltd., Cornes House, 13-40 Nishi-honmachi 1-chome, Nishi-Ku, Osaka 550. Tel: 6 532 1012.Tx: 525-4496. Fax: 6 541-8850.
KOREA	**KML Corporation,** 6th Floor, Dukmyung Building, (A-Dong) 113-3, Banpo-Dong, Shucho-Gu, CPO Box 7981, Seoul. Tel: 2 595 9101-6. Fax: 2 595 9107.
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NETHERLANDS	**Tekelek-Airtronic B.V.,** PO Box 63, NL-2700 AB Zoetermeer. Tel: 079 310100. Fax: 079 417504
NORWAY	**Skandinavisk Elektronikk A/S,** Ostre Aker Vei 99, Postboks 99 Veitvet, Oslo 5. Tel: 22 64 11 50. Tx: 71963 Fax: 22 64 34 43.
POLAND	**Macropol Co. Ltd,** Ul Bitwy Warszawskiej 11, 02 366 Warsaw. Tel: 48 22 224337. Fax: 48 22 229136.
PORTUGAL	**Anatronic SL,** Urbanisazao Do, Infantado, Lote 18, 2° ESQ, Loures. Tel: 1 79 33 2 99.
RUSSIA	**Anastasia Neklusova,** St Petersburg, Ul Zamshina 15. Tel: 7 812 545 0723. Fax: 7 812 254 51256.
SLOVAK REPUBLIC	**Macro Zilinia,** Vysokoskolakov 6, 010-01 Zilinia. Tel: 42 89 634181/45041. Fax: 42 89 634109.
SOUTH AFRICA	**T.E.C. Tellumat Electronic Components,** 1 Jansen Road, Jet Park, Boksburg 1459, P.O. Box 8174, Elandsfontein 1406. Tel: 2711 823 2950. Fax: 2711 823 2668.
SPAIN	**Anatronic SA,** Avda de Valladolid 27, 28008 Madrid. Tel: 91 542 4455/6. Fax: 91 2486975.
	Anatronic SA, Bailen, 176, Estresuelo 1°, 08037 Barcelona. Tel: 93 258 1906/7. Fax: 93 258 7128.
SWEDEN	**Pronesto AB (Microwave Products Only),** Finlandsgatan 18, 16475 Kista. Tel: (08) 752 9080. Fax: (08) 751 4111.
SWITZERLAND	**Basix für Electronik AG,** Hardturmstr 181, CH-8010 Zuerich. Tel: 1 2761111. Fax: 1 2764199.
TAIWAN	**Prospect Technology Corporation,** 5, Lane 55, Long-Chiang Road, Taipei, Taiwan. Tel: (886-2) 721-9533. Fax: (886-2) 773-3756.
	World Peace Industrial Co Ltd, 8th Floor, 76 Cheng Kung Road, Sec. I., Nankang District, Taipei, Taiwan ROC. Tel: (886-2) 788-5200. Fax: (886-2) 788-3255.

THAILAND	**Westech Electronics Co. Ltd,** 77/113 Moo Ban Kitikorn, Ladprao Soi 3, Ladprao Road, Ladyao, Jatujak, Bangkok 10900. Thailand. Tel: 2 5125531. Fax: 2 2365949.
TURKEY	**EMPA,** 34630, Besyol Londra Asfalti Florya Is Merkezi Sefakoy, Istanbul. Tel: (1) 599 30 50 Tx: 21137 Etna tr Fax: (1) 598 53 53.
UNITED KINGDOM	**Celdis Ltd.,** 300 Kings Road, Reading, Berks RG1 4GA. Tel: 0734 666676. Tx: 818142. Fax: 0734 263100.
	ESD Distribution Ltd, Edinburgh Way, Harlow, Essex CM20 2DF. Tel: 0279 626777. Tlx: 818801. Fax: 0279 441687.
	Farnell Electronic Components Ltd., Canal Road, Leeds LS12 2TU. Tel: 0532 636311. Tx: 55147. Fax: 0532 633404.
	Gothic Crellon Ltd., 3 The Business Centre, Molly Millars Lane, Wokingham, Berkshire RG11 2EY. Tel: 0734 788878, 787848. Tx: 847571. Fax: 0734 776095.
	Gothic Crellon Ltd., P.O.Box 301, Elizabeth House, 22 Suffolk Street, Queensway, Birmingham B1 1LZ. Tel: 021 643 6365. Tx: 338731. Fax: 021 633 3207.
	Macro Group, Burnham Lane, Slough SL1 6LN. Tel: 0628 604383. Fax: 0628 666873/668071.
	Semiconductor Specialists (UK) Ltd., Carroll House, 159 High Street Yiewsley, West Drayton, Middlesex UB7 7XB Tel: (0895) 445522. Tx: 21958. Fax: (0895) 422044.
	Unitel Ltd., Unitel House. Fishers Green Road, Stevenage, Herts. Tel: (0438) 312393. Tx: 825637. Fax: (0438) 318711.
USA: Alabama	**Pioneer Technologies,** 4835 University Square #5, Huntsville, AL 35816. Tel: (205) 837-9300. Fax: (205) 837-9358.
	Hammond, 4411-B Evangel Circle NW, Huntsville, AL 35816. Tel: (205) 830-4764. Fax: (205) 830-4287.
Arizona	**Insight Electronics,** 1515 W. University Dr., Suite 103. Tempe, AZ 85281. Tel: (602) 829-1800. Fax: (602) 967-2658.
California	**Insight Electronics (Corp.),** 6885 Flanders Dr., Unit C, San Diego, CA 92121. Tel: (619) 587-0471. Fax: (619) 587-0903.
	Insight Electronics, 2 Venture Plaza, Ste. 340, Irvine, CA 92718. Tel: (714) 727-3291. Fax: (714) 727-1804.
	Insight Electronics, 4333 Park Terrace Dr., Ste. 101, Westlake Village, CA 91361. Tel: (818) 707-2101. Fax: (818) 707-0321.
	Insight Electronics, 1295 Oakmead Parkway, Sunnyvale, CA 94086. Tel: (408) 720-9222. Fax: (408) 720-8390.
	Pioneer Standard, 217 Technology Dr., Ste. 110, Irvine, CA 92718. Tel: (714) 753-5500. Fax: (714) 753-5074.
	Pioneer Standard, 5850 Canogo Ave., Ste. 400, Woodland Hills, CA 91367. Tel: (818) 883-4640. Fax: (818) 883-9721.
	Pioneer Technologies, 134 Rio Robles, San Jose, CA 95134. Tel: (408) 954-9100. Fax: (408) 954-9113.
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	Pioneer Technologies, 2200 Gateway Centre Blvd., Ste. 215, Morrisville, NC 27560. Tel: (919) 460-1530. Fax: (919) 460-1540.
South Carolina	**Hammond,** 1035 Lowndes Hill Rd., Greenville, SC 29607. Tel: (803) 232-0872. Fax: (803) 232-0320.
Colorado	**Insight,** 384 Inverness Dr. S., Ste. 105, Engelwood, CO 80112. Tel: (303) 649-1800. Fax: (303) 690-4754.
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	Hammond Orlando (Corp.), 1230 West Central Blvd., Orlando, FL 32805. Tel: (407) 849-6060. Fax:(407) 648-8584.

Pioneer Technologies, 674 South Military Trail, Deerfield Beach, FL 33442.
Tel: (305) 428-8877. Fax: (305) 481-2950.
Pioneer Technologies, 337 South Northlake Blvd., #1000, Altamonte Springs.
FL 32701 Tel: (407) 834-9090. Fax: (407) 834-0865.

Georgia **Hammond,** 5680 Oakbrook Pkwy., Suite 160, Norcross, GA 30093.]
Tel: (404) 449-1996. Fax: (404) 242-9834.
Pioneer Technologies, 4250C Rivergreen Pkwy., Duluth, GA 30136.
Tel: (404) 623-1003. Fax: (404) 623-0665

Illinois **Pioneer Standard,** 2171 Executive Drive #104, Addison, IL 60101.
Tel: (708) 495-9680. Fax: (708) 495-9831

Indiana **Pioneer Standard,** 9350 N. Priority Way W. Drive, Indianapolis, IN 46240.
Tel: (317) 573-0880. Fax: (317) 573-0979

Maryland **Pioneer/Tech. Group. Inc.,** 9100 Gaither Rd., Gaithersburg, MD 20877.
Tel: (301) 921-0660. Fax: (301) 921-4255

Massachusetts **Pioneer Standard,** 44 Hartwell Avenue, Lexington, MA 02173. Tel: (617) 861-9200.
Fax: (617) 863-1547

Michigan **Pioneer Standard,** 13485 Stamford, Livonia, MI 48150. Tel: (313) 525-1800.
Fax: (313) 427-3720.
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Tel: (616) 698-1800. Fax: (616) 698-1831.

Minneapolis **Pioneer Standard,** 7625 Golden Triangle Dr., Eden Prairie, MN 55344.
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Tel: (314) 432-4350. Fax: (314) 432-4854.

New Jersey **Pioneer Standard,** 14-A Madison Rd.. Fairfield, NJ 07006. Tel: (201) 575-3510.
Fax: (201) 575-3454.

New Mexico **Alliance Electronics,** 10510 Research Rd. SE, Albuquerque, NM 87123.
Tel: (505) 292-3360 Fax: (505) 275-6392

New York **Mast,** 710-2 Union Pkwy., Ronkonkoma, NY 11779. Tel: (516) 471-4422.
Fax: (516) 471-2040.
Pioneer Standard, 68 Corporate Drive, Binghamton, NY 13904.
Tel: (607) 722-9300. Fax: (607) 722-9562.
Pioneer Standard (Corp.), 60 Crossways Park West, Woodbury, NY 11797.
Tel: (516) 921-8700 Fax: (516) 921-2143.
Pioneer Standard, 840 Fairport Park, Fairport, NY 14450. Tel: (716) 381-7070.
Fax: (716) 381-5955.

Ohio **Pioneer Standard,** 4800 East 131st St., Cleveland, OH 44105.
Tel: (216) 587-3600. Fax: (216) 587-3906.
Pioneer, 4433 Interpoint Blvd., Dayton, OH 45424. Tel: (513) 236-9900. .
Fax: (513) 236-8133.

Oregon **Insight,** 8705 SW Nimbus Ave., #200, Beaverton, OR 97005. Tel: (503) 644-3300

Pennsylvania **Pioneer Technologies,** Keith Valley Business Center, Horsham, PA 19044.
Tel: (215) 674-4000. Fax: (215) 674-3107.
Pioneer Standard, 259 Kappa Drive, Pittsburgh, PA 15238. Tel: (412) 782-2300.
Fax: (412) 963-8255.

Texas **Insight,** 12701 Research Bl.Ste 301, Austin, TX 78759.
Insight, 1778 Plano Rd., Suite 320, Richardson, TX 75081. Tel: (214) 783-0800.
Fax: (214) 680-2402.
Insight,15437 McKaskle, Sugarland, TX 77478.
Pioneer Standard, 1826-D Kramer Ln., Austin. TX 78758. Tel: (512) 835-4000.
Fax: (512) 835-9829.
Pioneer Standard, 13765 Beta Road, Dallas, TX 75244.
Tel: (214) 386-7300. Fax: (214) 490-6419.
Pioneer Standard, 10530 Rockley Rd. #100, Houston, TX 77099.
Tel: (713) 495-4700. Fax: (713) 495-5642.

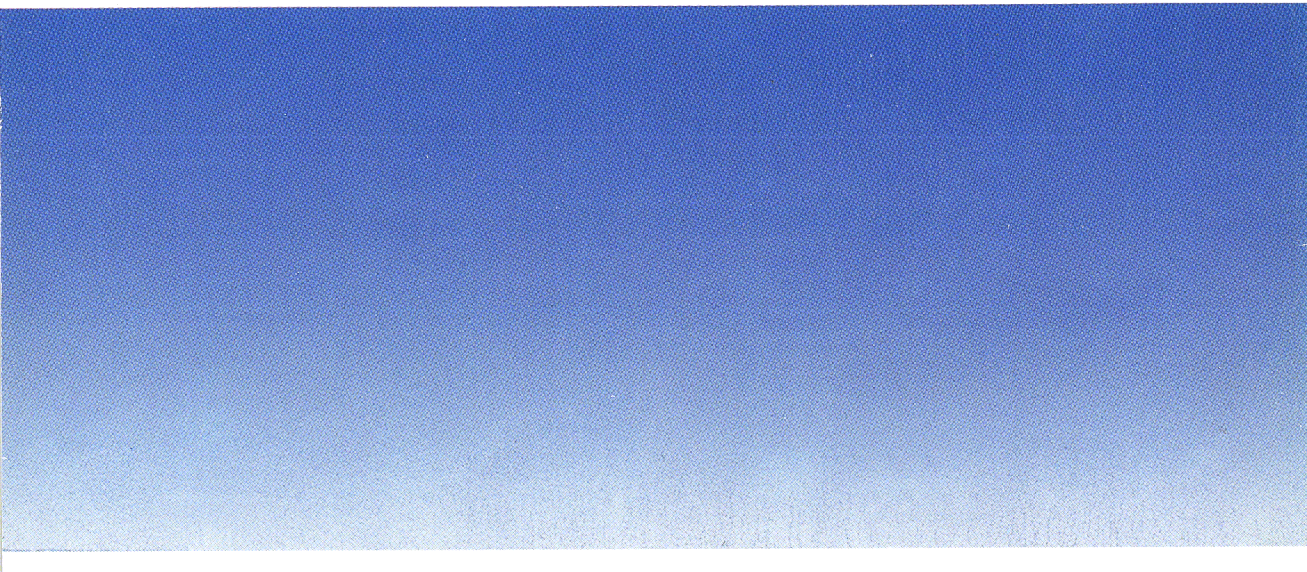
Washington	**Insight,** 12002 115th Ave. N.E., Kirkland, WA 98034. Tel: (206) 820-8100. Fax: (206) 821-2976.
Wisconsin	**Pioneer Standard,** 120 Bishop's Way #163, Brookfield, WI 53005. Tel: (414) 784-3480. Fax: (414) 784-8207.

UK Export

(To countries other than those listed)	**GEC Plessey Semiconductors ,** Unit 1, Crompton Road, Groundwell Industrial Estate, Swindon, Wilts, UK SN2 5AF. Tel: (0793) 518510. Fax: (0793) 518582. **Whiteaway Laidlaw (Overseas) Ltd.,** PO Box 93, Ambassador House, Devonshire Street North, Manchester M60 6BU Tel: 061 273 3228 Fax: 061 274 3757

Publication No. HB2480-2.0 June 1994

Supersedes PS2480-1.0 May 1991 Edition



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